Collating List of Pages

This reference drawing contains the collating sequence, page side, and EC level of pages for *IBM 3480 Magnetic Tape Subsystem Maintenance Information Manual (MI) Volume A04*, SY32-5055-13.

The part number of the divider tab list is 8673746.

This reference drawing is to be placed at the front of the manual.

PAGE	SIDE	LEVEL
FRONT COVER	Front	EC C13783
PREF 1	Back	EC 336395
TAB 1	Front	EC 336395
TAB 2	Back	EC 336395
LGND Tab		
LGND 1	Front	EC 336395
LGND 5	Back	EC 336395
LGND 10	Front	EC 336396
LGND 15	Back	EC 336396
LGND 20	Front	EC 336395
LGND 25	Back	EC 336395
LGND 30	Front	EC 336395
LGND 35	Back	EC 336395
LGND 40	Front	EC 336395
LGND 45	Back	EC 336395
LGND 46	Front	EC 336395
LGND 47	Back	EC 336395
LGND 48	Front	EC 336396
LGND 50	Back	EC 336396
LGND 55	Front	EC 336395
LGND 60	Back	EC 336395
LGND 65	Front	EC 336396
LGND 70	Back	EC 336396
LGND 75	Front	EC 336395
LGND 80	Back	EC 336395

PAGE	SIDE	LEVEL
SPROC Tab		
SPROC 1	Front	EC A57723
SPROC 2	Back	EC A57723
SPROC 3	Front	EC 336395
SPROC 4	Back	EC A57723
SPROC 100	Front	EC A57723
SPROC 110	Back	EC A57723
SPROC 120	Front	EC A57723
SPROC 130	Back	EC A57723
SPROC 140	Front	EC A57723
SPROC 150	Back	EC A57723
SDISK Tab		
SDISK 1	Front	EC 336395
SDISK 100	Back	EC 336395
SDISK 105	Front	EC A57724
SDISK 110	Back	EC 336395
SDISK 111	Front	EC 336396
SDISK 115	Back	EC A57724
SDISK 116	Front	EC A57724
SDISK 120	Back	EC 336396
SDISK 121	Front	EC 336396
SDISK 125	Back	EC 336396
SDISK 126	Front	EC 336395
SDISK 130	Back	EC 336395

PAGE	SIDE	LEVEL
SDISK 131	Front	EC 336395
SDISK 135	Back	EC 336395
SDISK 140	Front	EC 336395
SDISK 145	Back	EC A47957
SDISK 146	Front	EC A57723
SDISK 150	Back	EC 336396
SDISK 155	Front	EC 336395
SDISK 160	Back	EC 336395
SDISK 165	Front	EC A47957
SDISK 170	Back	EC 336396
DIAG Tab		
DIAG 1	Front	EC A57723
DIAG 2	Back	EC A57723
DIAG 3	Front	EC A57723
DIAG 4	Back	EC 336395
DIAG 5	Front	EC 336395
DIAG 6	Back	EC 336395
DIAG 7	Front	EC 336395
DIAG 20	Back	EC 336395
DIAG 30	Front	EC 336395
DIAG 32	Back	EC 336395
DIAG 34	Front	EC 336395
DIAG 50	Back	EC 336395
DIAG 55	Front	EC 336395
DIAG 60	Back	EC 336395
DIAG 65	Front	EC A57723
DIAG 66	Back	EC A57723
DIAG 70	Front	EC A57723
DIAG 100	Back	EC 336395

PAGE	SIDE	LEVEL
DIAG 102	Front	EC A57723
DIAG 104	Back	EC 336395
DIAG 105	Front	EC A57723
DIAG 106	Back	EC A57721
DIAG 110	Front	EC A57723
DIAG 112	Back	EC A57723
DIAG 114	Front	EC A57723
DIAG 118	Back	EC A57723
DIAG 120	Front	EC A57723
DIAG 124	Back	EC A57723
DIAG 150	Front	EC 336395
DIAG 152	Back	EC 336395
DIAG 160	Front	EC 336395
DIAG 162	Back	EC 336395
DIAG 164	Front	EC 336395
DIAG 166	Back	EC 336395
DIAG 170	Front	EC 336395
DIAG 200	Back	EC A57693
DIAG 202	Front	EC A57724
DIAG 204	Back	EC A57693
DIAG 206	Front	EC A57693
DIAG 208	Back	EC 336395

Collating List of Pages

PAGE	SIDE	LEVEL
DIAG 210	Front	EC 336395
DIAG 212	Back	EC 336395
DIAG 214	Front	EC 336395
DIAG 218	Back	EC A57693
DIAG 219	Front	EC A57693
DIAG 220	Back	EC 336395
DIAG 222	Front	EC 336396
DIAG 224	Back	EC 336396
DIAG 226	Front	EC 336396
DIAG 228	Back	EC 336396
DIAG 229	Front	EC 336395
DIAG 300	Back	EC A57724
DIAG 301	Front	EC A47957
DIAG 302	Back	EC A47957
DIAG 304	Front	EC 336395
DIAG 306	Back	EC 336395
DIAG 308	Front	EC 336395
DIAG 310	Back	EC 336395
DIAG 312	Front	EC 336395
DIAG 320	Back	EC 336395
DIAG 321	Front	EC 336396
DIAG 322	Back	EC 336396
DIAG 323	Front	EC 336396
DIAG 324	Back	EC 336396
DIAG 326	Front	EC 336395
DIAG 328	Back	EC 336395
DIAG 330	Front	EC 336395
DIAG 332	Back	EC 336395
DIAG 334	Front	EC 336395
DIAG 336	Back	EC 336395
DIAG 338	Front	EC 336395
DIAG 340	Back	EC 336395
DIAG 342	Front	EC 336395
DIAG 344	Back	EC 336395

PAGE	SIDE	LEVEL
DIAG 346	Front	EC 336395
DIAG 348	Back	EC 336395
DIAG 400	Front	EC A57723
DIAG 402	Back	EC 336395
DIAG 410	Front	EC 336396
DIAG 412	Back	EC 336396
DIAG 450	Front	EC 336396
DIAG 452	Back	EC 336396
DIAG 454	Front	EC 336395
DIAG 460	Back	EC 336395
DIAG 462	Front	EC 336395
DIAG 500	Back	EC 336395
DIAG 501	Front	EC 336395
DIAG 502	Back	EC 336395
DIAG 503	Front	EC 336396
DIAG 504	Back	EC 336396
DIAG 506	Front	EC 336395
DIAG 508	Back	EC 336395
DIAG 509	Front	EC 336395
DIAG 510	Back	EC 336395
DIAG 511	Front	EC 336395
DIAG 512	Back	EC 336395
DIAG 514	Front	EC 336395
DIAG 516	Back	EC 336395
DIAG 518	Front	EC 336395
DIAG 520	Back	EC 336395
DIAG 522	Front	EC 336396
DIAG 524	Back	EC 336396
DIAG 526	Front	EC 336395
DIAG 528	Back	EC 336395
DIAG 530	Front	EC 336395
DIAG 532	Back	EC 336395
DIAG 534	Front	EC 336395
DIAG 536	Back	EC 336395

PAGE	SIDE	LEVEL
DIAG 538	Front	EC 336396
DIAG 540	Back	EC 336396
DIAG 542	Front	EC 336395
DIAG 544	Back	EC 336395
DIAG 550	Front	EC C13783
DIAG 551	Back	EC 336395
DIAG 552	Front	EC 336395
DIAG 554	Back	EC C13783
DIAG 556	Front	EC 336395
DIAG 558	Back	EC 336395
DIAG 560	Front	EC 336395
DIAG 562	Back	EC 336395
DIAG 564	Front	EC 336396
DIAG 566	Back	EC 336396
DIAG 568	Front	EC 336395
DIAG 570	Back	EC 336395
DIAG 572	Front	EC 336395
DIAG 574	Back	EC 336395
DIAG 576	Front	EC 336395
DIAG 578	Back	EC 336395
DIAG 580	Front	EC 336396
DIAG 582	Back	EC 336396
DIAG 584	Front	EC 336395
DIAG 586	Back	EC 336395
DIAG 600	Front	EC A57723
DIAG 605	Back	EC 336396
DIAG 610	Front	EC 336395
DIAG 615	Back	EC 336395
DIAG 620	Front	EC 336395
DIAG 720	Back	EC A57723
DIAG 721	Front	EC A47957
DIAG 722	Back	EC 336396
DIAG 725	Front	EC A57693
DIAG 755	Back	EC 336395

PAGE	SIDE	LEVEL
DF Tab		
DF 1	Front	EC A57723
DF 3	Back	EC 336395
DF 5	Front	EC A57723
DF 10	Back	EC 336395
DF 12	Front	EC A57723
DF 15	Back	EC 336395
DF 20	Front	EC 336395
DF 25	Back	EC 336395
DF 30	Front	EC 336395
DF 33	Back	EC 336395
DF 35	Front	EC 336395
DF 36	Back	EC A57723
DF 37	Front	EC A57723
DF 40	Back	EC 336395
DF 45	Front	EC A57724
DF 50	Back	EC 336395
DF 55	Front	EC 336395
DF 60	Back	EC A57721
DF 62	Front	EC 336395
DF 65	Back	EC 336395
DF 70	Front	EC 336396
DF 75	Back	EC 336396
DF 80	Front	EC 336395
DF 82	Back	EC 336395
DF 85	Front	EC 336395
DF 88	Back	EC A57723
DF 88-1	Front	EC A57723
DF 88-2	Back	EC A57723
DF 90	Front	EC 336395
DF 95	Back	EC 336395
DF 100	Front	EC 336395
DF 105	Back	EC 336395

Collating List of Pages

PAGE	SIDE	LEVEL
DF 110	Front	EC 336395
DF 115	Back	EC 336395
DF 117	Front	EC 336395
DF 120	Back	EC A57723
DF 125	Front	EC 336395
DF 130	Back	EC 336395
DF 135	Front	EC 336395
DF 140	Back	EC 336396
DF 145	Front	EC 336396
DF 150	Back	EC 336395
DF 155	Front	EC 336395
DF 160	Back	EC A57721
OPER Tab		
OPER 1	Front	EC 336395
OPER 2	Back	EC A47957
OPER 5	Front	EC 336396
OPER 10	Back	EC A57721
OPER 15	Front	EC 336395
OPER 20	Back	EC A57723
OPER 25	Front	EC A57693
OPER 30	Back	EC A57693
OPER 35	Front	EC 336395
OPER 40	Back	EC 336395
OPER 45	Front	EC 336396
OPER 50	Back	EC 336396
OPER 55	Front	EC 336396
OPER 60	Back	EC 336396
OPER 65	Front	EC 336395
OPER 70	Back	EC 336395
OPER 75	Front	EC 336395
OPER 80	Back	EC 336395
OPER 81	Front	EC 336396
OPER 85	Back	EC C13783
OPER 90	Front	EC A57723
OPER 95	Back	EC A57693
OPER 96	Front	EC 336395
OPER 100	Back	EC A57723
OPER 105	Front	EC 336395
OPER 106	Back	EC 336395
OPER 110	Front	EC 336395
OPER 115	Back	EC A57693
OPER 120	Front	EC 336396
OPER 125	Back	EC 336396
OPER 130	Front	EC 336395
OPER 131	Back	EC 336395
OPER 135	Front	EC 336395
OPER 140	Back	EC 336395
OPER 141	Front	EC 336395
OPER 142	Back	EC 336395
OPER 145	Front	EC 336395
OPER 150	Back	EC 336395
OPER 155	Front	EC A57723
OPER 160	Back	EC 336395
OPER 165	Front	EC A57723
OPER 170	Back	EC A57723
OPER 175	Front	EC 336395
OPER 180	Back	EC 336395
OPER 185	Front	EC 336395
OPER 186	Back	EC 336395
OPER 187	Front	EC 336395
OPER 188	Back	EC 336395
OPER 190	Front	EC 336395
OPER 196	Back	EC 336395
OPER 200	Front	EC 336395
OPER 205	Back	EC 336395
OPER 210	Front	EC 336395
OPER 215	Back	EC 336395
OPER 220	Front	EC A57723
OPER 230	Back	EC A57723
OPER 240	Front	EC A57693
OPER 245	Back	EC A47957
RCF-1	Front	
RCF-2	Back	

3480 MI

PN 8673721	EC A57721	EC A57723	EC A57724	EC C13783	
3 of 3	27 Oct 88	24 Jul 89	11 May 90	30 Sep 91	

8674065

PUBLICATIONS REFERENCE DRAWING

MACHINE TYPE/MODEL NO. 3480

MACHINE NAME - Magnetic Tape Subsystem

FORM NO.	E C NO.	DESCRIPTION/COMMENTS
SY32-5055-0	991552	VOL. A04 - Maintenance Information REA 12-11655
	336326	TNL SN32-0310 IEC 001122571 (REA 12-25744) IEC 002122571 (REA 12-25494, REA 12-25496)
SY32-5055-1	336389	Second Edition IEC 0011215156 IEC 0011225996
SY32-5055-2	336390	Third Edition IEC 0011225997 IEC 0011215157
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	336393	TNL SN32-5036
SY32-5055-5	336394	Sixth Edition
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SY32-5055-8	A47957C	Ninth Edition
SY32-5055-9	A57693	Tenth Edition
SY32-5055-10	A57721	Eleventh Edition
SY32-5055-11	A57723	Twelfth Edition
SY32-5055-12	A57724	Thirteenth Edition
SY32-5055-13	C13783	Fourteenth Edition

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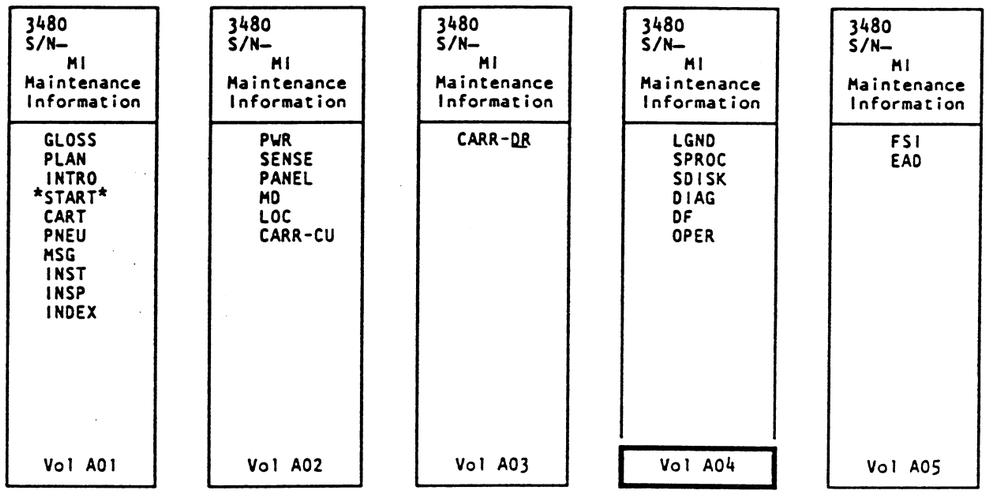
NAME.	PUB REF DWG (PRD)
DESIGN	SHT OF
DETAIL	
CHECK	CLASSIFICATION
APPRO	

	DATE	CHANGE NO		DATE	CHANGE NO
REL	See EC History				
	7/24/89	A57723			
	5/11/90	A57724			
	9/30/91	C13783			

MUST CONFORM TO ENG SPEC	DEVELOPMENT NO	LOGIC PG NO
		RD004

8674065 B

IBM Maintenance Information



Maintenance Library
Maintenance Information **Vols. A01 to A05**
Logic Diagrams **Vols. C01 and D01**

3480 Magnetic Tape Subsystem

SY32-7018-03

Preface

This manual contains maintenance information about the IBM 3480 Magnetic Tape Subsystem and is intended for customer engineers responsible for servicing the 3480 tape subsystem. This publication is designed to be used with the IBM Maintenance Device (MD). Therefore, CEs using this manual should be familiar with that tool.

Prerequisite Knowledge

It is assumed that you have a background in data processing concepts and that you are familiar with the hexadecimal numbering system, stored program concepts, and have a basic understanding of tape subsystems and their relationship to a processor I/O channel.

Related Publications

IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information, GA22-6974.

IBM 3480 Magnetic Tape Subsystem Description, GA32-0042.

How to Update the Maintenance Information

This manual is form number controlled. The 3480 manuals will be updated by Technical Newsletters (TNLs). The TNL cover letter will indicate the new EC level. The entire manual will be updated by major revision. All updates are processed through normal MLC control. The Publications Reference Drawing (PRD) in the front of each volume contains the EC history.

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Tab List

Volume A01

GLOSS	Glossary
PLAN	Maintenance Plan
INTRO	3480 Introduction
START	Start Maintenance
CART	Cartridge Analysis
PNEU	Pneumatic Analysis
MSG	Console Messages and EREP
INST	Installation/Removal
INSP	Safety Check Procedures
INDEX	Index

Volume A02

PWR	Power Maps
SENSE	Sense/Status
PANEL	Panel
MD	Maintenance Device
LOC	Locations
CARR-CU	Control Unit Checks/Adjustments/Removal/Replacement

Volume A03

CARR-DR	Drive Checks/Adjustments/Removal/Replacement

Volume A04

LGND	Legend
SPROC	Support Procedures
SDISK	Support Diskette Procedures
DIAG	Support Diagnostic Descriptions
DF	Data Fields and Registers
OPER	Theory of Operation

Volume A05

FSI	Fault Symptom Index
EAD	Error Analysis Diagrams

Contents

Graphic Symbols and Lines

Keys

Primary Key

Reverse number in a black square. Used in text and diagrams.

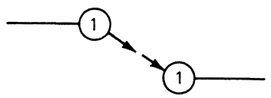
Secondary Key

Reverse letter in black circle. Used in text when keying to a test point symbol in a diagram.

Connectors

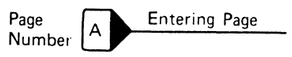
On-Page Connectors

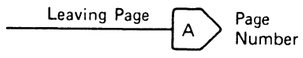
Connection between parts of the same diagram. Arrows point to remote connectors and indicate flow direction of the line.



Off-Page Connectors

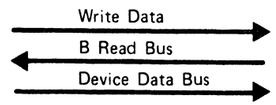
Connection between diagrams on separate pages. Letter keys are used to identify corresponding points.



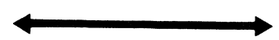


Bus and Control Lines

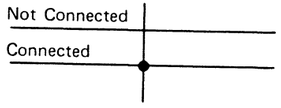
Minor Bus Lines



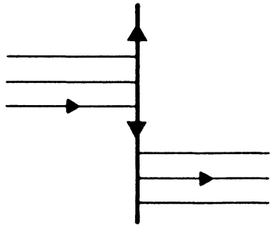
Major Bus Line



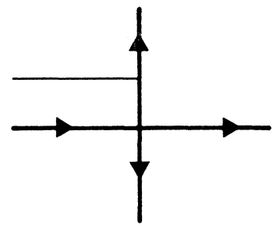
Control Lines



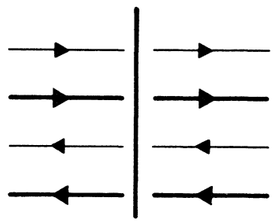
Bus or cable with multiple control lines entering and exiting.



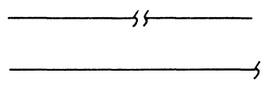
Bus and control lines that connect to a bus.



Bus and control lines that do not connect to a bus.



Standard line break, used when a line break is needed.



Legend

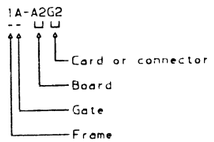
Identifying Parts

Two different formats are used in the maintenance information (MI) and logic diagrams to represent the unit that a part is located.

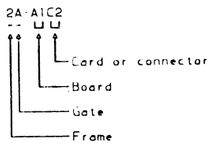
Examples of the First Format:

1A-A1H4
1A-A1D2-U06
1A-A1E2-W22
1A-A2G2
2A-A1C2

Control Unit Logic Part Definitions

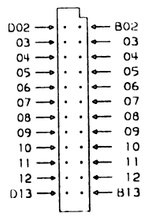


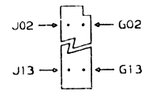
Tape Unit Logic Part Definitions

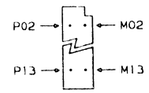


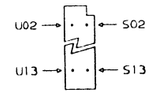
lgnd10a

Card Connector Pins (View from end of card)

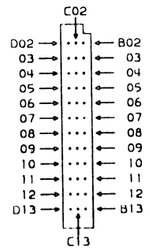


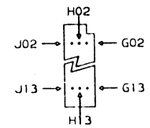


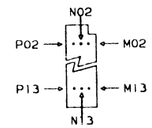


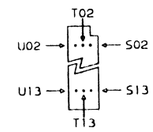


Card Connector Pins (View from end of card (02A-A1B2 card only)



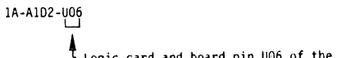






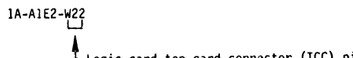
lgnd10b

Logic Board Card Pin Position Identifiers



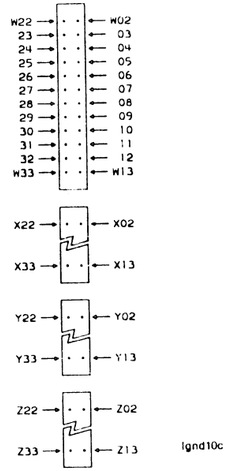
Logic card and board pin U06 of the 1A-A1D2 board position (this is the pin connection between the logic board and the logic card bottom card connector (BCC) or other connector in that position.

Logic Board Card Pin Position Identifiers



Logic card top card connector (TCC) pin W22 for the logic card in position 1A-A1E2 (the TCC is a card to card connector located on the non-pin side of the card and provides for card to card connections or a single wide TCC connects TCC card pins within a card.

Top card connector (TCC) pins (View from the top of the card)



lgnd10c

Examples of the Second Format:

1A-T1A1	TU-D1-PA-J1-D12
1A-T1A3Y	TU-D0/D1-A1-C1B11
2A-A1Z2	TU-D0/D1-P1-3
1A-A2Y2	TU-D0/D1-DK-P7-4
CU-P2A4	TU-D0-EL-J7-1
CU-PS-01-J1-3	TU-D1-DSP-P1-D11
CU-L/R-P2-2	TU-PS-01-P11-3
CU-A1-TB3-6	TU-PS1-J2-9
CU1AP1-3	TU-D0-P1-WA2-D05
TU-D0-PA-J1-D12	TU-D1-A1-A2-B12

Subsystem Unit Identifiers

1A-....	Control unit
CU-....	Control unit
2A-....	Tape unit
TU-....	Tape unit

Tape Drive Unit Identifiers

For subsystems unit with identifiers of TU or 2A only.

TU-D0....

TU-D1....

TU-D0/D1

2A-D0/D1

2A-... --- or TU-... --- TU-D0-.. -- TU-D1-.. -- TU-D0/D1-.. --	(when no D0 or D1) The next numbers are the functional area within the tape unit, **not** the individual drives within the tape unit. Drive 0 - the remaining numbers pertain to FRUs or parts in drive 0. Drive 1 - the remaining numbers pertain to FRUs or parts in drive 1. Drive 0/1 - the remaining numbers pertain to FRUs or parts in both drive 0 and drive 1.

Logic Location Area Identifiers

1A-T1A1... ----	TU-D0/D1-A1... --
CU-P2A4... ----	TU-D0/D1-P1-P1... -----
CU-PS-01... -----	TU-D0/D1-DK... --
CU-L/R-P2... ------	TU-D1-DSP... ---
CU-A1-TB3... -----	TU-PS-01... -----
TU-D0-MSG... ---	TU-D0-P1-WA2... ------

Note: *For descriptions, locations, and remove/replace procedures for the location area identifiers, see the following for:*

- *Control unit – "Figure 1. Control Unit Location Area Definitions"*
- *Tape unit and tape drives – "Figure 2. Tape Unit and Drives Location Area Definitions"*

Part Location Identifiers

CU-PS-01-J1-3 ----	(pin 3 of connector J1) --
CU-L/R-P2-2 ----	(pin 2 of connector P2) -----
TU-D0/D1-A1-C1B11 -----	(pin B11 of position C1) --
TU-PS-01-P11-3 ------	(pin 3 of connector P11) ---
TU-PS1-J2-9 -----	(pin 9 of connector J2) -----
TU-D0-P1-WA2-D05 ---	(pin D05 of connector WA2) ------

Legend

The following figures show how to locate parts in the 3480 documentation, using the identifying numbers that are shown in "Examples of the Second Format" on LGND 10.

For the part location area that is used in the logics, the figures show where they are located in the 3480 subsystem by referencing the "Table of Contents" entry in the LOC and CARR sections of the Maintenance Information. The LOC and CARR sections "Table of Contents" may not be the exact name or FRU number of the part referenced in the logic, however the page referenced by the "Table of Contents" will relate to the part you are looking for.

These figures also show where a part can be found in the logics. For example, if the power is suspected to be a problem, you can look for power parts (CBs, Power Supplies, and so forth) and find the logic pages that show these areas.

Control Unit Location Area Definitions

LOGIC LOCATION AREA IDENTIFIER	DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
1AP1	Connectors for gate fans	YF005	Fan Assemblies 1 and 2	FRU165
+24v Service Switch	Service switch	ZT020	CU-A1 Logic Gate (Hinge Side)	FRU162
A1	Logic board	AA000 AA100	01A-A1 Logic Board	FRU139
A1A2	Logic board position A2	AA000	01A-A1 Logic Board	FRU139
A1Y2	Logic board connector Y2 at top of board	AA000	01A-A1 Logic Board	FRU139
A1Z2	Logic board connector at bottom of board	AA000	01A-A1 Logic Board	FRU139
A1P2Y	Single wide TCC board position P2 row y	AA001	01A-A1 Top Card Connectors and Cables	FRU181
A1YCDE	TCC row Y across board positions C-E	AA000	01A-A1 Top Card Connectors and Cables	FRU193
A1ZFG	TCC row Z across board positions F-G	AA000	01A-A1 Top Card Connectors and Cables	FRU187
A2	Logic board	AA001 AA200	01A-A2 Logic Board	FRU140
A2A2	Logic board position A2	AA001	01A-A2 Logic Board	FRU140
A2C2W	Single wide TCC board position C2 row W	AA001 CA002 WA005/006	01A-A2 Top Card Cables	FRU170
A2C2W22	Single wide TCC board position C2 row W, pin 22	AA001 CA002 WA005/006	01A-A2 Top Card Cables	FRU170
A2Y2	Logic board connector Y2 at top of board	AA001	01A-A2 Top Card Cables	FRU140
A2Z2	Logic board connector Z2 at bottom of board	AA001	01A-A2 Top Card Cables	FRU140
Diskette Drive	Diskette drive	WZ001/002	Operator Set Up Panel	FRU086
Fans (Gate)	Gate fans	YF005	Fan Assembly 1 Fan Assembly 2	FRU150 FRU151
L/R	Local/remote power panel	YF020	Operator Set Up Panel	FRU084
-J1	Connector	YF020	Operator Set Up Panel	
-J2	Connector	YF020	Operator Set Up Panel	
Local Power Enable	Local power enable	YF020	Operator Set Up Panel	
MD Connector	CU connector for MD attachment	WX001	MD Connector	FRU169
OP	Operator panel		Operator Set Up Panel	FRU142
-J1/J2	Connector	WZ106		
-J2/P2	Connector	WZ106		
-J5	Connector	YF015 WZ106	Operator Set Up Panel	FRU142
-Power On-Indicator	Power on indicator	YF015	Operator Set Up Panel	FRU142
-(Sub) System Power Switch	(Sub) system power switch	YF015	Operator Set Up Panel	FRU142
-UEPO Switch	UEPO switch	YF015	Operator Set Up Panel	FRU198

Control Unit Location Area Definitions (Continued)

LOGIC LOCATION AREA IDENTIFIER	DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
OSU	Operator (controller) setup panel		Operator Set Up Panel	FRU141
-"A" Channel Type (Mode) Switch	Channel type (mode) switch	WZ102	Operator Set Up Panel	FRU141
-"B" Channel Type (Mode) Switch	Channel type (mode) switch	WZ102	Operator Set Up Panel	FRU141
-"C" Channel Type (Mode) Switch	Channel type (mode) switch	WZ104	Operator Set Up Panel	FRU141
-Channel A Disable Indicator	Channel disable indicator	YF010 (Sheet 1)	Operator Set Up Panel	FRU141
-Channel A Enable/ Disable Switch	Channel enable/disable switch	YF010 (Sheet 2)	Operator Set Up Panel	FRU141
-Channel B Disable Indicator	Channel disable indicator	YF010 (Sheet 1)	Operator Set Up Panel	FRU141
-Channel B Enable/ Disable Switch	Channel enable/disable switch	YF010 (Sheet 2)	Operator Set Up Panel	FRU141
-Channel C Disable Indicator	Channel disable indicator	YF010 (Sheet 1)	Operator Set Up Panel	FRU141
-Channel C Enable/ Disable Switch	Channel enable/disable switch	YF010 (Sheet 2)	Operator Set Up Panel	FRU141
-Channel D Disable Indicator	Channel disable indicator	YF010 (Sheet 1)	Operator Set Up Panel	FRU141
-Channel D Enable/ Disable Switch	Channel enable/disable switch	YF010 (Sheet 2)	Operator Set Up Panel	FRU141
-CUO/CU1 Switch	CUO/CU1 switch	YF010	Operator Set Up Panel	FRU197
-CU "A" Address Switch	Channel address switch	WZ102	Operator Set Up Panel	FRU197
-CU "B" Address Switch	Channel address switch	WZ102	Operator Set Up Panel	FRU197
-CU "C" Address Switch	Channel address switch	WZ104	Operator Set Up Panel	FRU197
-CU "D" Address Switch	Channel address switch	WZ104	Operator Set Up Panel	FRU197
-CU Error Indicator	CU error indicator	YF010	Operator Set Up Panel	FRU141
-CU Online Switch	CU online switch	YF010	Operator Set Up Panel	FRU141
-CU Waiting Indicator	CU wait indicator	YF010	Operator Set Up Panel	FRU141
-"D" Channel Type (Mode) Switch	Channel type (mode) switch	WZ104	Operator Set Up Panel	FRU141
-DC Power On Indicator	DC power on indicator	YF010	Operator Set Up Panel	FRU141
-IML/Power On Reset Switch	IML/power on reset switch	YF010	Operator Set Up Panel	FRU141
-J1/P1	Connector	WZ106 YF010 (Sheets 1 and 2)	Operator Set Up Panel	FRU141
-J2/P2	Connector	WZ106 YF010 (Sheets 1 and 2)	Operator Set Up Panel	FRU141
-J3/P3	Connector	YF010 (Sheet 2)	Operator Set Up Panel	FRU141
-J4/P4	Connector	YF010 (Sheet 2)	Operator Set Up Panel	FRU141
-J5/P5	Connector for thermal jumper	YF010 (Sheet 2)	Operator Set Up Panel	FRU141

Control Unit Location Area Definitions (Continued)

LOGIC LOCATION AREA IDENTIFIER	DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
-Local Power Enable Switch	Local power enable switch	YF010	Operator Set Up Panel	FRU141
-Offline Indicator	Offline indicator	YF010	Operator Set Up Panel	FRU141
-Test/ Normal Switch	Test/Normal switch	YF010	Operator Set Up Panel	FRU141
P1	Cable panel		CU-P1 Read/Write Bus Connectors	FRU150
-A1	Connector	WT004 WT006 WW020	CU-P1 Read/Write Bus Connectors	FRU150
-A2	Connector	WT001 WW010	CU-P1 Read/Write Bus Connectors	FRU150
-B1	Connector	WW020	CU-P1 Read/Write Bus Connectors	FRU150
-B2	Connector	WW010	CU-P1 Read/Write Bus Connectors	FRU150
-J1	Thermal connector	YF015	CU-P1 Read/Write Bus Connectors	FRU150
P2	Cable panel		CU-P2 Cable Connectors (Dual Control Unit Communication Connectors)	FRU150
-A1	Connector	WW020	CU-P2 Cable Connectors (Dual Control Unit Communication Connectors)	FRU150
-A2	Connector	WT008 WT010 WW020	CU-P2 Cable Connectors (Dual Control Unit Communication Connectors)	FRU150
-A3	Connector	WK005 WW010	CU-P2 Cable Connectors (Dual Control Unit Communication Connectors)	FRU150
-A4	Connector	WK001 WK003 WK005 WW010	CU-P2 Cable Connectors (Dual Control Unit Communication Connectors)	FRU150
-A5	Connector	WK006 WT003 WW010	CU-P2 Cable Connectors (Dual Control Unit Communication Connectors)	FRU150
PS-01	Power supply	YF001 YF003	CU-PS01 (two different types)	FRU144
-CB1	Circuit breaker	YF001 YF003	CU-PS01 (two different types)	FRU144
-CB2	Circuit breaker	YF001 YF003	CU-PS01 (two different types)	FRU144
-CB3	Circuit breaker	YF001 YF003	CU-PS01 (two different types)	FRU144
-F1	Fuse	YF001 YF003	CU-PS01 (two different types)	FRU144
-J1-J4B	Connectors	YF001 YF003	CU-PS01 (two different types)	FRU144
-J9-J10	Connectors	YF001 YF003	CU-PS01 (two different types)	FRU144
-J11	Connector	YF001	CU-PS01 (two different types)	FRU144
-J13-J15	Connectors	YF003	CU-PS01 (two different types)	FRU144
PS-02	Power supply	YF002	CU-PS02	FRU145
-CB1	Circuit breaker	YF002	CU-PS02	FRU145
-CB2	Circuit breaker	YF002	CU-PS02	FRU145
-CB3	Circuit breaker	YF002	CU-PS02	FRU145
-F1	Fuse		CU-PS02	FRU147
-F2	Fuse	YF002	CU-PS02	FRU148
-J1-J20	Connectors	YF002	CU-PS02	FRU145
-K1	Relay	YF002	CU-PS02	FRU145
T1	Tailgate	AA002 AT100	I/O Tailgate Connector	FRU136, 137 233-238
T1A1	Tailgate position A1	AA002 IB001 IB002 IB003	I/O Tailgate Connector	FRU136, 137 233-238
T1A3Y	Tag shoe card connector y	IT003 WA004	I/O Tailgate Connector	FRU137, 234, 236, 238

Control Unit Location Area Definitions (Continued)

LOGIC LOCATION AREA IDENTIFIER	DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
T1A3Z	Tag shoe card connector z	1T003 WA005/006	I/O Tailgate Connector	FRU170
TB1	Terminal block	ZT010	CU-A1 Logic Gate (hinge side)	FRU160
TB2	Terminal block	ZT011	CU-A1 Logic Gate (hinge side)	FRU160
TB3	Terminal block	ZT011	CU-A1 Logic Gate (hinge side)	FRU160
Thermal Switch (Top of gate)	Thermal switch	ZT020	Thermal Switch Assembly	FRU224
Thermal Switch (Bottom of gate)	Thermal switch	YF015	Thermal Switch Assembly	FRU143

Tape Unit and Drive Location Area Definitions

LOGIC LOCATION AREA IDENTIFIER	DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
A1	Logic board in each drive in the tape unit	AA000 AA100	02A-A1 Logic Board Pin and Card Side	FRU058
CB1	Circuit breaker (primary power)	YF050 YF060	Tape Unit AC Power CB	FRU218
Compressor	Compressor	YF050 YF060	Major FRU Locations 50/60 Hz	FRU030
DC Switch	DC switch (these are additional contacts on the drive fan and power switch)	SN001/002 (Sheet 2)	Tape Unit Locations	FRU104
-P1	Plug	SN001/002 (Sheet 2)		FRU104
DK	Deck assembly		Drive Locations	
-Cartridge Latched Sensor and LED	Cartridge latched sensor and LED	SN001/002 (Sheet 1)	Cartridge Latch Assembly	FRU011
-Cartridge Present Sensor and LED	Cartridge present sensor and LED	SN001/002 (Sheet 1)	Cartridge Present Sensor	FRU010
-File Reel Tach	File reel tachometer	SN001/002 (Sheet 2)	File Reel Motor	FRU003
-FPSW	Deck assembly file protect switch	SN001/002 (Sheet 2)	File Protect Switch	FRU009
-J14	Connector for tension transducer	PA000/001 (Sheet 2)	Tension Transducer	FRU014
-Machine Reel Tach Phase A Sensor and LED	Machine reel tachometer phase A sensor and LED	SN001/002 (Sheet 1)	Machine Reel Tach Sensor A	FRU225
-Machine Reel Phase B Sensor and LED	Machine reel tachometer phase B sensor and LED	SN001/001 (Sheet 1)	Machine Reel Tach Sensor B	FRU226
-P1	Connector for tape path sensor A	SN001/002 (Sheet 1)	Tape Path Sensor A	FRU006
-P2	Connector for tape path sensor B	SN001/002 (Sheet 1)	Tape Path Sensor B	FRU007
-P3	Connector for cartridge present sensor and file protect switch	SN001/002 (Sheet 1 and 2)	Cartridge Present Sensor and File Protect Switch	FRU010
-P4	Connector for cartridge latched sensor	SN001/002 (Sheet 1)	Cartridge Latch Assembly	FRU011
-P5	Connector for machine reel tach phase B sensor	SN001/002 (Sheet 1)	Machine Reel Tach Sensor B	FRU226
-P6	Connector for machine reel tach phase A sensor	SN001/002 (Sheet 1)	Machine Reel Tach Sensor A	FRU225
-P7	Connector for file reel tach	SN001/002 (Sheet 2)	File Reel Motor	FRU003
-Plenum Press Sw	Plenum pressure sensor switch	SN001/002 (Sheet 2)	Plenum Assembly and Pressure Switch	FRU040
-Tape Path Sensor A and LED	Tape path sensor A and LED	SN001/002 (Sheet 1)	Tape Path Sensor A	FRU006
-Tape Path Sensor B And LED	Tape path sensor B and LED	SN001/002 (Sheet 1)	Tape Path Sensor B	FRU007
-Tray Solenoid	Cartridge latch solenoid	YG010 YG110	Latch Sensor	FRU002
Drive Fan and Power Switch	Drive fan and power switch	YF020	Tape Unit Locations	FRU104
DSP	Message display		Operator Control and Display	FRU021
-J1	Connector	WD000 WD001		
-J2	Connector	WD000 WD001		
-J3	Connector	WD000 WD001		
-J4	Connector	WD000 WD001		
-Ready Switch	Switch	WD000 WD001	Ready/Not Ready Switch	FRU109

Tape Unit and Drive Location Area Definitions (Continued)

LOGIC LOCATION AREA IDENTIFIER	DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
-Rewind Switch	Switch	WD000 WD001	Rewind Switch	FRU109
-Unload Switch	Switch	WD000 WD001	Unload Switch	FRU109
EL	External load register panel	WD000 WD001	Major FRU Locations 50/60 Hz (-5 V dc Resister panel)	FRU036
Fan	Fan (located near the compressor in the tape unit for 50 Hz)(fan is located at the bottom of the tape unit frame for 60 Hz)	YF050 YF060	Major FRU Locations 50/60 Hz	FRU071
Fan	Fan for drive gate	YG010 (drive 0) YG110 (drive 1)	50/60 Hz Blower Assembly	FRU020
File Reel Motor	File reel motor	YG010 (drive 0) YG110 (drive 1)	File Reel Motor	FRU003
Head (Tape Lifter) Solenoid	Solenoid at the head to move tape away from the head during high-speed tape movement (tape lifter)	YG010 (drive 0) YG110 (drive 1)	Tape Lifter Solenoid	FRU216
Local	Local read/write and control DDB cabling CU/TU CU0 local drive address 0-7 CU1 local drive address 8-F	VP001 WW010 WW020 ZW101 ZW102 ZW103	Read Adapter Cables and Write Adapter Cables	FRU087-089 FRU091-093
Machine Reel Motor	Machine reel motor	YG010 (drive 0) YG110 (drive 1)	Machine Reel Motor	FRU004
Online/ Offline Switch	Online/offline switch	SN001/002 (Sheet 2)	Tape Unit Locations	FRU105
OSU	Operator set up panel for drive address switches	SN001/002 (Sheet 2)	Tape Unit Locations	FRU108
-Drive Logical Address Switch	Drive logical address switch	SN001/002 (Sheet 2)	Tape Unit Locations	FRU108
-J1	Connector for drive logical address switch	SN001/002 (Sheet 2)	Tape Unit Locations	FRU108
P1	Cable panel		50/60 Hz TU-D0/1-P1	
-J/P1	Connector for PS1 voltage distribution	ZZ010 ZZ020 ZZ110 ZZ120	50/60 Hz TU-D0/1-P1	
-J/P2	Connector for PS1 voltage distribution	ZZ010 ZZ020 ZZ110 ZZ120	50/60 Hz TU-D0/1-P1	
-J3	Connector for drive fan and power switch	YF020	50/60 Hz TU-D0/1-P1	
-J4	Connector to drive logical address switch connector OSU-J1	SN001/002 (Sheet 2)	50/60 Hz TU-D0/1-P1	
-P1	Plug to message display card	WD000	50/60 Hz TU-D0/1-P1	
-RA1	Connector for read bus local	VP001 WW020	50/60 Hz TU-D0/1-P1	FRU087-089
-RB1	Connector for read bus remote	VP002 WW020	50/60 Hz TU-D0/1-P1	FRU091-093
-WA1	Connector for write bus local	WW010 ZW101 ZW102	50/60 Hz TU-D0/1-P1	FRU087-089
-WA2	Connector for write bus local	WW010 ZW102 ZW102	50/60 Hz TU-D0/1-P1	FRU087-089
-WB1	Connector for write bus remote	WW010 ZW202	50/60 Hz TU-D0/1-P1	FRU091-093
-WB2	Connector for write bus remote	WW010 ZW201 ZW202 ZW203	50/60 Hz TU-D0/1-P1	FRU091-093

Tape Unit and Drive Location Area Definitions (Continued)

LOGIC LOCATION AREA IDENTIFIER	DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
P2	Read/write DDB cable connector panel between tape units		TU-P2 Read/Write Bus Connectors	FRU199, 248, 264, 265
-J1	Thermal connector	SN001/002 (Sheet 2)	Tape Unit Locations	
-A1	Connector for read bus local	WW020	TU-P2 Read/Write Bus Connectors	FRU087-089
-B1	Connector for read bus remote	WW020	TU-P2 Read/Write Bus Connectors	FRU087-089
-WA1	Connector for write bus local	WW010 ZW103	TU-P2 Read/Write Bus Connectors	FRU087-089
-WB1	Connector for write bus remote	WW010 ZW203	TU-P2 Read/Write Bus Connectors	FRU087-089
PA	Power amplifier	PA000/001	TU-D0/1-PA Power Amplifier Board	FRU059
-J1	Connector	PA000/001 (Sheet 1)	TU-D0/1-PA Power Amplifier Board	
-J2, J3	Connectors	PA000/001 (Sheet 2)	TU-D0/1-PA Power Amplifier Board	
-J4-J8, J11	Connectors	PA000/001 (Sheet 3)	TU-D0/1-PA Power Amplifier Board	
PASW	Physical address switch	SN001/002 (Sheet 1)	Physical Address Switch	FRU129
Power On Reset Switch	Power on reset switch	SN001/002 (Sheet 2)	Tape Unit Locations	FRU107
PS	Tape unit power supply 1	YF100	Tape Unit DC Power Supply (two different types)	FRU095
PS1	Tape unit power supply 1	YF100	Tape Unit DC Power Supply (two different types)	FRU095
PS-01	Tape unit power supply 1	YF100	Tape Unit DC Power Supply (two different types)	FRU095
-CB1	Circuit breaker	YF100	Tape Unit DC Power Supply (two different types)	FRU095
-CB2	Circuit breaker	YF100	Tape Unit DC Power Supply (two different types)	FRU095
-F1-F13	Fuses	YF100	Tape Unit DC Power Supply (two different types)	FRU095
-P/J1 to P/J16	Connectors	YF100	Tape Unit DC Power Supply (two different types)	FRU095
Remote	Remote read, write, and control DDB cables CU/TU CU0 remote drive address 8-F CU1 remote drive address 0-7	VP002 WW010 WW020 ZW201 ZW202 ZW203	Read Adapter Cables and Write Adapter Cables	FRU087-089 FRU091-093
Tape Lifter Solenoid (Head)	Solenoid at the head to move tape away from the head during high-speed tape movement (tape lifter)	YG010 YG110	Tape Lifter Solenoid	FRU216
TB1	Terminal block	YF050 YF060	TB1	FRU075, 076
Tension Transducer Assembly	Tension transducer assembly	ZT030	Tension Transducer	FRU014
Terminator (See note 1 on WW020)	Write bus terminator	WW010	TU-P2 Read/Write Bus Connectors	FRU199, 248, 264, 265
Thermal Switch	Thermal switch in D0/1 logic gates	SN001/002 (Sheet 2)	Thermal Switch Assembly	FRU110
Thermal Switch S-2	Thermal switch	SN001/002 (Sheet 2)	Tape Unit Locations	FRU082
Thread Motor	Thread motor	YG010 (drive 0) YG110 (drive 1)	Threader Motor	FRU001

Legend

Tape Unit and Drive Location Area Definitions

Automatic Cartridge Loaders

DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
Load Assembly		Load Locations	
Cartridge Latched Sensor and LED	SN001/002 (Sheet 1)	Cartridge Latch Assembly	FRU011
Cartridge Present Sensor and LED	SN001/002 (Sheet 1)	Cartridge Present Sensor	FRU010
Feed Complete Sensor (Hall Effect Switch)	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU282
Load Assembly File Protect Switch	SN001/002 (Sheet 2)	File Protect Switch	FRU009
Connector for Cartridge Present Sensor	SN001/002 (Sheet 1)	Cartridge Present Sensor	FRU010
Connector for File Protect Switch	SN001/002 (Sheet 2)	File Protect Switch	FRU009
Connector for Load Motor Complete Sensor	SN003 (Sheet 2)	Automatic Cartridge Loader Feature	FRU284
Connector for Cartridge Latched	SN001/002 (Sheet 1)	Cartridge Latch Assembly	FRU011
Connector for Feed Complete Sensor	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU282
Load Motor	YG120	Automatic Cartridge Loader Feature	FRU283
Load Motor Complete Sensor And LED	SN003 (Sheet 2)	Automatic Cartridge Loader Feature	FRU284
Load Motor	YG120	Automatic Cartridge Loader Feature	FRU283
Loader Control Card	AL001, 002, 003	Automatic Cartridge Loader Feature	FRU281
Loader Control Card Connectors		Automatic Cartridge Loader Feature	FRU281
Connector to Signal Cable from Drive	AL001, 002, 003	Automatic Cartridge Loader Feature	FRU281
Connector to Loader Sensors	AL001, 002, 003	Automatic Cartridge Loader Feature	FRU281
Connector to Voltage Cable from Drive	AL001, 002, 003	Automatic Cartridge Loader Feature	FRU281
Connector to Loader Motors and Solenoid	AL001, 002, 003	Automatic Cartridge Loader Feature	FRU281
Connector to Loader Operator Panel	AL001, 002, 003	Automatic Cartridge Loader Feature	FRU281
Loader Mechanical Assembly		Loader Mechanical Locations	FRU285
Loader +5 V.DC	ZZ020/120	Automatic Cartridge Loader Feature	FRU299
Loader +24 V.DC	ZZ020/120	Automatic Cartridge Loader Feature	FRU288
Signal Cable Connector to Drive	ZX004	Automatic Cartridge Loader Feature	FRU286
Power Cable Connector to Drive	ZZ020/120	Automatic Cartridge Loader Feature	FRU287

Tape Unit and Drive Location Area Definitions

Automatic Cartridge Loaders

DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
Loader Operator Panel-Attention and Power LED, Mode and Start Switches	AL002	Automatic Cartridge Loader Feature	FRU298
Loader Operator Panel	AL002	Automatic Cartridge Loader Feature	FRU298
Attention LED on Operator Panel	AL002	Automatic Cartridge Loader Feature	FRU298
Power LED on Operator Panel	AL002	Automatic Cartridge Loader Feature	FRU298
Start Switch on Operator Panel	AL002	Automatic Cartridge Loader Feature	FRU298
Input Stack Assembly		Automatic Cartridge Loader Feature	FRU290
Cartridge in Stick Sensor and LED	SN003 (Sheet 2)	Automatic Cartridge Loader Feature	FRU291
Cartridge Staged Sensor and LED	SN003 (Sheet 1)	Automatic Cartridg Loader Feature	FRU292
Input Complete Sensor and LED	SN003 (Sheet 2)	Automatic Cartridge Loader Feature	FRU293
Input Motor	YG120	Automatic Cartridge Loader Feature	FRU290
Connector for Cartridge in Stack Sensor	SN003 (Sheet 2)	Automatic Cartridge Loader Feature	FRU291
Connector for Input Motor	YG120	Automatic Cartridge Loader Feature	FRU290
Connector for Input Complete Sensor	SN003 (Sheet 2)	Automatic Cartridge Loader Feature	FRU293
Connector for Cartridge Staged Sensor	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU292
Left Input Rail Assembly		Automatic Cartridge Loader Feature	FRU293
Right Input Rail Assembly		Automatic Cartridge Loader Feature	FRU294
Feed Assembly		Automatic Cartridge Loader Feature	FRU295
Extract Complete Sensor and LED	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU295
Feeder Motor Left	YG120	Automatic Cartridge Loader Feature	FRU295
Feeder Motor Right	YG120	Automatic Cartridge Loader Feature	FRU295
Feeder Solenoid	YG120	Automatic Cartridge Loader Feature	FRU295
Connector for Feeder Motor Left	YG120	Automatic Cartridge Loader Feature	FRU295
Connector for Feeder Solenoid	YG120	Automatic Cartridge Loader Feature	FRU295
Connector for Feeder Motor Right	YG120	Automatic Cartridge Loader Feature	FRU295
Connector for Tracks Feed Sensor	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU295
Connector for Tracks Closed Sensor	SN003	Automatic Cartridge Loader Feature	FRU295

Legend LGND 47

Legend

Tape Unit and Drive Location Area Definitions

Automatic Cartridge Loaders

DESCRIPTION	LOGIC PAGE	LOC 1 TABLE OF CONTENTS REFERENCE	CARR 1 TABLE OF CONTENTS REFERENCE
Connector for Extract Complete Sensor	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU295
Track Closed Sensor and LED	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU295
Track Feed Sensor and LED	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU295
Output Stack Assembly		Automatic Cartridge Loader Feature	FRU297
Output Motor	YG120	Automatic Cartridge Loader Feature	FRU297
Connector for Output Motor	YG120	Automatic Cartridge Loader Feature	FRU297
Stack Up Position Sensor and LED	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU296
Connector for Stack Up Position Sensor	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU296
Stack Low Position Sensor and LED	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU89
Connector for Stack Low Position Sensor	SN003 (Sheet 1)	Automatic Cartridge Loader Feature	FRU289

Legend

Error Analysis Diagram (EAD) Logic Blocks

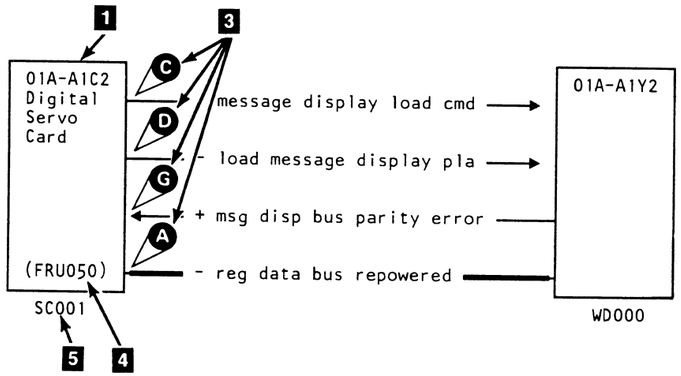
EADs are block diagrams which show the logical functions relating to the error code.

The error analysis logic blocks contain the following information:

- Physical card location 1
- Card name 2
- Test points 3
- FRU number 4
- Logic diagram 5

  Note: The actual logic diagram references must be used when performing scoping or probing procedures.

- Signal lines and buses that pertain to the error condition



Logic Diagrams

Logic diagrams show the input and output connectors of each card.

Card Location Chart

Card Location Charts for each board are included at the start of the logic diagrams. The charts identify the cards and cables that plug into the board, their names, and the location of plug information and reference pages (input and output connector logic diagrams). Crossover connectors and their part numbers are also shown.

Card Plug List

Card Plug Lists **3** are provided for each card in the subsystem. They contain information such as the card function, location, and logic diagram page numbers. Part, EC, and REA numbers for the primary and alternate cards are also listed. The comments area provides information about an alternate card.

For example, an EAD indicates that inputs and outputs from the Write Data Flow card 01A-A1P2 had to be scoped. The 'P' card position **1** on the chart shows that the card input and output connectors can be found on logic pages DF001 and DF002 **2**. This information can also be found on the Card Plug List.

To expand on the example, suppose the EAD also indicates that the card output to be scoped was the MUX WRITE DATA and the inputs were the BF/WD CLOCK S2-S3 and WDF DATA.

The "Sample Logic Diagrams" on LGND 15 show that the 'MUX WRITE DAT' line **8** is found on logic page DF002 **9** and that it can be scoped at the Top Card Connector pins (identified by TCC **7** following the card label). The inputs ('BF/WD CLOCK' line **5** and 'WDF DATA' line **6** are found on logic page DF001 **11** and can be scoped at the Bottom Card Connector pins (BCC) on the same card **10** and **12**. The connector is identified by the (BCC) **4** following the card label.

Note: BCC pins are the same as the pins on the back of the board.

Multiple Logic Diagrams for One Card

Logic pages are not true functional representations of logic cards. They only represent the input and output connectors to the cards.

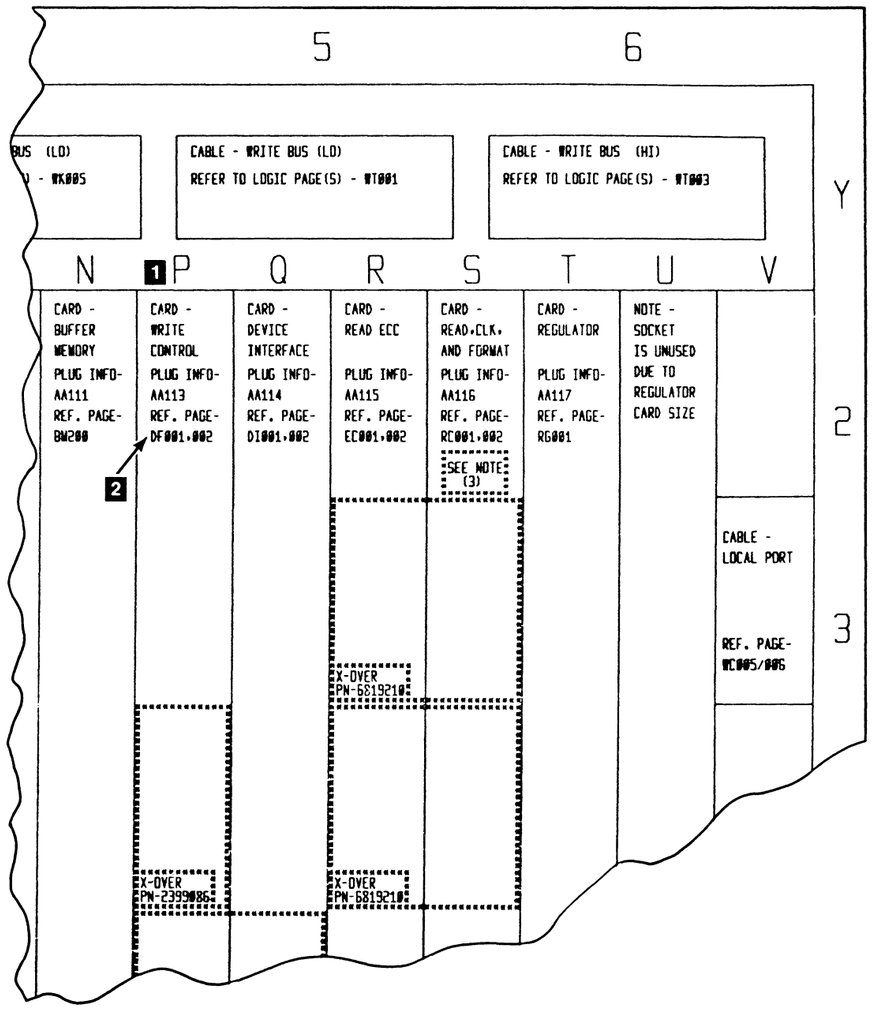
A card can have three types of connectors:

- Bottom Card Connector (BCC)
- Middle Card Connector (MCC)
- Top Card Connector (TCC)

Only one type of connecter is shown on each logic diagram; therefore, one card may be shown on up to three separate diagrams. To determine the number of logic diagrams for a card, see the card plug list.

Note: The relationship between the input and output card connector pins cannot be determined from the logic diagrams. When required, these relationships are defined in the Error Analysis Diagram (EAD) section by error code.

Card Location Chart



3 *Card Plug List*

FUNCTION – CHANNEL ADAPTER
LOCATION – 1A-A2C2

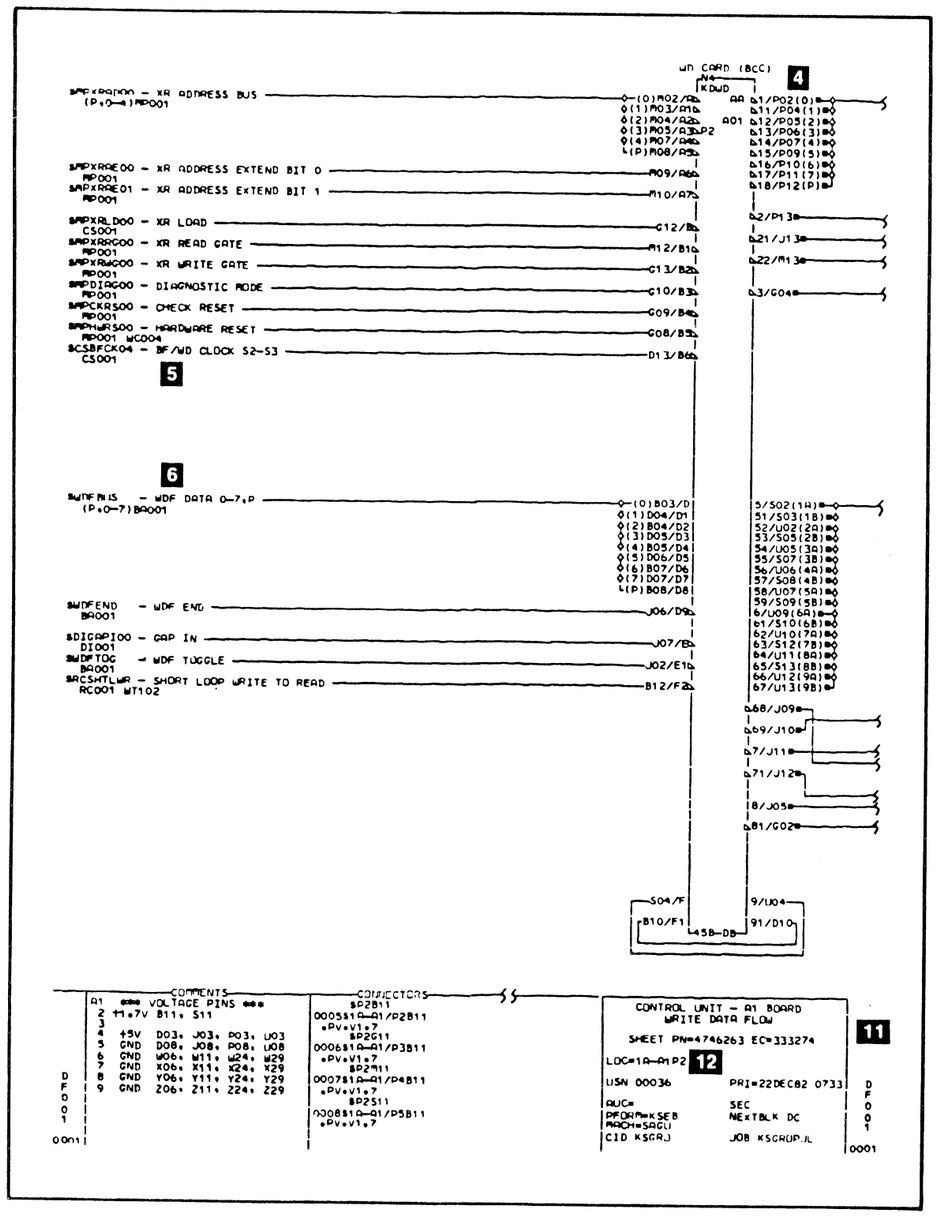
LOGIC SHEETS – CA001, CA002

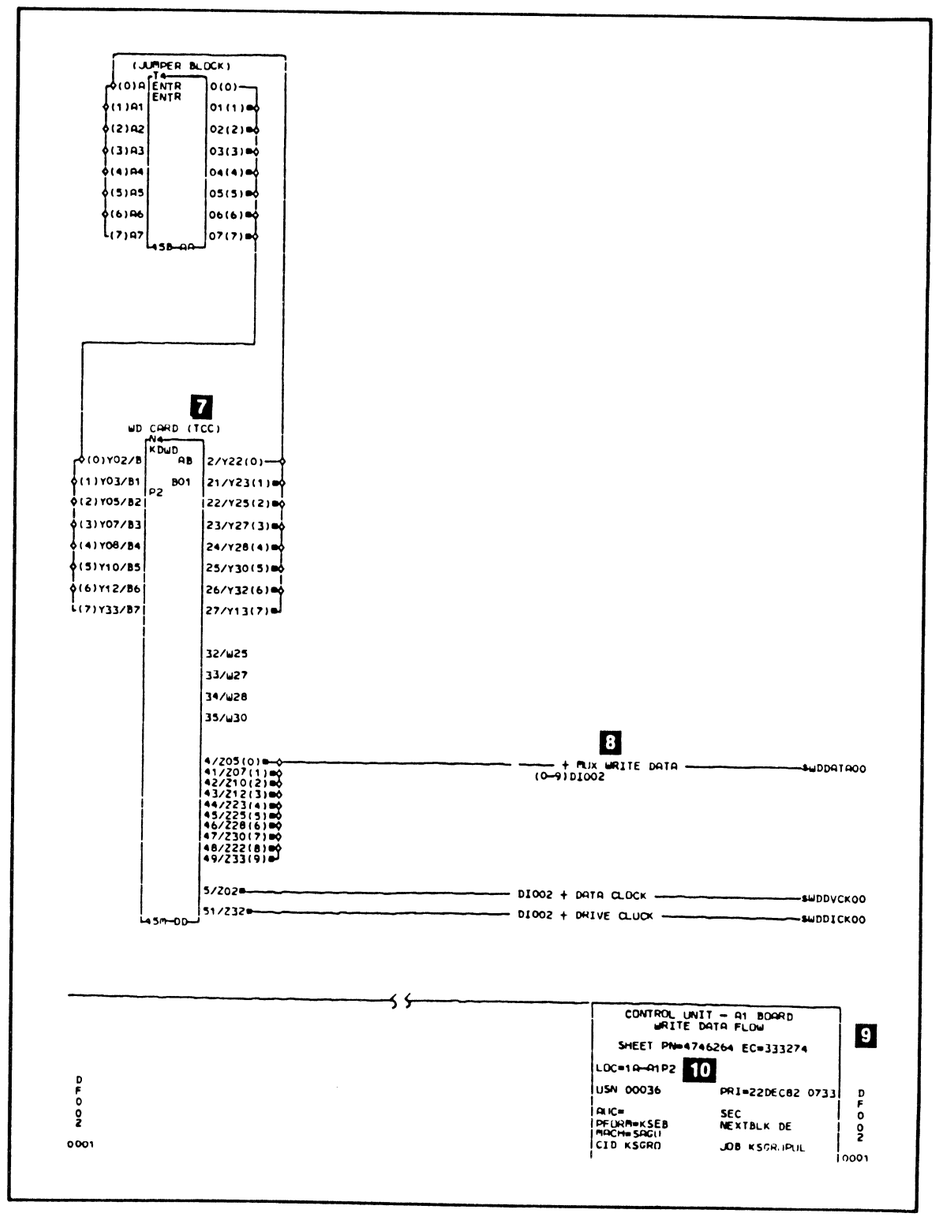
	PRIMARY	ALTERNATE
PNAME	KUCA	
PART NUMBER	6050663	
EC NUMBER	9916829	
REA NUMBER		

COMMENTS –
30E-AA

Logic Diagrams (Continued)

Sample Logic Diagrams





Legend

Logic Diagrams (Continued)

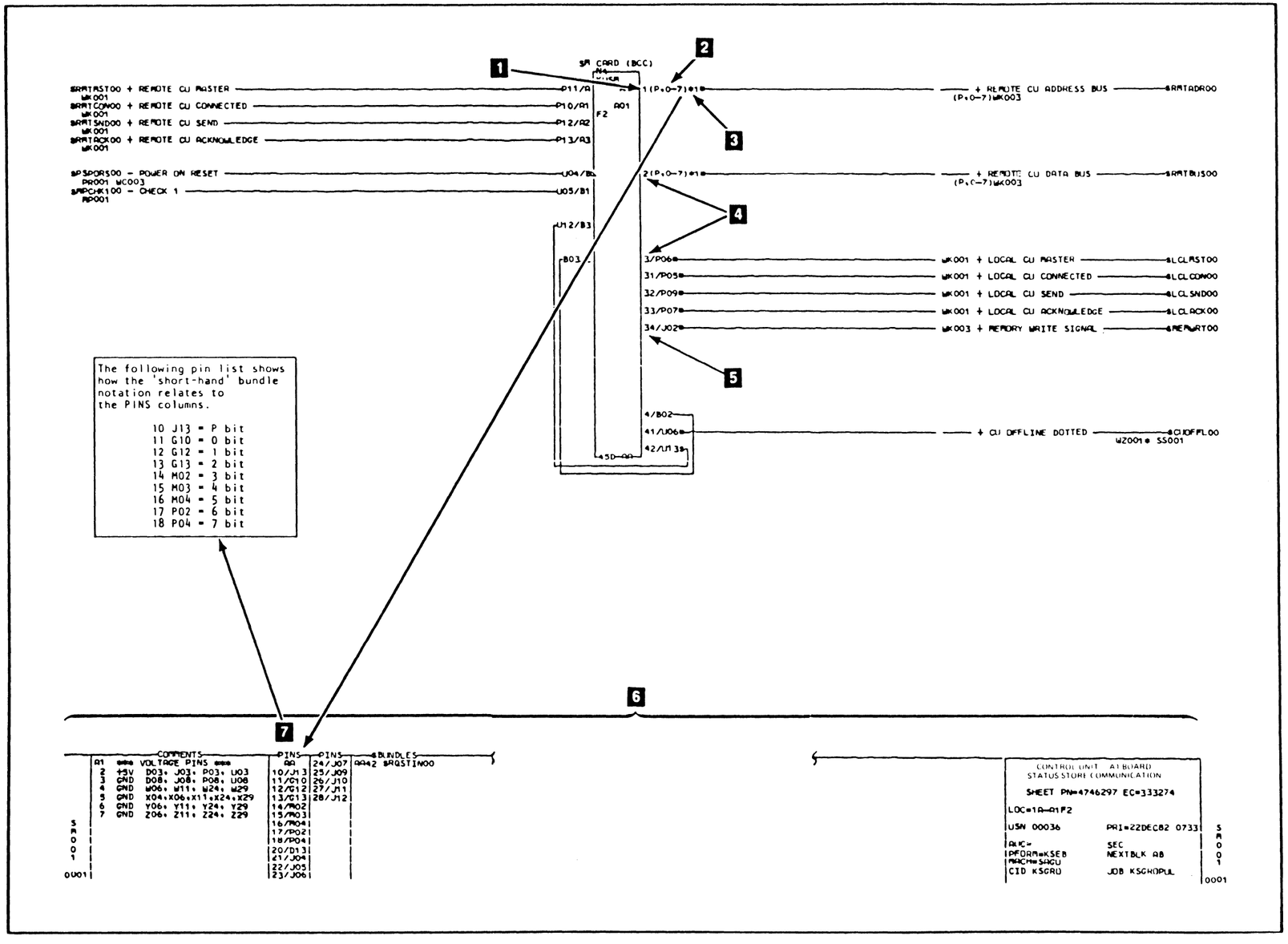
Bundled Lines

Bundled lines combine the bit lines in a bus and represent the bus as a single line. The bit lines in the bundle are identified by a 'short-hand' notation. The (P,0-7) **2** indicates that a parity bit and bits 0 through 7 are included in the REMOTE CU ADDRESS BUS. An asterisk (*) **3** following the 'short-hand' notation (P,0-7) indicates that the bit lines are defined in the information area **6** at the bottom of the logic diagram.

The PINS columns **7** in the information area define the pins for each bundle on the diagram. Pins 10/J13 through 18/P04 represent the pins contained in the REMOTE CU ADDRESS BUS bundle **2**. The parity bit is on pin 10/J13 (low order zeros do not appear on the diagram for logical pins **1** and **4**) and the 7 bit is on pin 18/P04.

Logical/Physical Pins

Pins are identified by logical pin notation and pin number **5**. J02 is the physical pin. The 34 is a logical pin notation and is used for engineering purposes only. Low order zeros are not used for logical pin notation. For example, logical pin 10 = 1, 20 = 2 **1** and **4**, and so on.



Legend

Logic Diagrams (Continued)

Logic diagrams show the input and output pins of each card.

Dot OR's of Output Lines

The '- LOCAL BUFFER SERVICE OUT' lines on logic diagram pages CA001 1, CA101 2, CA201 3, and CA301 4 appear to be output lines exiting the logic page and going to another page. However, instead of being inputs to other logic pages, the lines are all outputs that are "Dot-OR'ed" together.

To differentiate between a driver (source) and receiver (sink) for non-directional (BI-DI) lines on the right side of a logic diagram:

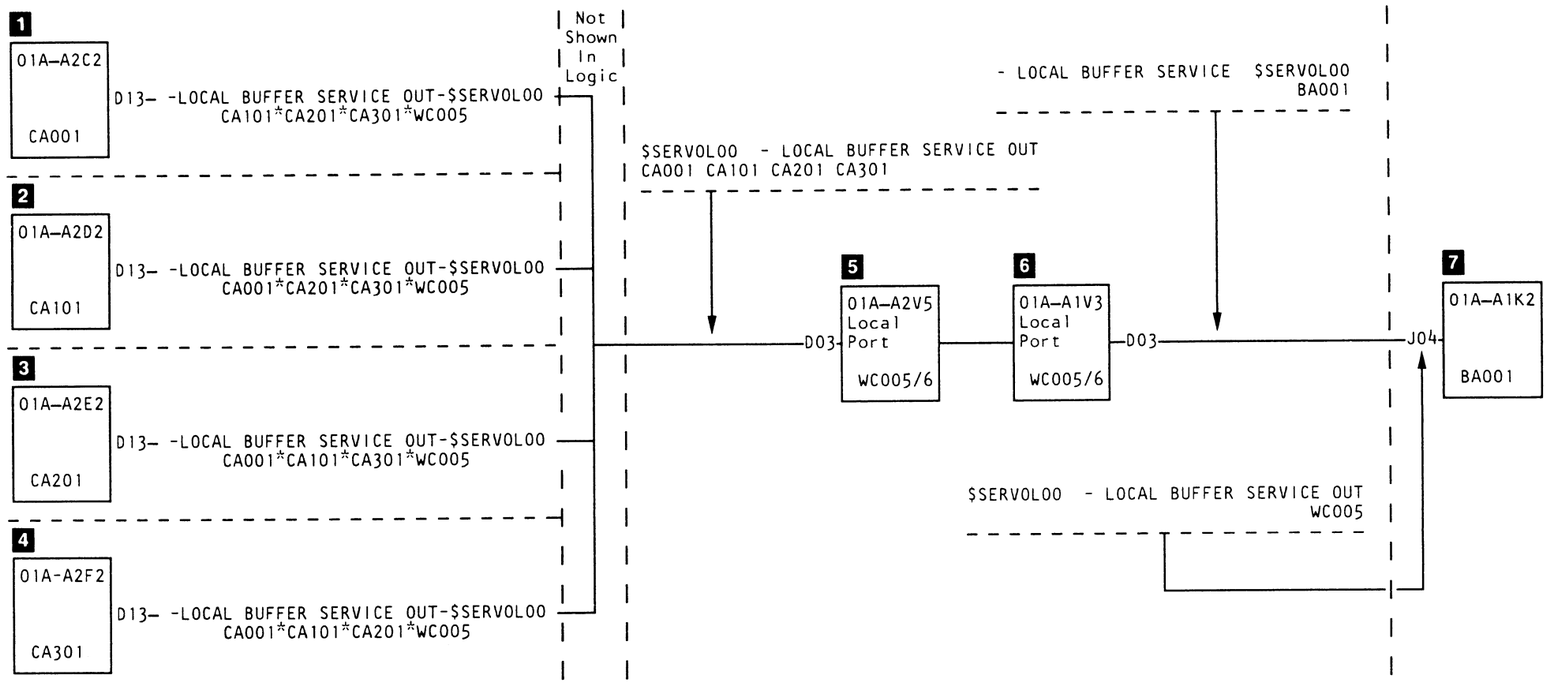
1. All logic diagram page references, except those beginning with "W" (WA001, WC006), that are followed by an asterisk (*) are other driver logic diagram pages for the receiver.

2. All logic diagram page references, except those beginning with a "W" that are not followed by an asterisk are the receiver logic diagram pages from the driver.

In this diagram the logic represents a wire-to-wire path, not a logical flow path. The only output from the four CA cards is to logic page BA001 7. The drive logics are on CA pages 1 - 4, WC005/6 5 6, and the receiver card on BA001 7.

Test Points

Some logic card outputs are test points and connect only as far as indicated in the logics. These lines are represented by having a "TP" or "T.P." in the line name.



Legend

Field Wire Net Lists

The Field Wire Nets Lists, show the following for the 01A-A1 and 01A-A2 boards:

- Pin to Net List
- Net to Pin List
- Voltage Distribution List

Pin to Net List

To determine which net contains a specific pin:

1. Find the pin number in the PIN column **1**.
2. The column to the right of the pin number is the NET column **2** that lists the net the pin is included in.
3. A 'V' to the left of the pin number **3** indicates that the pin is a voltage pin. Such a pin will also be referenced in the Voltage Distribution List.

Net to Pin List

To determine which pins are included in a net:

1. Find the net number in the ENG. NET NO. column **4**.
2. The two columns to the right of the net number, the FROM and TO columns **5**, contain a listing of the pins included in the net. They also indicate the order in which the pins are connected.

Voltage Distribution List

The Voltage Distribution List, references the voltage levels and the pins that are supplied by that specific voltage level. See the "Voltage Tolerance Tables" in the PWR section for the specific voltage level tolerance.

Note: The VOLTAGE column **6** shows the different voltages that are supplied to the boards. +08500 **7** means +8.5 Vdc, and so on.

Pin to Net List

DATE - 01/26/82 - FIELD WIRE NET LIST

PART NO. 0004741673

EC NO. 000991666A (41)

NODE NAME CR

	1 PIN	**2** NET	PIN	NET
	B3B13-	$CUBSEL00	B3B14-	$CUBBUS 01
	B3C11-	$CUBCKA00	B3C14-	$SCPARSTM
	B3D05-	$CUBCKA00	B3D06-	$CUBCKB00
	B3D10-	$IFBSTI00	B3D11-	$IFBRPI00
	B3E04-	$CUABUS 01	B3E05-	$CUBCKA00
	B3E10-	$CUBCKA00	B3E11-	$CATRPORM
	B4A05-	$CUBBUS 02	B4A06-	$CUBCKB00
	B4A10-	$SCLTCW00	B4A11-	$SCLTCW00
	B4B03-	$SNDADR01	B4B04-	$SNDADR02
	B4B13-	$IFBSEL00	B4B14-	$CUBSEL00
	B4C03-	$SNDADR01	B4C04-	$CUBCMD00
	B4D02-	$IFITLEVI01	B4D04-	$IFITLEVI02
	B4D07-	$MPXREG2901	B4D09-	$MPXREG2902
	B4D12-	$IFINTREQ	B4D13-	$IFWENB00
	B4E05-	$CUBBUS 02	B4E06-	$CUBBUS 03
	B5A06-	$CUBCKB00	B5A07-	$CUBGAP00
	B5B02-	$IFWRDATA00	B5B03-	$IFWRDATA01
	B5B07-	$IFWRDATA04	B5B08-	$IFWRDATA05
	B5B12-	$IFWRDATA08	B5B14-	$IFWRDATA07
	B5C05-	$IFASEL00	B5C06-	$SCXRDATA04
	B5C11-	$CAPORSTM	B5C12-	$IFWRDATA02
	B5D04-	$IFCLKB00	B5D05-	$IFASEL00
3 V	B5D08-	IF000BA10	B5D09-	IF000BA10
	B5D12-	IF000BA10	B5D13-	$IFRASDAT01
	B5E06-	$CUBBUS 03	B5E10-	$IFBIAS00
	B6A02-	$SWITCHM4	B6A03-	$SCLTCC00
	B6B02-	$SCRSETAM	B6B03-	$IFWRDA
V	B6C03-	PA001AAB2	B6C05-	
	B6E03-	$SCLTCC00	B6E05-	
	C1B10-	$SCLEDI04	C1B1	
	C1C13-	$SCXRDATA08		
	C1E14-	$SCXRDATA07		
	C2A05-	$SWITCHM6		
	C2B03-	$CAPA		

Voltage Distribution List

DATE - 01/26/82 - FIELD WIRE NET LIST

PART NO. 0004741673

EC NO. 000991666A (41)

VOLTAGE DISTRIBUTION LIST

6 VOLTAGE	PIN	PLANE	X	Y
.	G2D03	03	+01.0000	+04.2500
.	J2D03	03	+01.0000	+05.5000
.	J3A01	03	+02.5000	+05.1250
.	J3D03	03	+02.7500	+05.5000
.	J4A01	03	+04.2500	+05.1250
.	J4D03	03	+04.5000	+05.5000
.	J5A01	03	+06.0000	+05.1250
.	J5D03	03	+06.2500	+05.5000
.	K4D03	03	+04.5000	+06.1250
.	K5D03	03	+06.2500	+06.1250
7 +08500	B2A14	03	+02.3750	+00.7500
.	B3A14	03	+04.1250	+00.7500
.	B4A14	03	+05.8750	+00.7500
.	C2B11	03	+02.0000	+01.5000
.	D2B11	03	+02.0000	+02.1250
.	D3B11	03	+03.7500	+02.1250
.	D4B11	03	+05.5000	+02.1250
.	D5B11	03	+07.2500	+02.1250
.	E2B11	03	+02.0000	+02.7500
.	E3B11	03	+03.7500	+02.7500
.	E4B11	03	+05.5000	+02.7500
.	E5B11	03	+07.2500	+02.7500
.	F2B11	03	+02.0000	+03.3750
.	F3B11	03	+03.7500	+03.3750
.	F4B11	03	+05.5000	+03.3750
.	F5B11	03	+07.2500	+03.3750
.	J2A14	03	+02.3750	+05.1250
.	J2B11	03	+02.0000	+05.2500
.	J3A14	03	+04.1250	+05.1250
.	J4A14	03	+05.8750	
.	K5B11			
+10500	G2D04			

Net to Pin List

DATE - 01/26/82 - FIELD WIRE NET LIST -

PART NO. 0004741673

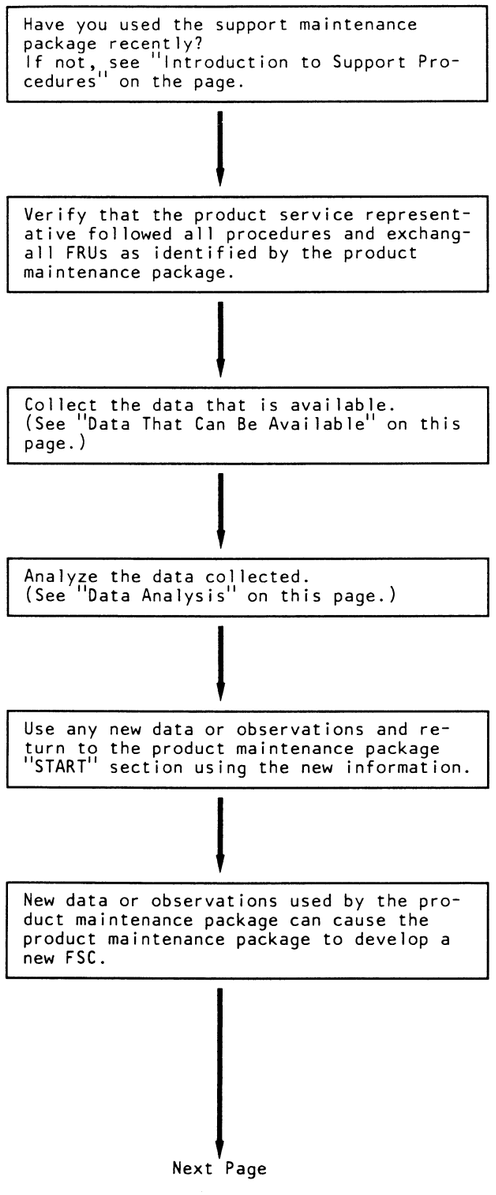
EC NO. 000991666A (41) LOCATION 1A-A

4 ENG. NET NO.	**5** FROM	TO	PL	WIR TYP	LENGTH
.	A3C10-	A4C09-	03		01.775
.	A4C09-	A4D09-	01		00.125
.	A4D09-	A4E09-	01		00.125
.	A4E09-	A5E09-	03		01.809
.	A5E09-	A5D09-	01		00.125
$IFBIAS00	K4B13-	K2B01-	03		05.100
.	K2B01-	J2D01-	01		00.484
.	J2D01-	J2D06-	03		00.734
.	J2D06-	J2E02-	03		00.625
.	J2E02-	G2C02-	01		01.709
.	G2C02-	G5A10-	03		06.500
.	G5A10-	B5E10-	01		02.775
.	B5E10-	B5E11-	03		00.125
.	B5E11-	B5D11-	01		00.125
$IFBRPI00	B3D11-	A3C12-	01		00.875
.	A3C12-	A4D11-	03		01.750
.	A4D11-	A5C11-	03		01.875
.	A5C11-	A5D11-	01		00.125
$IFBSEL00	J2D10-	J1D12-	03		01.650
.	J1D12-	E1D12-	01		02.650
.	E1D12-	E4C04-	03		04.684
.	E4C04-	D4E04-	01		00.484
.	D4E04-	D4E13-	03		01.275
.	D4E13-	B4B13-	01		01.775
$IFBSTI00	B3D10-	A3E11-	01		
.	A3E11-	A4D10-	03		
.	A4D10-	A5D10-			
$IFCLKB00	K4B10-				
.	G5A11-				
.	D5A11-				
.	D5A05-				
$IFDSEA00					
.					
.					
$IFINTREQ					

3480 MI EC A57723

Contents

Start



Next Page

Introduction to Support Procedures

The information in Volumes A04 and A05 of this maintenance information make up the support material for the 3480 Magnetic Tape Subsystem. Each of the tabs within these volumes represents a section of information that aids the service representative in problem determination and repair at the support level.

The support service representative should already be thoroughly familiar with the information in Volumes A04 and A05. In addition, the product service representative can, with aid, use this information in troubleshooting when the product maintenance package fails to isolate a subsystem problem.

Support Maintenance Package

The support maintenance package supplies the service representative with a support diskette and documentation that can be used to isolate difficult subsystem problems. The support diskette gives the service representative the ability to select and run specific diagnostics or utilities. The support documentation supplies maintenance information beyond the scope of MAPs and procedures used by the product service representative.

When to Use the Support Maintenance Package

Use the support maintenance package to correct failures that were not repaired using the product maintenance package. The following kinds of failures may require use of the support maintenance package.

- The FRUs identified by the product maintenance package were not exchanged, or procedures were not followed as directed by the product maintenance package.
- Power is missing or out of tolerance at the point of failure.
- Connections between FRUS (cables, connectors, top card connectors, or board wiring) have short circuits or open circuits.
- A FRU exchanged by the product service representative is defective.
- A design problem exists in the hardware, the microcode, or the maintenance package.
- No trouble was found.
- Failures occur during installation or after EC rework.

Transition From the Product Maintenance Package to the Support Maintenance Package

The support maintenance package is intended to be used when the product maintenance package fails to repair a problem. The support service representative can use it by itself if the MD is not available or is not operable. However the support maintenance package is entered, it contains both reference material and action-oriented material. You should enter the package at the block marked 'Start' on this page and follow the steps as they continue to other pages.

This Support Procedures section of the maintenance information contains the information about how to proceed to gather appropriate information, how to analyze that information, and how to use the action-oriented Fault Symptom Index (FSI), EAD, and DIAG sections.

Data That Can Be Available

- Fault symptom codes (FSCs) that are supplied by the product maintenance package. See PLAN 1 for "3480 Maintenance Package Summary."
- System console messages. See MSG 1 for "How to Use OS/VS/MVS System Console Messages."
- Drive message displays. See PANEL 1 for "Message Display Messages."
- EREP output. See MSG 1 for "Environmental Recording, Editing, and Printing Program."
- OLT messages. See *IBM 3480 Online Tests (OLTs)*, D99-3480.
- Audio-visual indications of the subsystem or media.
- Next level of support symptom file search.

Data Analysis

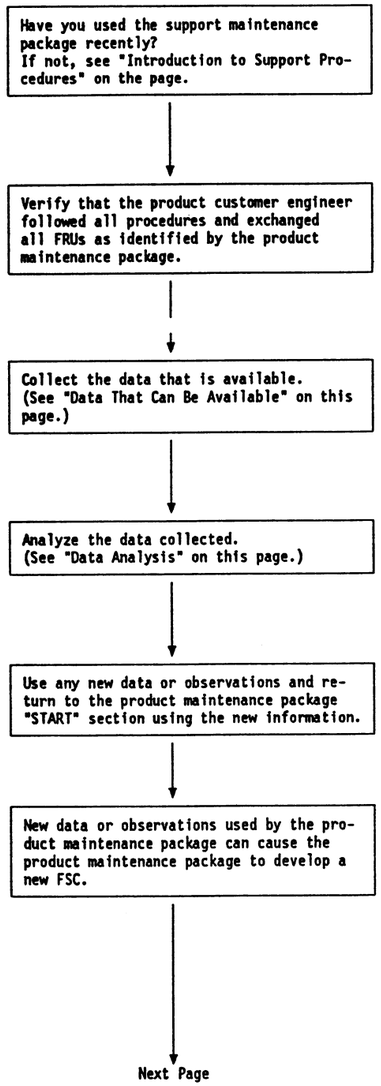
- Is it consistent?
- Does it indicate multiple problems?
- Is the problem (or one of the problems) obvious?
- Does the problem indicate system, programming, operator, or other errors?

If the problem analysis indicates some obvious errors, correct the obvious errors before you continue. If correcting the obvious errors shows that wrong data was used in the initial attempt to correct the problem, return to the product maintenance package with the new data and start again.

Some items to check in the data analysis are:

- Console messages
  - Some messages are abend codes. Look for other IEA000I messages, or EREP for the failing address. The IEA000I messages and EREP provide useful sense data for troubleshooting (see the MSG section).
- Console messages and EREP
  - Look for multiple records.
  - Are there earlier sense records for the failing address with different sense data (it is possible that after the original failing sense data, later sense data can indicate the effect of the problem, not the cause)?
  - Do multiple FSCs relate to a common problem?
  - Are FSCs common or similar for the drives on the same subsystem?
  - Check for possible common control unit problems.
- For two control unit configuration
  - Was the MD connected to the correct control unit?
  - Were the FRUs exchanged in the correct control unit?
  - See the MSG section for "Error Path Isolation."

Start



Introduction to Support Procedures

The information in Volumes A04 and A05 of this maintenance information make up the support material for the 3480 Magnetic Tape Subsystem. Each of the tabs within these volumes represents a section of information that aids the customer engineer in problem determination and repair at the support level.

The support customer engineer should already be thoroughly familiar with the information in Volumes A04 and A05. In addition, the product customer engineer can, with aid, use this information in troubleshooting when the product maintenance package fails to isolate a subsystem problem.

Support Maintenance Package

The support maintenance package supplies the customer engineer with a support diskette and documentation that can be used to isolate difficult subsystem problems. The support diskette gives the customer engineer the ability to select and run specific diagnostics or utilities. The support documentation supplies maintenance information beyond the scope of MAPs and procedures used by the product customer engineer.

When to Use the Support Maintenance Package

Use the support maintenance package to correct failures that were not repaired using the product maintenance package. The following kinds of failures may require use of the support maintenance package.

- The FRUs identified by the product maintenance package were not exchanged, or procedures were not followed as directed by the product maintenance package.
- Power is missing or out of tolerance at the point of failure.
- Connections between FRUs (cables, connectors, top card connectors, or board wiring) have short circuits or open circuits.
- A FRU exchanged by the product customer engineer is defective.
- A design problem exists in the hardware, the microcode, or the maintenance package.
- No trouble was found.
- Failures occur during installation or after EC rework.

Transition From the Product Maintenance Package to the Support Maintenance Package

The support maintenance package is intended to be used when the product maintenance package fails to repair a problem. The support customer engineer can use it by itself if the MD is not available or is not operable. However the support maintenance package is entered, it contains both reference material and action-oriented material. You should enter the package at the block marked 'Start' on this page and follow the steps as they continue to other pages.

This Support Procedures section of the maintenance information contains the information about how to proceed to gather appropriate information, how to analyze that information, and how to use the action-oriented fault symptom index (FSI), EAD, and DIAG sections.

Data That Can Be Available

- Fault symptom codes (FSCs) that are supplied by the product maintenance package. See PLAN 1 for "3480 Maintenance Package Summary."
- System console messages. See MSG 1 for "How to Use OS/VS/MVS System Console Messages."
- Drive message displays. See PANEL 1 for "Message Display Messages."
- EREP output. See MSG 1 for "Environmental Recording, Editing, and Printing Program."
- OLT messages. See *IBM 3480 Online Tests (OLTs)*, D99-3480.
- Audio-visual indications of the subsystem or media.
- Next level of support symptom file search.

Data Analysis

- Is it consistent?
- Does it indicate multiple problems?
- Is the problem (or one of the problems) obvious?
- Does the problem indicate system, programming, operator, or other errors?

If the problem analysis indicates some obvious errors, correct the obvious errors before you continue. If correcting the obvious errors shows that wrong data was used in the initial attempt to correct the problem, return to the product maintenance package with the new data and start again.

Some items to check in the data analysis are:

- Console messages
  - Some messages are abend codes. Look for other IEA000I messages, or EREP for the failing address. The IEA000I messages and EREP provide useful sense data for troubleshooting (see the MSG section).
- Console messages and EREP
  - Look for multiple records.
  - Are there earlier sense records for the failing address with different sense data (it is possible that after the original failing sense data, later sense data can indicate the effect of the problem, not the cause)?
  - Do multiple FSCs relate to a common problem?
  - Are FSCs common or similar for the drives on the same subsystem?
  - Check for possible common control unit problems.
- For two control unit configuration
  - Was the MD connected to the correct control unit?
  - Were the FRUs exchanged in the correct control unit?
  - See the MSG section for "Error Path Isolation."

0 0 0 0 0 0 0 0 0 0

From Preceding Page

Use the FSC developed by the product maintenance package. If you want to verify this FSC, use the data gathered in the preceding steps to develop a fault symptom code (see "Determining a Fault Symptom Code" on START 300). Use the fault symptom code to find the error as listed in the Fault Symptom Code Index (FSI) section. Return here after you find the fault symptom code in the FSI and continue with other verification actions first, before doing any troubleshooting actions in the FSI (see Note).

If you want to verify that the MD is connected to the correct control unit in a two control unit configuration, or that the FRUs were exchanged in the correct control unit, see START 400 for "Error Path Isolation".

Next Page

ATTENTION

Take care in using the FSI. The FSI is designed on the assumption that the identified error indicator is the selected fault symptom code (FSC), not just any error code taken from the sense bytes. This means that if you are to use the FSI for corrective action, the source of the FSC must be the product maintenance package exit or the result of following the "Determine a Fault Symptom Code" (see START 300).

Any use of the FSI other than for FSCs developed as stated above is for information purposes only. The 3480 develops many error codes in the sense data from the same problem. Some codes define the original cause of the problem, and other codes can be the result of attempted error recovery actions. Because all codes are not direct results of the original error, if you review an error code not given by the product maintenance package or not developed by following this FSC development procedure, you could be troubleshooting the effect of the problem, not its cause.

Note: The SPROC section procedures are used to verify that you are in the correct functional area before doing any more troubleshooting or corrective actions. These actions are, for example, re-running the product maintenance package if the newly developed FSC differs from the original FSC, or verifying that the MD was connected to the correct control unit during product maintenance. If your are sure that the earlier actions were correct and the existing information still points to the same area, continue with the actions specified in the FSI "Additional Action/Comments" column instead of returning to the SPROC block that sent you to this note. However, after completing all the actions specified in the FSI, you must return to SPROC 4 and follow "General Problem Definition Diagnostics," and if necessary the "End of Call Actions."

From Preceding Page

Use the information from the FSI to recheck the actions that were taken by the product CE.
(See "Rechecking Actions" on this page)

If the FSI explanation and your analysis are different, some of the data may have been interpreted incorrectly earlier. Return to the product maintenance package using the new data.

If the problem information is consistent and the FRUs have been exchanged, check the cables and boards identified by the FSI.

Perform the actions defined in the "Additional Actions/Comments" column in the FSI for the FSC, before continuing any other actions in this SPROC section. Use the information referenced in the FSI (EADs, diagnostics or others) to analyze the problem. Sometimes, a diagnostic or an EAD can lead you to a new error code. Use the new error code for the entry to the FSI for more fault isolation. Return here after all other defined actions have been done, whether the problem was fixed or not.

There are additional diagnostics available to test major functional areas of the 3480 subsystem. If you did not have enough data to define the problem, you can run any, or all of these programs to assist in defining

If you want to select these diagnostics, see "General Problem Definition Diagnostics", on this page.

Complete the call.
(See "End of Call Actions", on this page.)

Rechecking Actions

- Compare the FSI explanation of the problem being analyzed with what is known from the data collection and analysis done in the preceding steps. If the FSI explanation and your analysis vary widely, some misinterpretation of data may have occurred using the new data from the FSI. Return to the product maintenance package using the new data from the FSI.
- Compare the FRU list from the FSI with the FRU list developed by the product maintenance package. If the FRU lists do not match or, the product service representative did not exchange all the FRUs, exchange those FRUs that have not been exchanged.
- If the product maintenance package was not used, exchange the FRUs identified by the FSI.

General Problem Definition Diagnostics

The following are some general diagnostics that can be used to test the functional areas of the subsystem when there is not enough data to fully define a problem.

- Basic control unit tests within the subsystem
  - See "Basic CU Tests" on DIAG 1
- Basic drive tests within the subsystem
  - See the "Diagnostic Identification Table" on DIAG 3 for EE40 and EEA0
- Control unit commands: non-motion and motion including write and read commands from the host system
  - See *IBM 3480 Online Tests (OLTs)*, D99-3480, for OLT 3480A
- Subsystem pathing assignment tests from the host system
  - See *IBM 3480 Online Tests (OLTs)*, D99-3480, for OLT 3480B
- Subsystem write and read reliability tests with extended run times from the host system
  - See *IBM 3480 Online Tests (OLTs)*, D99-3480, for OLT 3480C
- Tape interchange tests with forced error logging for sense definition of temporary errors, from the host system
  - See *IBM 3480 Online Tests (OLTs)*, D99-3480, for OLT 3480D

End of Call Actions

Failure Has Not Been Repaired

If the failure has not been repaired, or is intermittent without a repair by either the product maintenance package or the support maintenance package, call your next level of support, then use the "No Trouble Found Procedures" EAD. Have a record of actions taken, FRUs exchanged, error codes observed, and any data collected during the analysis of the failure available when you call. If you leave the call, leave the record for follow-on effort.

Failure Has Been Repaired

If the failure has been found, verify the repair by retesting using the program or diagnostic test that originally failed. Rerun the product maintenance package, 'Unit Test' option, to run the functional verify program.

Record the actions taken during the call, FRUs exchanged, tests completed, and short ideas on how the fix was found.

From Preceding Page

Use the information from the FSI to recheck the actions that were taken by the product CE.
(See "Rechecking Actions" on this page)

If the FSI explanation and your analysis are different, some of the data may have been interpreted incorrectly earlier. Return to the product maintenance package using the new data.

If the problem information is consistent and the FRUs have been exchanged, check the cables and boards identified by the FSI.

Perform the actions defined in the "Additional Actions/Comments" column in the FSI for the FSC, before continuing any other actions in this SPROC section. Use the information referenced in the FSI (EADs, diagnostics or others) to analyze the problem. Sometimes, a diagnostic or an EAD can lead you to a new error code. Use the new error code for the entry to the FSI for more fault isolation. Return here after all other defined actions have been done, whether the problem was fixed or not.

There are additional diagnostics available to test major functional areas of the 3480 subsystem. If you did not have enough data to define the problem, you can run any, or all of these programs to assist in defining

If you want to select these diagnostics, see "General Problem Definition Diagnostics", on this page.

Complete the call.
(See "End of Call Actions", on this page.)

Rechecking Actions

- Compare the FSI explanation of the problem being analyzed with what is known from the data collection and analysis done in the preceding steps. If the FSI explanation and your analysis vary widely, some misinterpretation of data may have occurred using the new data from the FSI. Return to the product maintenance package using the new data from the FSI.
- Compare the FRU list from the FSI with the FRU list developed by the product maintenance package. If the FRU lists do not match or, the product customer engineer did not exchange all the FRUs, exchange those FRUs that have not been exchanged.
- If the product maintenance package was not used, exchange the FRUs identified by the FSI.

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  - See *IBM 3480 Online Tests (OLTs)*, D99-3480, for OLT 3480C
- Tape interchange tests with forced error logging for sense definition of temporary errors, from the host system
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End of Call Actions

Failure Has Not Been Repaired

If the failure has not been repaired, or is intermittent without a repair by either the product maintenance package or the support maintenance package, call your next level of support, then use the "No Trouble Found Procedures" EAD. Have a record of actions taken, FRUs exchanged, error codes observed, and any data collected during the analysis of the failure available when you call. If you leave the call, leave the record for follow-on effort.

Failure Has Been Repaired

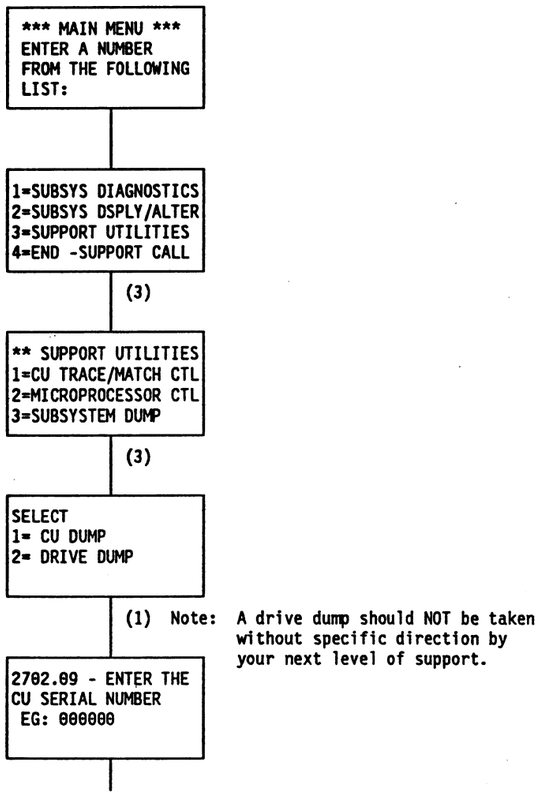
If the failure has been found, verify the repair by retesting using the program or diagnostic test that originally failed. Rerun the product maintenance package, 'Unit Test' option, to run the functional verify program.

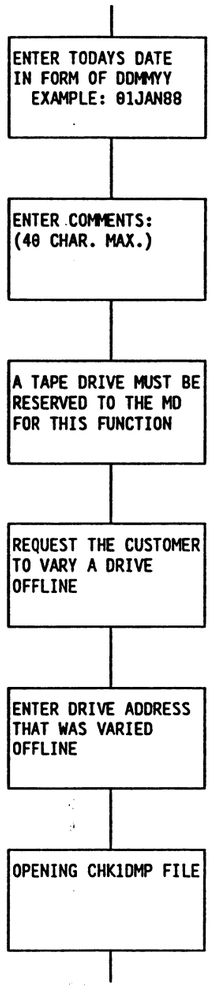
Record the actions taken during the call, FRUs exchanged, tests completed, and short ideas on how the fix was found.

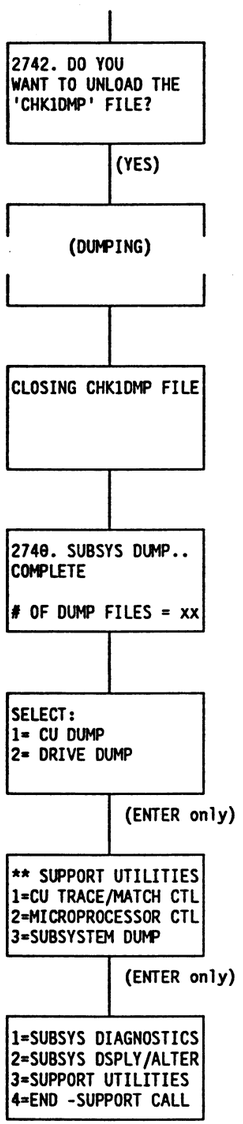
0 0 0 0 0 0 0 0 0 0

Taking a CHK1 dump

CHK1 dumps are recorded on the functional microcode diskette when errors are detected that are considered to be microcode related.. CHK1 dumps are not recorded for errors deemed to be hardware related because hardware controls may not be functional. The support diskette dump procedures will always interrogate the CHK1 dump area to determine if any valid data has been stored.

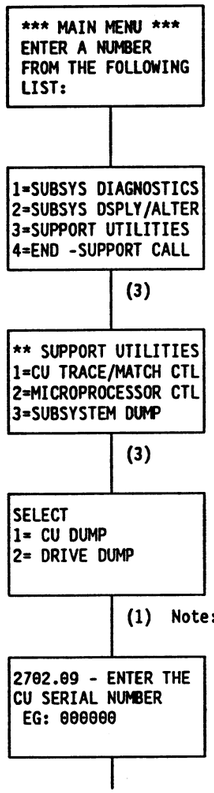




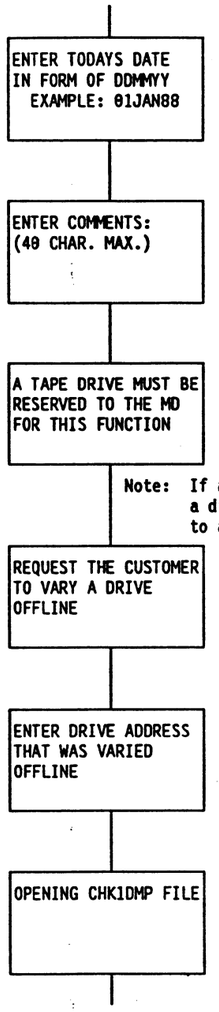


Taking a Concurrent Dump

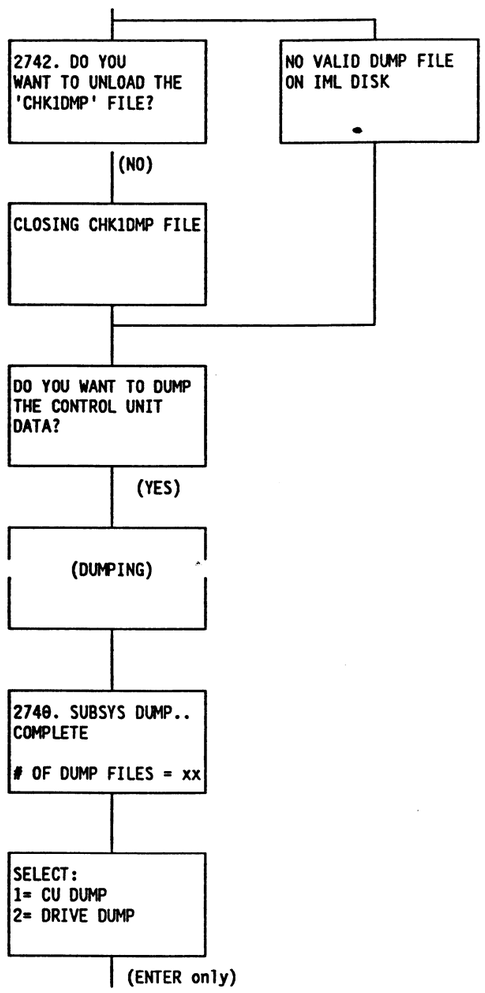
Concurrent control unit dumps are 'snapshots' of running control units that are taken without impact to the customer. These dumps are usually taken to determine the status of the control unit with respect to the host or the attached drives. For example, does a particular interface have access to a particular drive? Or, what was the last operation performed with a particular drive? This function is sometimes used if the problem can be recreated, but requires that the dump be obtained as soon as possible following an error. The depth of the trace tables is limited and other activity can cause pertinent data to be overwritten.

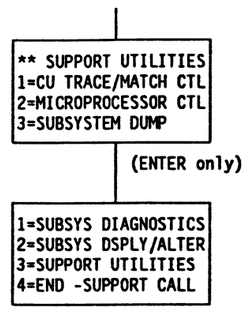


Note: A drive dump should NOT be taken without specific direction by your next level of support.



Note: If a drive problem is suspected, use a different drive for this function to avoid polluting the dump data.

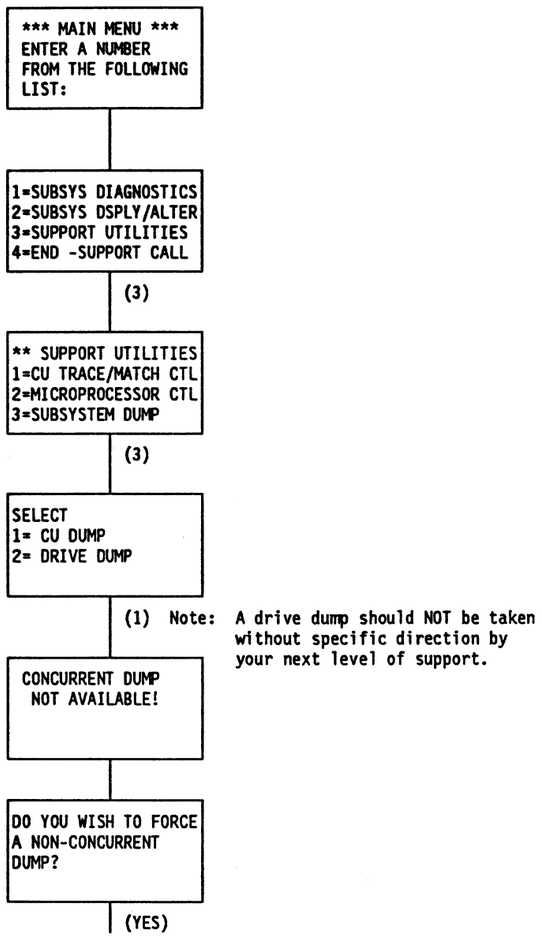


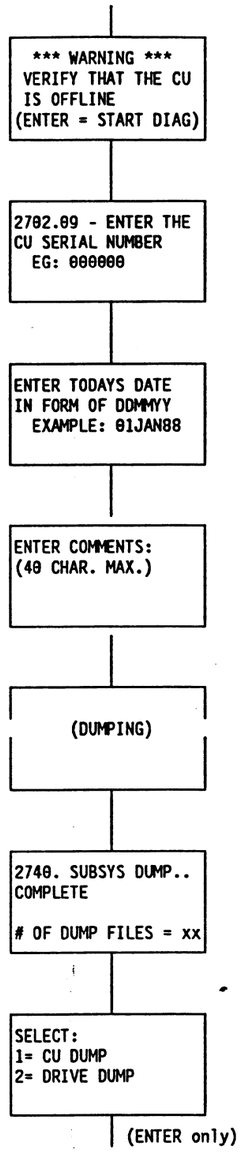


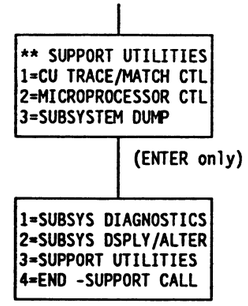
0 0 0 0 0 0 0 0 0 0

Taking a Non-Concurrent Dump

Non-concurrent control unit dumps are taken to preserve the contents of control storage following errors that stop the control unit clocks. The data is 'clocked' out of the control unit using the Maintenance Device (MD) and as a result, is slightly slower than a concurrent dump.

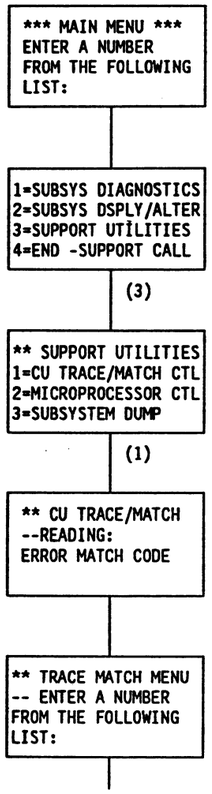


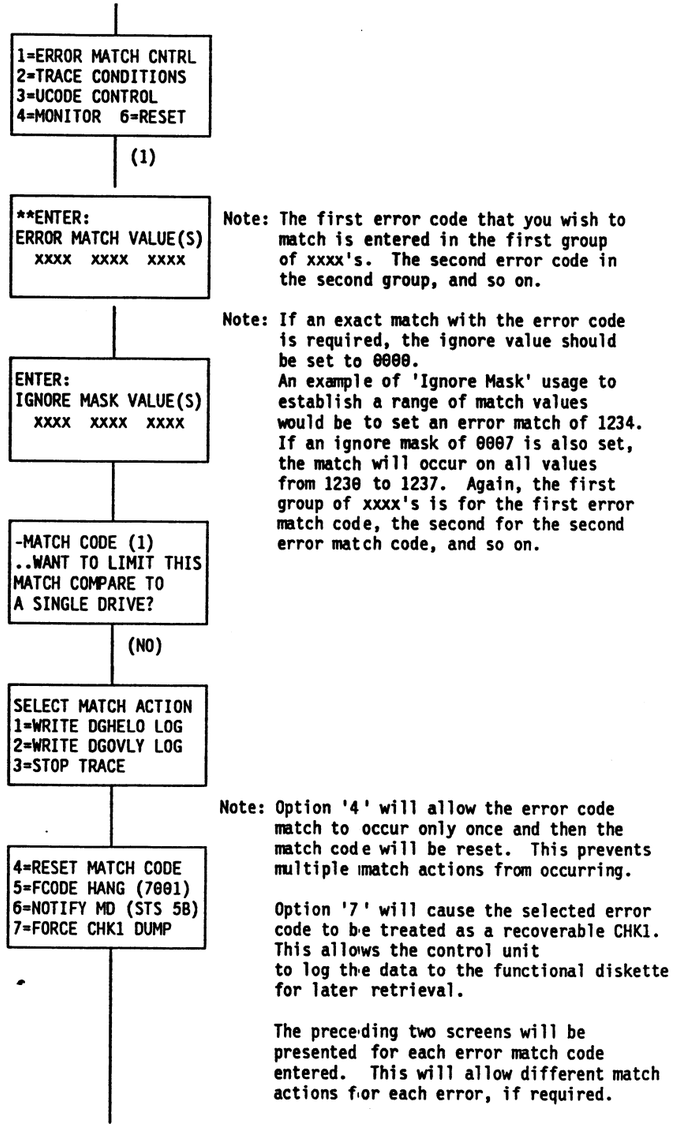




0 0 0 0 0 0 0 0 0 0

Setting Error Match Codes and Trace Conditions





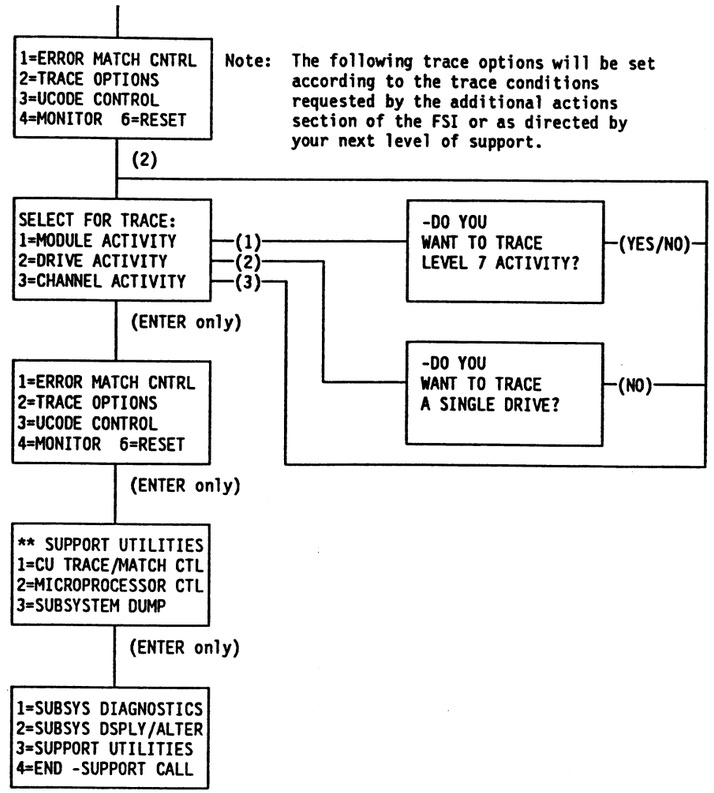
Note: The first error code that you wish to match is entered in the first group of xxxx's. The second error code in the second group, and so on.

Note: If an exact match with the error code is required, the ignore value should be set to 0000.
An example of 'Ignore Mask' usage to establish a range of match values would be to set an error match of 1234. If an ignore mask of 0007 is also set, the match will occur on all values from 1230 to 1237. Again, the first group of xxxx's is for the first error match code, the second for the second error match code, and so on.

Note: Option '4' will allow the error code match to occur only once and then the match code will be reset. This prevents multiple match actions from occurring.

Option '7' will cause the selected error code to be treated as a recoverable CHK1. This allows the control unit to log the data to the functional diskette for later retrieval.

The preceding two screens will be presented for each error match code entered. This will allow different match actions for each error, if required.



Note: The following trace options will be set according to the trace conditions requested by the additional actions section of the FSI or as directed by your next level of support.

0 0 0 0 0 0 0 0 0 0

Microcode Error Problem Determination

This procedure is used whenever an error in the MD microcode is suspected. The procedure causes a unique label to be entered in the MD trace table (PELOG) and the table is then written to the MD diskette. After performing the procedure, the next level of support should be contacted to determine the next course of action. The diskette may need to be forwarded to engineering for further analysis of the trace table.

Note: The error code can only be generated when running the MD and may not relate to any customer problems.

Procedure E

1. Press the RESET button on the MD.
2. When the MAIN MENU appears on the MD keyboard/display, remove the diskette from the MD.
3. Call your next level of support for further instructions.

0 0 0 0 0 0 0 0 0 0

0 0 0 0 0 0 0 0 0 0

Contents

Support Plan

The support plan provides SRs with a support diskette and documentation that can be used to isolate difficult or intermittent subsystem problems.

The support diskette gives SRs the ability to select and run specific diagnostics or utilities. The support documentation provides maintenance information beyond the scope of MAPs and procedures used by product SRs.

Note: The MD displays in the following diagrams may not be the same as the actual MD displays.

Support Diskette

The support diskette supplies the following facilities:

- Subsystem diagnostics
- Subsystem display and alter programs
- Support utility programs.

The subsystem diagnostics are explained in the DIAG section of the maintenance information. This SDISK section explains the subsystem display and alter programs and the support utility programs.

You can perform two classes of maintenance with the support diskette:

- Concurrent maintenance. This class of maintenance lets a customer run jobs on all of the subsystem except on the drive you are troubleshooting. Subsystem performance may be slightly degraded.
- Non-concurrent maintenance. The subsystem is not available for customer use.

Subsystem Display and Alter Programs

The subsystem display and alter programs perform as a service panel. They permit you to:

- Display the subsystem configuration.
- Display and alter various storages in the subsystem.
- Display and alter various registers in the subsystem.
- The PF key causes the current program to stop running and returns to the 'MAIN MENU'.
- Null (pressing the enter key only) causes the current operation to stop and returns to the preceding menu, or to what is defined on the MD screen.

Support Utilities Programs

The support utilities programs permit you to:

- Perform a microcode trace
- Operate the microprocessor in the control unit
- Dump data from the control unit and the drives.

Loading The Support Diskette

To load the support programs, insert the support diskette into the maintenance device and press the IPL key. The MD then performs an initial program load (IPL) to load the support programs. When the initial program load (IPL) is complete, the following screen displays:

```
3480  SUPPORT DSKT
DISKETTE PN= 4770121
DISKETTE EC= xxxxxxx
CU0= xxxxx CU1=xxxxx
```

This screen provides the part number and EC level of the diskette and the serial numbers of the subsystem control units.

Press ENTER: The following screen displays:

```
     *WARNING*
YOU MAY DESTROY NEW
DISKETTES IF THEY ARE
INSERTED          ...
```

This warning indicates that when a diskette is IPL'ed and being used, you cannot remove this diskette and insert another diskette and continue without IPLing the MD.

Press ENTER:

```
ALWAYS IPL THE MD
WHEN CHANGING 3480
MD DISKETTES
```

This screen is a reminder to IPL the last diskette inserted into the MD.

Press ENTER: The following screen displays:

```
*** MAIN MENU ***
ENTER A NUMBER
FROM THE FOLLOWING
LIST :            ...
```

This is the Main Menu title screen. If you know the menu selection, you can enter it via this screen. If you do not know the selection,

Press ENTER: The following selection screen displays:

```
1=SUBSYS DIAGNOSTICS
2=SUBSYS DSPLY/ALTER
3=SUPPORT UTILITIES
4=END -SUPPORT CALL
```

You can select the major support programs from this screen.

Some support diagnostic routines are non-concurrent. If possible, all other troubleshooting procedures should be performed before taking the subsystem away from the customer.

The diagnostics are defined in the Diagnostic Procedures (DIAG) section of the MI. Support utilities and subsystem display/alter selections are explained in this section. Registers displayed by the support programs and diagnostic routines, which are useful for isolating hardware failures, are explained in the Data Fields (DF) section of the MI.

Support Diskette Procedures Description

- An overview flow chart is provided for the Main Menu selection.
- The flow for each procedure begins at the selection screen that displays after the Main Menu selection has been entered.
- Blocks represent MD display output.
- All charts start at 'MAIN MENU'.
- MD display information screens are included only if they contain information needed to use the procedure.
- Pressing the PF key causes the current operation to stop and returns to the 'MAIN MENU'.

Subsystem Display/Alter

Display Subsystem Configuration

The following procedure is used to display the subsystem configuration:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 2 (SUBSYS DSPLY/ALTER).
4. Enter a 1 (SUBS CONFIG. DSPLY) from the Display/Alter menu screen.

Subsystem Component Descriptions

Control Unit and drive description display **1**:

3480 MODEL = Control Unit model number - Defined by switches on the device adapter card (01A-A1Q2).

SN = Control Unit unit serial number.

CUID = Setting of the CU0/CU1 switch on the control unit operator panel.

DRIVE MODEL = Drive model number - Defined by switches on the device adapter card (01A-A1Q2).

CUS = Defines the number of control units in the subsystem.

CHAN = Defines the number of channel adapters and their locations (A, B , C, D).

Microcode description display **2**:

UCODE PN = Identifies the part number of the functional microcode currently loaded in the control unit.

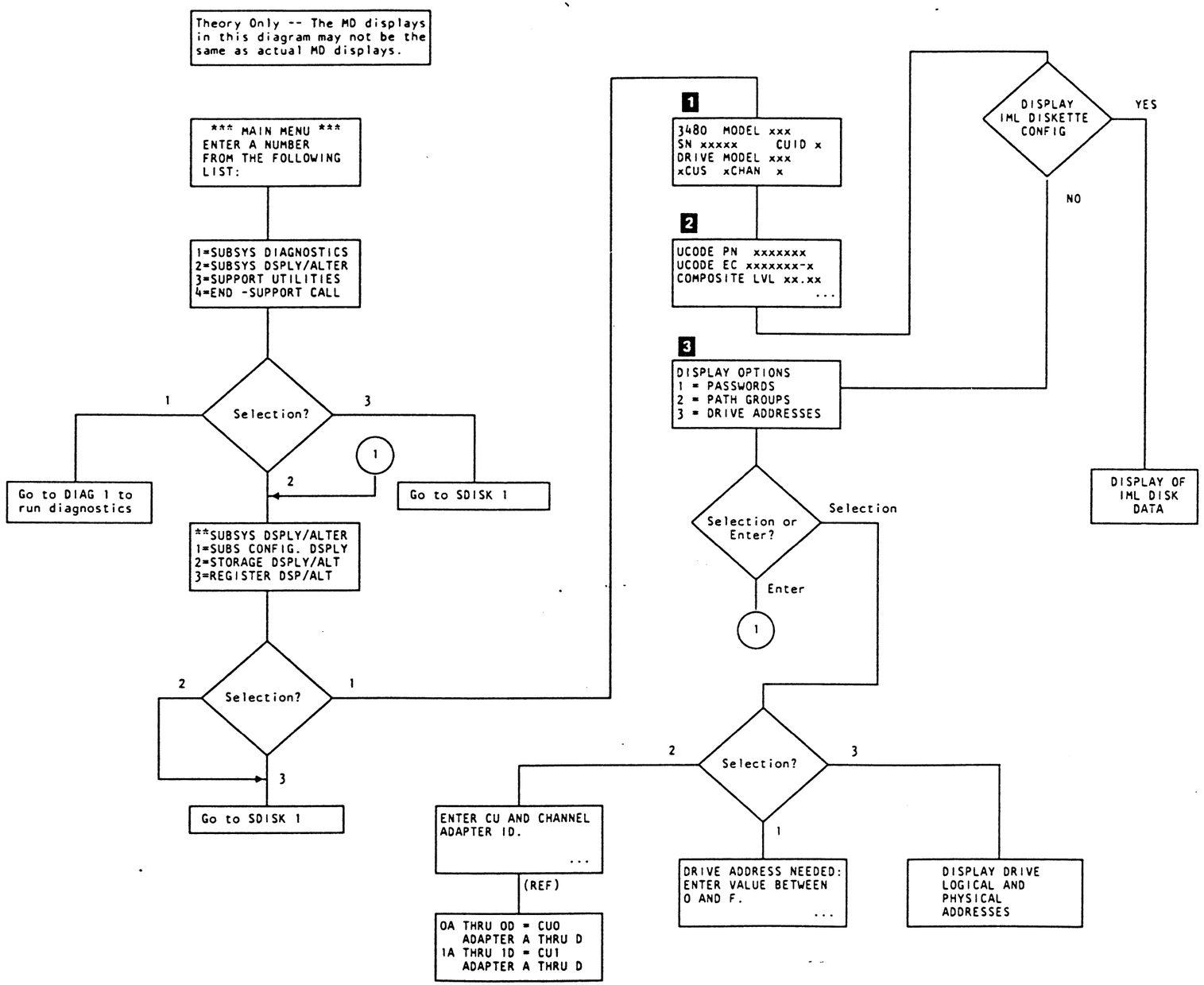
UCODE EC = Identifies the EC level of the functional microcode currently loaded in the control unit.

COMPOSITE LVL = Defines the linked composite of the functional microcode currently loaded in the control unit.

Display options display **3**:

PASSWORDS = Unique passwords assigned by the host system for specified drives.

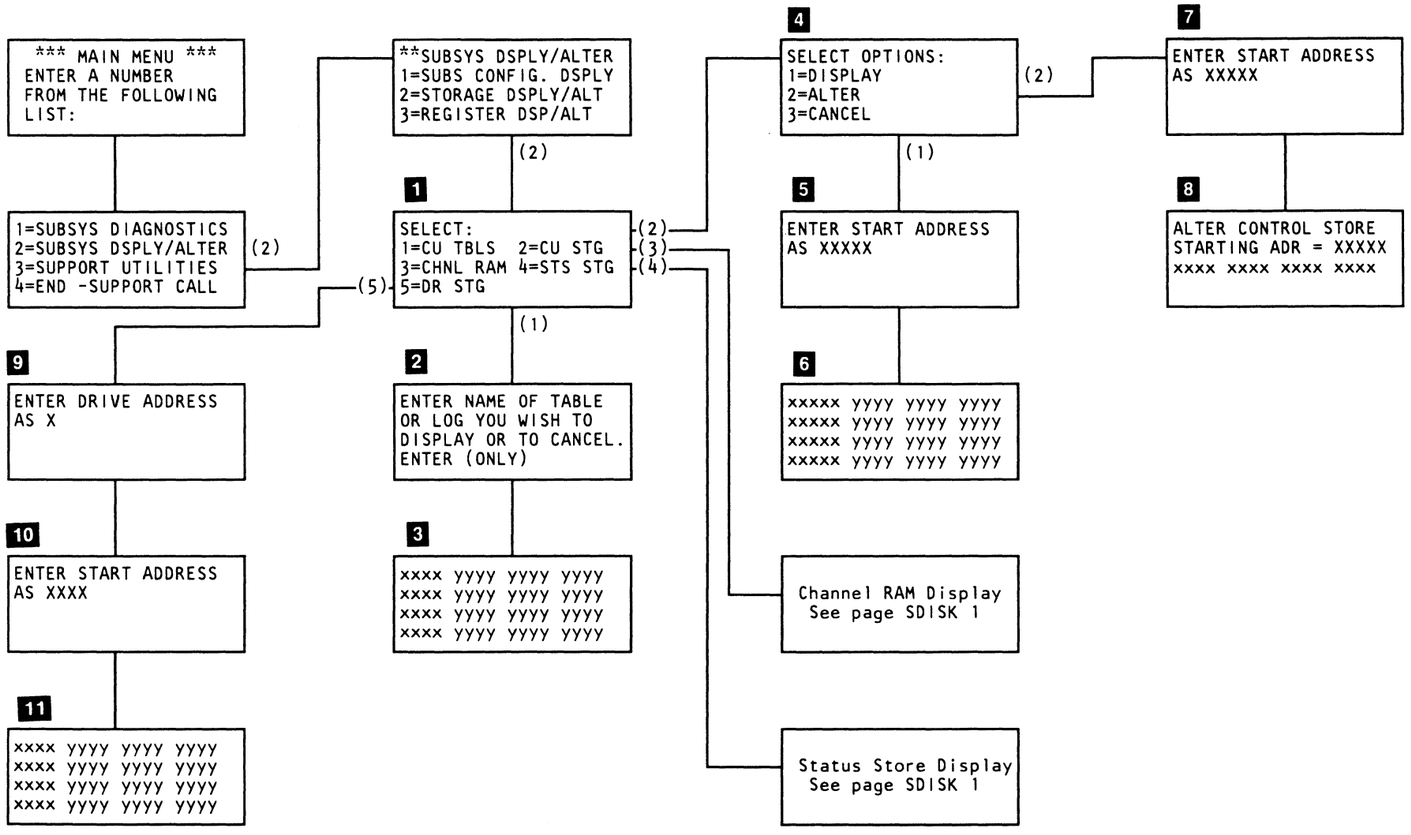
PATH GROUPS = Unique path IDs assigned by the host system for specified channel adapters.



Subsystem Display/Alter

Storage Display/Alter Diagram

Theory Only -- The MD displays in this diagram may not be the same as actual MD displays.



Subsystem Display/Alter (Continued)

Storage Display/Alter

The following procedure is used to display or alter subsystem storage, tables, and logs with the maintenance device:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 2 (SUBSYS DSPLY/ALTER).
4. Enter a 2 (STORAGE DSPLY/ALT) from the Display/Alter menu screen.
5. SELECT one of the following:

   1 = CU TBLS - Control unit tables
   2 = CU STG - Control unit storage (Control Storage)
   3 = CHNL RAM - Channel buffer
   4 = STS STG - Status storage
   5 = DR STG - Drive storage

Note: Display functions can be performed concurrently with customer operations. Alter functions are non-concurrent and are allowed only if the control unit microprocessor is stopped. You must vary all channel paths offline in the controlling computer operating system and take the control unit offline before performing any alter function.

Control Unit Tables

To display control unit tables:

1. Enter a 1 (CU TBLS) when the selection screen **1** displays.
2. Enter the acronym for the table you want to display **2**. For example, enter CST to display the Control Status Table. The table displays **3** in the following format:

   a. The x's represent the address of the data.

   b. The y's represent the data beginning at the xxxx address.

   Note: Refer to the Data Fields (DF) registers section of the MI for a description of the table data.

3. Press ENTER to display the next four address locations.

To exit from a table display, press the maintenance device RET (Return) key. The ENTER NAME OF TABLE **2** screen displays.

Control Unit Control Storage

The subsystem display/alter function allows you to display and alter control storage for trouble analysis. This function is particularly helpful when trying to isolate intermittent problems or problems that are difficult to define.

Display Control Storage

To display control storage:

1. Enter a 2 (CU STG) when the selection screen **1** displays.
2. Enter a 1 (DISPLAY) when the select option screen **4** displays.
3. Enter the address of the first storage location (START ADDRESS) that you want to display **5**. Control storage displays **6** in the following format:

   a. The x's represent the address of the data.

   b. The y's represent the data beginning at the xxxx address.

To exit from display mode, press the maintenance device RET (Return) key. The SELECT OPTION screen displays.

Alter Control Storage

Warning: Altering control storage overlays subsystem microcode. The subsystem must be offline before using the ALTER function and an IML must be performed again before it is returned to the customer.

. . . . . .

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To alter control storage:

1. Enter a 2 (CU STG) when the selection screen **1** displays.
2. Enter a 2 (ALTER) when the select option screen **4** displays.
3. Enter the address of the first storage location (START ADDRESS) that you want to change **7**.
4. When the ALTER CONTROL STORE screen **8** displays, use the MD space key to move the cursor under the byte to be altered. Input new data.

   Note: Do not press the ENTER key until all data for the screen has been entered.

To exit from alter mode, press the maintenance device RET (Return) key. The SELECT OPTION screen displays.

Drive Control Storage

The subsystem display/alter function allows you to display drive control storage for trouble analysis.

Display Control Storage

To display control storage:

1. Enter a 5 (DR STG) when the selection screen **1** displays.
2. Enter a drive address when screen **9** displays.
3. Enter the address of the first storage location (START ADDRESS) that you want to display **10**. Control storage displays **11** in the following format:

   a. The x's represent the address of the data.

   b. The y's represent the data beginning at the xxxx address.

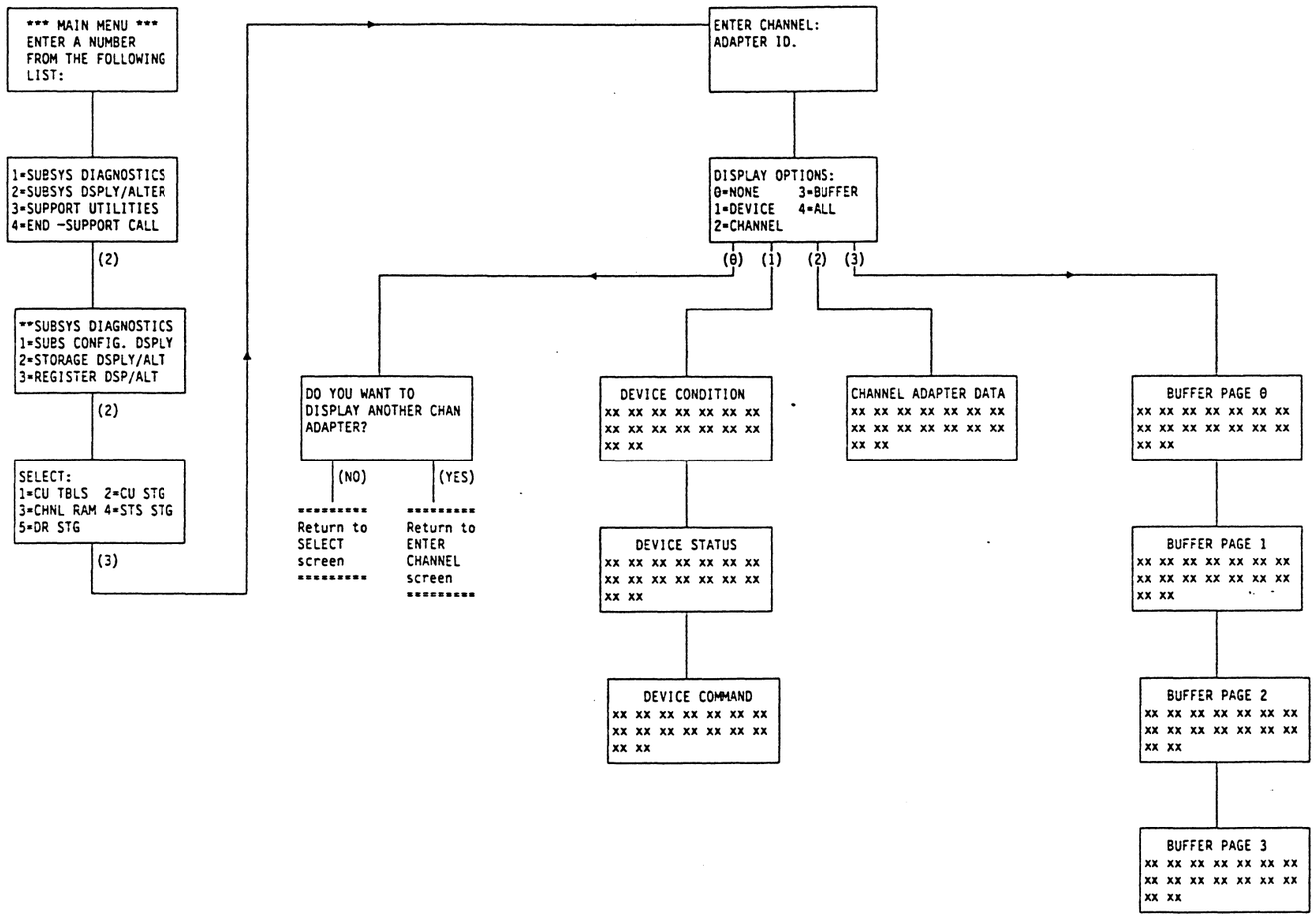
To exit from display mode, press the maintenance device RET (Return) key. The SELECT OPTION screen displays.

Note: You cannot alter drive control storage.

Subsystem Display/Alter (Continued)

Channel RAM Display Diagram

Theory Only — The MD displays in this diagram may not be the same as actual MD displays.



Subsystem Display/Alter (Continued)

Channel RAM Display

The following procedure is used to display channel buffer data:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 2 (SUBSYS DSPLY/ALTER).
4. Enter a 2 (STORAGE DSPLY/ALT) from the Display/Alter menu screen.
5. Enter a 3 (CHNL RAM).
6. Enter the channel adapter ID (A, B, C, or D).
7. Select one of the following DISPLAY OPTIONS:

   0 = NONE
   1 = DEVICE
   2 = CHANNEL
   3 = BUFFER
   4 = ALL

Note: One entry is used for each device starting with device 0.

Subsystem Display/Alter (Continued)

Status Store Display Diagram

Theory Only — The MD displays in this diagram may not be the same as actual MD displays.

```
*** MAIN MENU ***
ENTER A NUMBER
FROM THE FOLLOWING
LIST:

1=SUBSYS DIAGNOSTICS
2=SUBSYS DSPLY/ALTER
3=SUPPORT UTILITIES
4=END -SUPPORT CALL

(2)

**SUBSYS DSPLY/ALTER
1=SUBS CONFIG. DSPLY
2=STORAGE DSPLY/ALT
3=REGISTER DSP/ALT

(2)

SELECT:
1=CU TBLS  2=CU STG
3=CHNL RAM 4=STS STG
5=DR STG

(4)

0=QUIT
1=DEVICE DATA
2=INTERFACE DATA
3=CHECK1 DATA

4=MESSAGE BUFFER 0
5=MESSAGE BUFFER 1
6=ALL SS IN HEX FORM
```

```
DISPLAY OPTIONS
0=NONE      3=ERRORS
1=DEVICE    4=BUFF0
2=ASSIGN

(ENTER)

(REF)(1) (2) (3) (4)
```

```
5=BUFF1
6=HEX ALL

(5)  (6)
```

1

```
DEVICE ASSIGNMENTS
xx xx xx xx xx xx xx
xx xx xx xx xx xx xx
xx xx
```

2

```
DEVICE  STATUS
xx xx xx xx xx xx xx
xx xx xx xx xx xx xx
xx xx
```

3

```
DEVICE ASSIGN MASK
xx xx xx xx xx xx xx
xx xx xx xx xx xx xx
xx xx
```

4

```
DEVICE PROGRAM FLAGS
xx xx xx xx xx xx xx
xx xx xx xx xx xx xx
xx xx
```

5

```
INTFC ASSIGNMENTS
CHAN A B C D  SER
C 0
C 1
```

6

```
ERROR CODES
xxxxxxxxxx
```

7

```
80 xx xx xx xx xx xx
86 xx xx xx xx xx xx
8C xx xx xx xx xx xx
92 xx xx xx xx xx xx

98 xx xx xx xx xx xx
9E xx xx xx xx xx xx
A4 xx xx xx xx xx xx
AA xx xx xx xx xx xx

B0 xx xx xx xx xx xx
B6 xx xx xx xx xx xx
BC xx xx xx xx
```

8

```
C0 xx xx xx xx xx xx
C6 xx xx xx xx xx xx
CC xx xx xx xx xx xx
D2 xx xx xx xx xx xx

D8 xx xx xx xx xx xx
DE xx xx xx xx xx xx
E4 xx xx xx xx xx xx
EA xx xx xx xx xx xx

F0 xx xx xx xx xx xx
F6 xx xx xx xx xx xx
FC xx xx xx xx
```

9

```
00 xx xx xx xx xx xx
06 xx xx xx xx xx xx
0C xx xx xx x
12 xx xx xx xx xx xx

=======
00 Through FF

F0 xx xx xx x
F6 xx xx xx xx xx xx
```

Subsystem Display/Alter (Continued)

Status Store Display

The Status Store selection is used to display the status of the subsystem.

The following procedure is used to display status storage data:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 2 (SUBSYS DSPLY/ALTER).
4. Enter a 2 (STORAGE DSPLY/ALT) from the Display/Alter menu screen.
5. Enter a 4 (STS STG).
6. Select one of the following DISPLAY OPTIONS:

   0 = NONE
   1 = DEVICE
   2 = ASSIGN
   3 = ERRORS
   4 = BUFF0

   Note: *Status Store is initialized to:*

   Device Assignment = *X'00'*
   Device Status = *X'0E'*
   Device Assignment Mask = *X'FF'*
   Device Program Flags = *X'00'*

Device Assignments

One device assignment entry for each device starting with device 0 **1**:

80 = Control Unit 0, Adapter A
40 = Control Unit 0, Adapter B
20 = Control Unit 0, Adapter C
10 = Control Unit 0, Adapter D
08 = Control Unit 1, Adapter A
04 = Control Unit 1, Adapter B
02 = Control Unit 1, Adapter C
01 = Control Unit 1, Adapter D

Device Status

One device status entry for each device starting with device 0 **2**:

Bit 0 = Deferred unit check
Bit 1 = Not file protect
Bit 2 = Buffer assigned to control unit 0
Bit 3 = Buffer assigned to control unit 1
Bit 4 = Buffer write
Bit 5 = Buffer full/backward
Bit 6 = Buffer empty
Bit 7 = Device ready

Device Assignment Mask

One device assignment mask entry for each device starting with device 0 **3**:

80 = Control Unit 0, Adapter A
40 = Control Unit 0, Adapter B
20 = Control Unit 0, Adapter C
10 = Control Unit 0, Adapter D
08 = Control Unit 1, Adapter A
04 = Control Unit 1, Adapter B
02 = Control Unit 1, Adapter C
01 = Control Unit 1, Adapter D

Device Program Flags

One device program flag entry for each device starting with device 0 **4**:

80 = Local system reset
40 = Remote system reset
30 = CMP device deadlock state
20 = CU0 CMP device interlock
10 = CU1 CMP device interlock
08 = All channel paths assigned
04 = Device at BOT
02 = Initial extended contingent connection
01 = Give busy for extended contingent connection

Interface Assignments

An 'X' identifies which channel the control unit is using and whether it is assigned the serial bus **5**.

Error Codes

This is the error code of the last recovered Check 1 error **6**.

Buffer 0

This display contains control unit to control unit messages. Control unit 1 in write mode and control unit 0 in read mode **7**.

Buffer 1

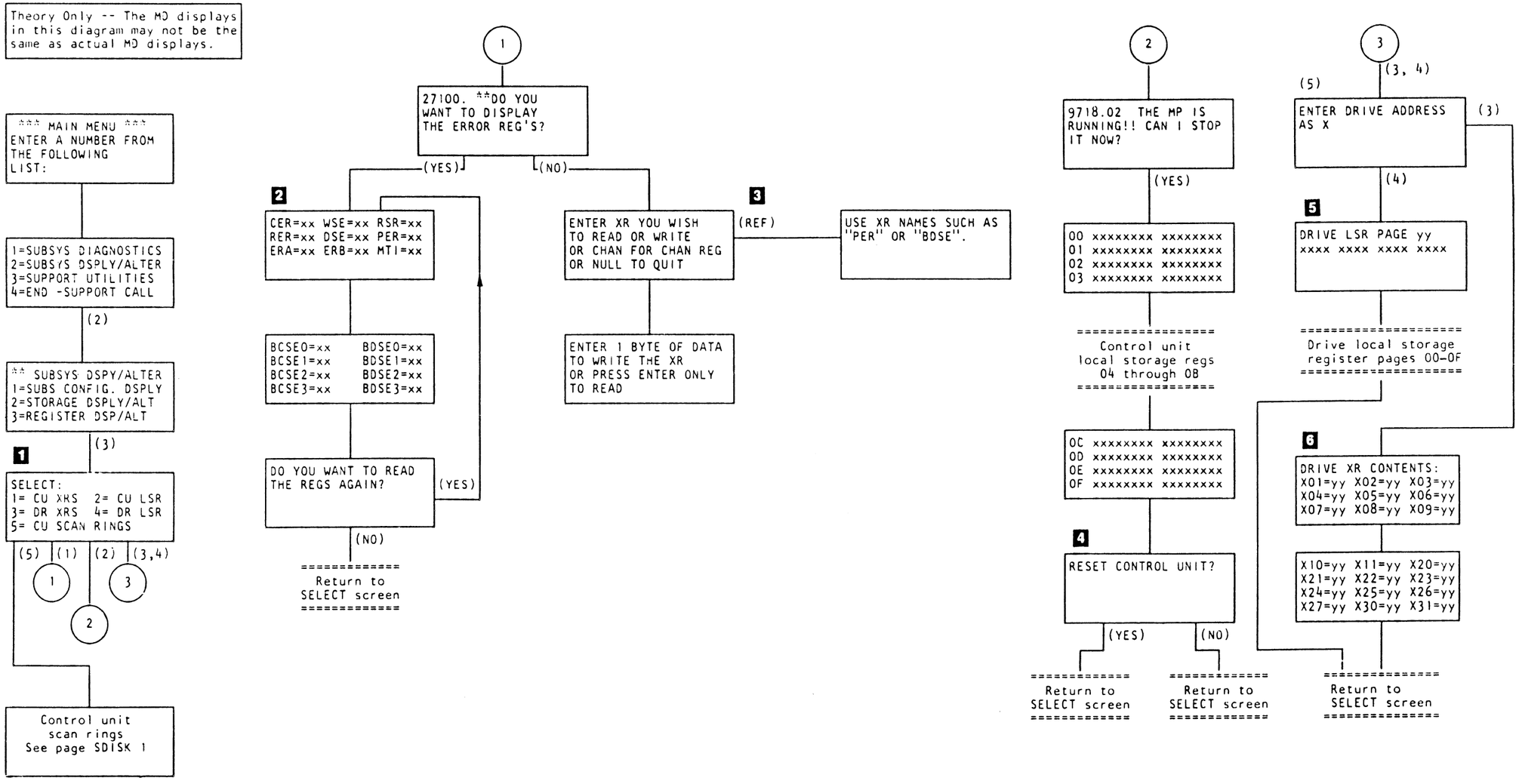
This display contains control unit to control unit messages. Control unit 0 in write mode and control unit 1 in read mode **8**.

Hex All

This selection provides a dump of all Status Store information (address 00 through FF) **9**.

Subsystem Display/Alter (Continued)

Register Display/Alter Diagram



Subsystem Display/Alter (Continued)

Register Display/Alter

The register display/alter routine lets you display or alter selected subsystem registers and to display the control unit scan rings.

Note: When the alter external register function is used, a subsystem reset is needed before the subsystem can be returned to the customer.

The following procedure is used to display control unit external registers:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 2 (SUBSYS DSPLY/ALTER).
4. Enter a 3 (REGISTER DSP/ALT) from the Display/Alter menu screen.
5. Select one of the following **1**:

   1 = CU XRS - Control Unit External Registers
   2 = CU LSR - Control Unit Local Storage Registers
   3 = DR XRS - Drive External Registers
   4 = DR LSR - Drive Local Storage Registers
   5 = CU SCAN RINGS - Control Unit Scan Register

The DF (Data Fields and Registers) section of the MI defines the registers that are useful when troubleshooting subsystem failures.

Error Registers

Error register definitions **2**:

CER = Channel Error Register
RER = Read Error Register
ERA = Error Register A
WSE = Write Status Error
DSE = Device Status Error
ERB = Error Register B
RSR = Read Status Register
PER = Processor Error Register
MTI = Maintenance Tag In
BCSE = Buffer Channel Status Error Register
BDSE = Buffer Device Status Error Register

Register data fields are defined in the Data Fields (DF) register section of the MI.

Reference Screen

The reference screen **3** is obtained by pressing the MD keyboard/display REF key. The screen is used for prompting and to ensure that correctly formatted data is entered.

Note: See the DF section of the MI for XR names, pages, and addresses.

Reset Control Unit

The control unit can be reset by answering yes to the question displayed on this screen **4**:

YES - Resets the control unit and forces a return to the SELECT screen.

NO - Forces a return to the SELECT screen.

Display Drive LSRs and XRs

Before you can display drive XRs **6** or LSRs **5**, the functional microcode must be running and the drive must be available to the MD (not assigned to a host processor).

Notes:

1. See the DF section for definitions of pertinent drive XR bits.
2. Unless indicated in a specific diagnostic, the contents of the external registers may be different from the original diagnostic display.

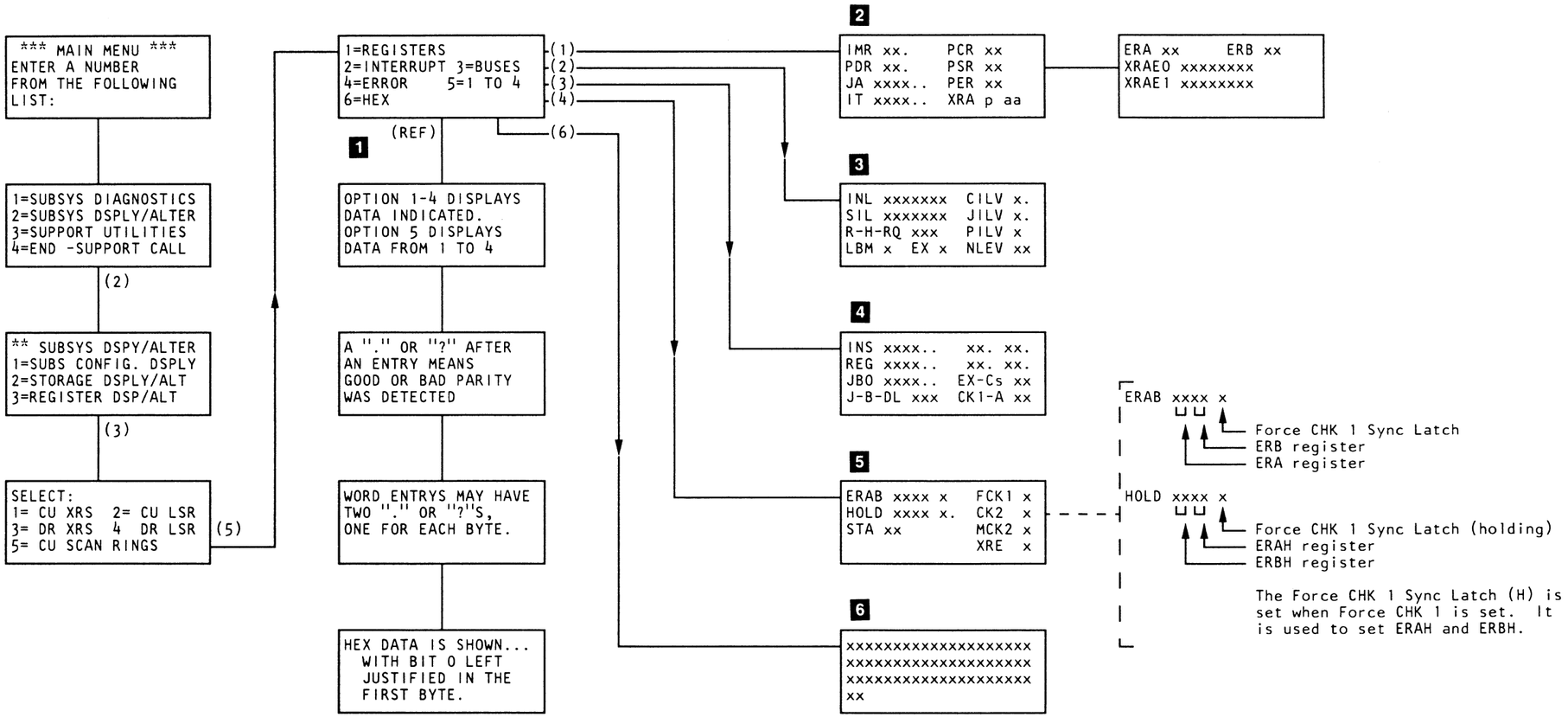
Subsystem Display/Alter (Continued)

Subsystem Display/Alter (Continued)

Subsystem Display/Alter (Continued)

Control Unit Scan Rings Diagram

Theory Only -- The MD displays in this diagram may not be the same as actual MD displays.



Subsystem Display/Alter (Continued)

Control Unit Scan Rings

The Control Unit Scan Ring routine allows you to display registers, interrupts, buses and error information when a Check 1 error condition exists.

The following procedure is used to display control unit scan rings:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 2 (SUBSYS DSPLY/ALTER).
4. Enter a 3 (REGISTER DSP/ALT) from the Display/Alter menu screen.
5. Enter a 5 (CU SCAN RINGS).
6. Select one of the following:

   1 = REGISTERS
   2 = INTERRUPT
   3 = BUSES
   4 = ERROR
   5 = 1 TO 4
   6 = HEX

Note: Scan ring data will not be valid unless a Check 1 condition exists.

Registers

The following registers are displayed **2** when the REGISTERS option is selected:

IMR = Interrupt Mask Register
PDR = Processor Diagnostic Register
JA = Processor Address high and low
IT = Interval Timers A and B
PCR = Processor Control Register
PSR = Processor Status Register
PER = Processor Error Register
XRA = External Register Address
p = page
aa = address
ERA = Error Register A (Ck 1)
ERB = Error Register B (Ck 1)
XRAE = External Register Address Extended

Note: The Data Fields (DF) section of the MI defines the registers that are useful when troubleshooting subsystem failures.

Interrupt

The following interrupt information is displayed **3** when the INTERRUPT option is selected:

INL = Interrupt Latches
SIL = Sample Interrupt Latches
R-H-RQ = Return, Hold, and Request Latches
LBM = Level Before Master Mask
EX = Extended Operation
CILV = Current Interrupt Level
JILV = Pending Processor Interrupt Level
PILE = Previous Interrupt Level
NLEV = New Interrupt Level

Buses

The following bus information is displayed **4** when the BUSES option is selected:

INS = Instruction register and source high/low. xx xx equals the location of the register (CS CS).
REG = Fetch Register. xx xx equals the location of the register (XR XR).
JBO = Processor Bus Out
J-B-DL = Jump, Blowout, and Disable LSR
Ex-CS = Extended Operations and Cycle Steal delayed latches
CK1-A = First bit on indicates that a Check 1 error latch is on. Second bit on indicates that multiple error latches are on.

Error

The following error information is displayed **5** when the ERROR option is selected:

ERAB = Error Registers A and B
HOLD = Holding registers for ERA and ERB (ERAH and ERBH). Indicates the condition that caused the first check 1 error.
STA = Scan only register; used to load CRR and ERR registers.
FCK1 = Force Check 1 on
CK2 = Check 2 on
MCK2 = Microprocessor Check 2
XRE = External Register Error

Hex Display

A Hex display of the scan rings is provided **6** when the HEX option is selected.

MD Reference Key

Provides prompting and information **1** about the option screen selections.

Notes SDISK 135

Notes SDISK 135

Support Utilities

Introduction

The following support utilities are selected from a support diskette utilities menu:

- Trace/Match control
- Microprocessor control
- Subsystem dump.

Trace/Match Control

The CU Trace/Match Control program gives you the ability to perform a microcode trace. It lets you stop or record specific error conditions and microcode data fields. The utility provides MI-defined data that aids you when isolating machine malfunctions. Trace/match control will run in concurrent and non-concurrent maintenance modes; however running this option in concurrent mode may affect system operation. Cautions that must be observed when running in concurrent mode are noted in the Trace/Match Control Procedure Details.

Microcode control options affect subsystem performance. All options except 1, 2 and 9 are reset when exiting from the utility.

Microprocessor Control

Note: The microprocessor control functions may cause errors at the host system.

The support diskette contains programs that provide service representative panel-like functions. The following functions may be selected to supply microprocessor control from the MD keyboard/display:

- Microprocessor reset
- Microprocessor start
- Microprocessor stop
- Microprocessor instruction step
- Address compare/stop
- Force branch
- Set/reset ignore error
- Set/reset check stop
- Set/reset check 2 = check 1
- Reset maintenance control register.

Subsystem Dump

The Subsystem Dump program dumps control unit or drive data fields and registers from the subsystem onto the support diskette dump area. The dumped data will be analyzed by your next level of support.

Sources of data for the control unit dump are the IML diskette and control store.

Selecting CU dump will cause the MD to automatically search for dump files, posting information to the keyboard display.

All dump activity is attempted in the concurrent mode (functional microcode running). If the functional microcode is not running, the MD will default to the non-concurrent mode, posting informational messages on the keyboard display.

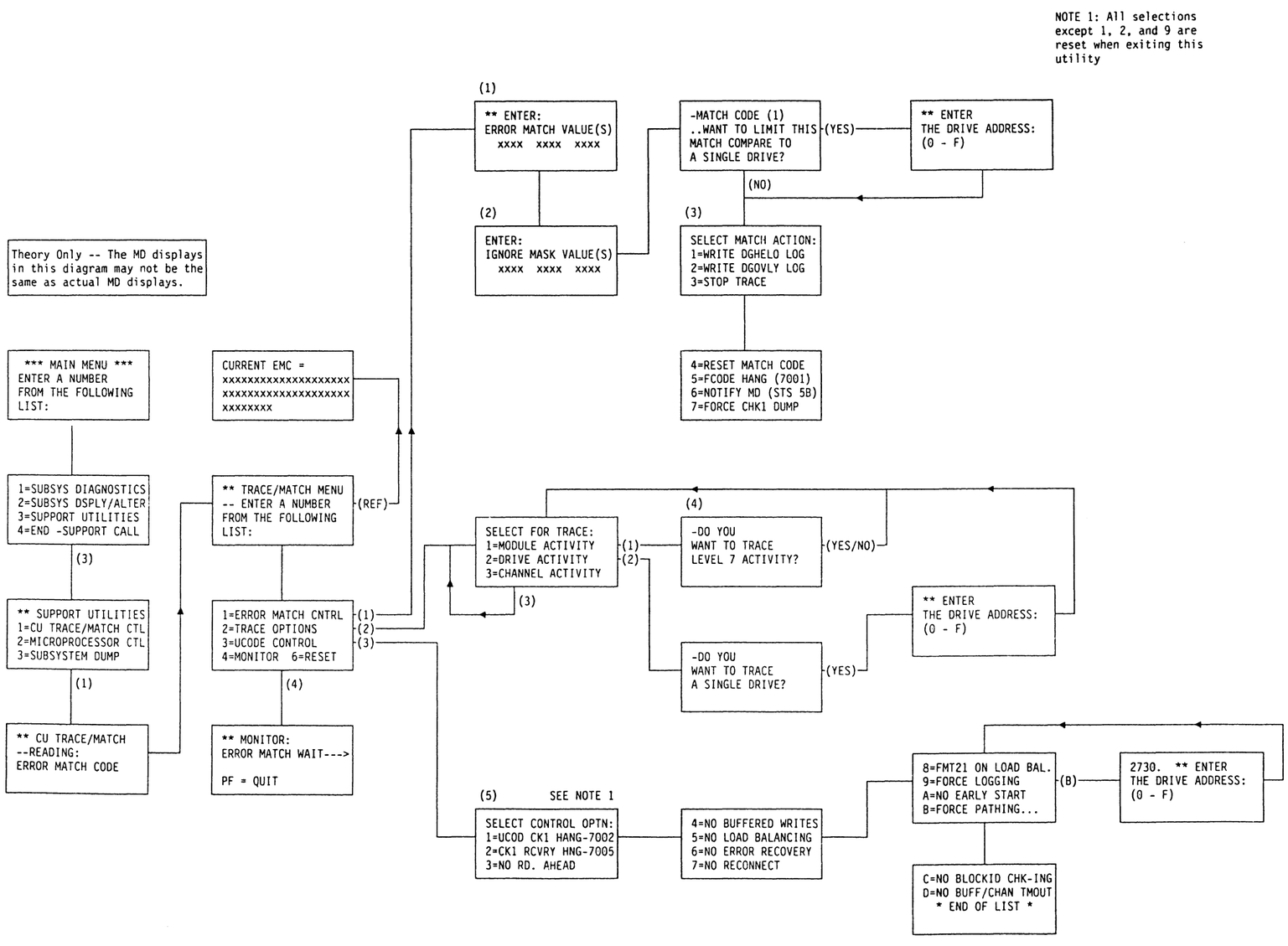
The IML diskette dump file contains information relative to microcode generated or recovered check 1 conditions. Generally speaking, it is historical data.

Dump files taken from control unit storage are files representing current conditions (at time of dump).

Support Utilities (Continued)

Trace/Match Control Diagram

Note: *See the warnings and notes on the facing page to review what effects this program has on the tape subsystem and host system before using trace/match control.*



Trace/Match Control

The Trace/Match Control Utility Program provides prompting for setup data that is used to specify actions to be taken when selected hardware or microprogram errors occur. The match values can be specified for all drives connected to a control unit or limited to a single drive.

After the match values and options have been specified, the MD monitor function can be given control. Its purpose is to wait for a signal from the subsystem that indicates that an error match has occurred. The monitor wait function can be terminated by pressing the PF key on the MD keyboard/display.

A Display Error Match Code command is periodically sent to the functional microcode's diagnostic monitor to detect stops, hangs, or Check 1 errors. If one of these conditions occur, an error message is displayed on the MD keyboard/display.

When a match action, control option, or trace option is asked for, more than one selection can be specified. The selection process is ended by pressing the ENTER key.

Note: When a selection is entered on the trace/match menu, select for trace, select match action, or select control option screens, an asterisk (*) replaces the equal (=) sign on the item line to indicate that the item has been selected.

The following procedure is used to run the trace/match control utility:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 3 (SUPPORT UTILITIES).
4. Enter a 1 (CU TRACE/MATCH CTL) from the support utilities menu screen.
5. Press ENTER after the CU TRACE/MATCH READINGS screen displays.
6. Select one of the following from the trace/match menu screen:

   1 = ERROR MATCH CNTRL
   2 = TRACE OPTIONS
   3 = UCODE CONTROL
   4 = MONITOR
   6 = RESET.

Note: The Error Match codes are reset when the control unit is IML'ed. Switching a control unit online in a dual control unit subsystem will cause its options to be replaced with the options of the online control unit.

Error Match Control

Error Match Value

The error match value **1** is compared to the current microcode error code (current EMC).

Ignore Mask Value

The Trace/Match Control Program ORs this ignore mask value **2** with the error code from the subsystem and the error match value **1**. As a result, any bit that is on in the ignore mask is treated as a don't care bit because the OR operation sets the bit on. If the ignore mask value is hexadecimal FFFF, a match is found for any error code.

An example of the way the ignore mask value works is:

```
Error Match Value    D800    Error Code Value   D8nn
Ignore Mask Value    00FF                       00FF
ORed Value           D8FF                       D8FF
```

In the example, the two ORed values match because the OR function forces the low order bytes to match. Of course, you can set the ignore mask to any value necessary to select the group of error codes you want.

Select Match Action

The Select Match Action screens **3** provide the following selections:

WRITE DGHELO LOG: External registers will be stored when an error code is matched.

WRITE DGOVLY LOG: The sense error history log data will be stored when an error code is matched.

STOP TRACE: All tracing stops when a matching error code is found.

RESET MATCH CODE: The matching "Error Match Code" entry will be reset after a match is found.

FCODE HANG: The microprocessor will hang at 7001 when an error is matched. See note 1.

NOTIFY MD: The microcode alerts the MD via a present status order when the error code is matched.

FORCE CHK1 DUMP: When the error code is matched, a CHK1 dump will be written in the logging area of the IML diskette.

Trace Options

Trace options are provided to permit tracing of the microcode activity if microcode problems are suspected.

Ucode Control

Select Control Options

The Select Control Option screens permit selecting the following options **5**:

Note: Select Control Options affect control unit operations; therefore, all drives will also be affected.

- UCOD CK1 HANG-7002: Will not force a Check 1 error. If a Check 1 error occurs, it will hang at 7002. See Note 1.
- CK1 RCVRY HANG-7005: Forces a Check 1 error and will hang at 7005 before error recovery starts. See Note 2.
- NO RD. AHEAD: No read ahead operations will be done by the control unit. See Note 3.
- NO BUFFERED WRITES: All write commands are interpreted as tape writes. See Note 3.
- NO LOAD BALANCING: This control unit will not initiate a Load Balance, but may receive Load Balance jobs from the other control unit. See Note 3.
- NO ERROR RECOVERY: Error recovery operations will not be activated if an error is detected. See Note 4.
- NO RECONNECT: Use of the reconnect timer (IT0) is inhibited. See Note 3.
- FMT21 ON LOAD BAL: When the FMT21 bit is sent, the buffered log will be off-loaded when a drive is load balanced to the other control unit.
- FORCE LOGGING: Sense data is sent to the host when an error occurs. (See MSG 1 for turn on/off instructions.)
- NO EARLY START: Use of the early start timer (ITD) and device selection over the serial interconnection is inhibited. See Note 3.

- FORCE PATHING: This function forces the subsystem to use this control unit's buffer for the transfer of data to and from a selected drive. The MD prompts the user for the drive address. After the function is active, a flashing message appears on the MD screen.
- NO BLOCKID CHK-ING: Unit checks caused by invalid block IDs detected during read operations are inhibited.

  Warning: This option must never be used in concurrent maintenance mode because data integrity of the subsystem can be affected.

  _____

  _____

  _____

- NO BUFF/CHAN TMOUT: Disables the eight second buffer-channel no activity microcode timer.

Monitor

This function monitors error match conditions that were previously defined in "Error Match Control."

Reset

This function CLEARS/RESETS all Trace Match functions that were previously selected.

Notes:

1. When an error occurs, this option will hang the entire subsystem (non-concurrent maintenance) and can hang the host system waiting for a response from the subsystem.
2. An error will cause the subsystem to hang (non-concurrent maintenance). However, the host system will receive a disconnect and will continue its processing without this subsystem.
3. This option can be used in concurrent maintenance mode, but subsystem performance for drives not under test will be affected.
4. In concurrent maintenance mode, errors normally recovered by the subsystem will be logged by the host as permanent errors. Subsystem performance will not be affected, but host throughput will, because the host will be performing its own error recovery actions more frequently for errors that are normally handled by the subsystem.

0 0 0 0 0 0 0 0 0 0

Trace/Match Control

The Trace/Match Control Utility Program provides prompting for setup data that is used to specify actions to be taken when selected hardware or microprogram errors occur. The match values can be specified for all drives connected to a control unit or limited to a single drive.

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When a match action, control option, or trace option is asked for, more than one selection can be specified. The selection process is ended by pressing the ENTER key.

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5. Press ENTER after the CU TRACE/MATCH READINGS screen displays.
6. Select one of the following from the trace/match menu screen:

   1 = ERROR MATCH CNTRL
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   6 = RESET.

> **Note:** *The Error Match codes are reset when the control unit is IML'ed. Switching a control unit online in a dual control unit subsystem will cause its options to be replaced with the options of the online control unit.*

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Error Match Value	D800	Error Code Value	D8nn
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The Select Match Action screens **3** provide the following selections:

WRITE DGHELO LOG: External registers will be stored when an error code is matched.

WRITE DGOVLY LOG: The sense error history log data will be stored when an error code is matched.

STOP TRACE: All tracing stops when a matching error code is found.

RESET MATCH CODE: The matching "Error Match Code." See Note 1.

NOTIFY MD: The microcode alerts the MD via a present status order when the error code is matched.

FORCE CHK1 DUMP: When the error code is matched, a CHK1 dump will be written in the logging area of the IML diskette.

Trace Options

Trace options are provided to permit tracing of the microcode activity if microcode problems are suspected.

Ucode Control

Select Control Options

The Select Control Option screens permit selecting the following options **5**:

> **Note:** *Select Control Options affect control unit operations; therefore, all drives will also be affected.*

- UCOD CK1 HANG-7002: Will not force a Check 1 error. If a Check 1 error occurs, it will hang at 7002. See Note 1.
- CK1 RCVRY HANG-7005: Forces a Check 1 error and will hang at 7005 before error recovery starts. See Note 2.
- NO RD. AHEAD: No read ahead operations will be done by the control unit. See Note 3.
- NO BUFFERED WRITES: All write commands are interpreted as tape writes. See Note 3.
- NO LOAD BALANCING: This control unit will not initiate a Load Balance, but may receive Load Balance jobs from the other control unit. See Note 3.
- NO ERROR RECOVERY: Error recovery operations will not be activated if an error is detected. See Note 4.
- NO RECONNECT: Use of the reconnect timer (IT0) is inhibited. See Note 3.
- FMT21 ON LOAD BAL: When the FMT21 bit is sent, the buffered log will be off-loaded when a drive is load balanced to the other control unit.
- FORCE LOGGING: Sense data is sent to the host when an error occurs. (See MSG 1 for turn on/off instructions.)
- NO EARLY START: Use of the early start timer (ITD) and device selection over the serial interconnection is inhibited. See Note 3.

- FORCE PATHING: This function forces the subsystem to use this control unit's buffer for the transfer of data to and from a selected drive. The MD prompts the user for the drive address. After the function is active, a flashing message appears on the MD screen.
- NO BLOCKID CHK-ING: Unit checks caused by invalid block IDs detected during read operations are inhibited.

  Warning: This option must never be used in concurrent maintenance mode because data integrity of the subsystem can be affected.

  . . . . . .

  . . . . . .

  . . . . . .

- NO BUFF/CHAN TMOUT: Disables the eight second buffer-channel no activity microcode timer.

Monitor

This function monitors error match conditions that were previously defined in "Error Match Control."

Reset

This function CLEARS/RESETS all Trace Match functions that were previously selected.

Notes:

1. *When an error occurs, this option will hang the entire subsystem (non-concurrent maintenance) and can hang the host system waiting for a response from the subsystem.*
2. *An error will cause the subsystem to hang (non-concurrent maintenance). However, the host system will receive a disconnect and will continue its processing without this subsystem.*
3. *This option can be used in concurrent maintenance mode, but subsystem performance for drives not under test will be affected.*
4. *In concurrent maintenance mode, errors normally recovered by the subsystem will be logged by the host as permanent errors. Subsystem performance will not be affected, but host throughput will, because the host will be performing its own error recovery actions more frequently for errors that are normally handled by the subsystem.*

Support Utilities (Continued)

Microprocessor Control

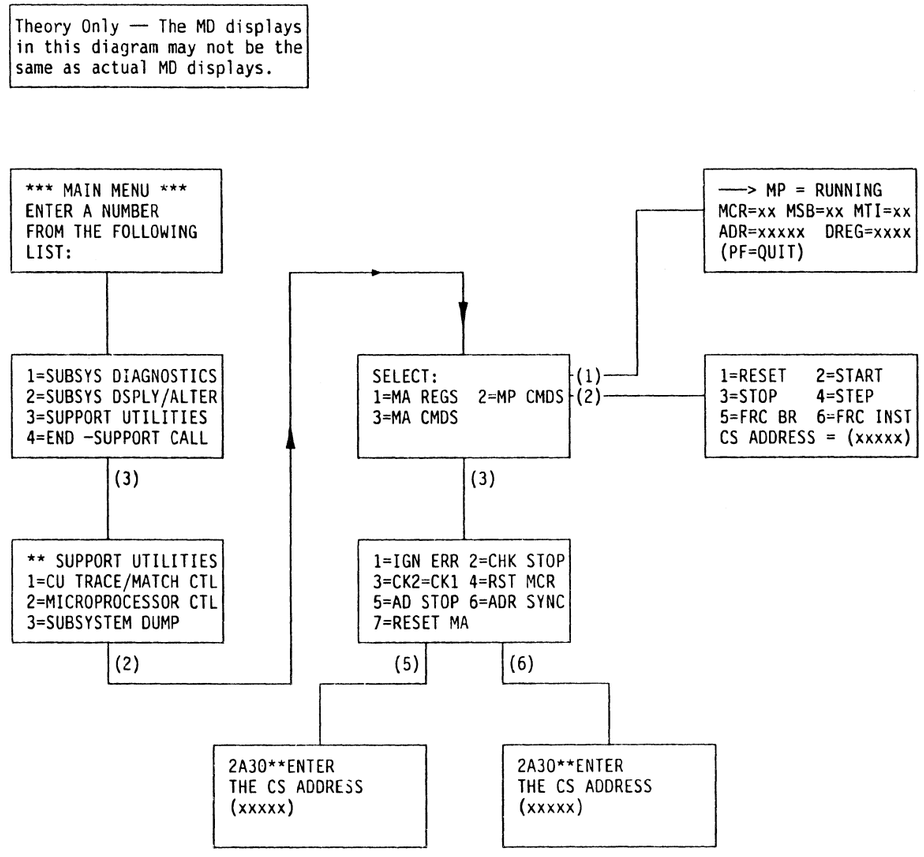
- This utility permits controlling:
  - Maintenance Control Register (MCR)
  - Microprocessor commands
  - Control storage commands
  - Maintenance Adapter commands.
- Host or channel errors may occur if the utility is run during concurrent maintenance mode.

Note: See the warnings on the following page to review what effects this program has on the tape subsystem and host system before using microprocessor control.

The following procedure is used to run the microprocessor control utility:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 3 (SUPPORT UTILITIES).
4. Enter a 2 (MICROPROCESSOR CTL) from the support utilities menu screen.
5. Select one of the following:

   1 = MA REGS - Maintenance Adapter Registers
   2 = MP CMDS - Microprocessor Commands
   3 = MA CMDS - Maintenance Adapter Commands.



Support Utilities (Continued)

The following procedures describe the flow and MD display screen content for each selectable path of the microprocessor control utility. Each path starts at the utility's selection screen.

Display Maintenance Adapter Registers

```
SELECT:
1=MA REGS  2=MP CMDS
3=MA CMDS
```

- Selections:

  1 = Product Maintenance Adapter Registers
  2 = Microprocessor Commands
  3 = Maintenance Adapter Commands

Enter a 1: The following screen displays current MA register status:

```
---> MP = RUNNING
MCR=xx MSB=xx MTI=xx
ADR=xxxx   DREG=xxxx
(PF=QUIT)
```

- ---> MP

  - RUNNING = Microprocessor is executing instructions
  - STOPPED = Microprocessor is stopped

  Note: This display flashes and register content is updated if the microprocessor is running and no error bits are on in the maintenance status byte (MSB) register (bits 4, 5, or 7).

- MCR (Maintenance Control Register)

  Bit 0: Ignore errors
  Bit 1: Address compare stop
  Bit 2: Check Stop
  Bit 3: Check 2 = Check 1
  Bit 4: Address compare sync

- MSB (Maintenance Status Byte)

  Bit 0: Spare
  Bit 1: Status modifier - Always inactive
  Bit 2: Extended Op in progress - MP executing in extended Op.
  Bit 3: Address compare equal - Match between the address entered from the MD and the control storage address.
  Bit 4: Check 1/Processor error - Hard error that affects the integrity of the control unit.
  Bit 5: MP stopped - MP has been stopped by a Check 1 condition or by a Stop MP command from the MD.
  Bit 6: Instruction executed - MP read an instruction from control storage during the last microprocessor cycle.
  Bit 7: Error, MTI data stored - Error data is stored in the MTI register and is available to the MD.

- MTI (Maintenance Tag In)

  Bit 0: MA Request/MA response - Indicates that another byte of information is available to the MP, or that the MA is ready to receive another byte. Also used to acknowledge "MP Status Out" or "Data" received from the MP.
  Bit 1: Data transfer - Active during data transfer to and from the MP.
  Bit 2: MD enabled - MD is on-line and enabled.
  Bit 3: FRU 1 - Microprocessor card
  Bit 4: FRU 2 - External register user card
  Bit 5: FRU 3 - Maintenance adapter card
  Bit 6: FRU 4 - Maintenance device
  Bit 7: Check 1 error recovery - Code currently executing is the result of a Check 1 error.

- ADR: Control program instruction address

- DREG: Control program data register

Microprocessor Commands

```
SELECT:
1=MA REGS  2=MP CMDS
3=MA CMDS
```

Enter a 2: The following screen displays microprocessor command controls:

Warning: The following selections should be used in non-concurrent maintenance mode only.

. . . . . .

. . . . . .

```
1=RESET   2=START
3=STOP    4=STEP
5=FRC BR  6=FRC INST
CS ADDRESS = (xxxx)
```

- RESET: Resets the MP and forces a level 0 interrupt.

- START: Starts the MP at the next logical instruction.

- STOP: Stops the MP. Must be done before force branch, force instruction, step, control storage, reset, or MA commands can be used.

- STEP: Allows MP to run in a single instruction mode.

- FRC BR (Force Branch): Transfers control to the address loaded in the MA data register.

- FRC INST (Force Instruction): Puts the instruction loaded in the data register on the data bus. MP may be stepped to execute the instruction.

- CS ADDRESS: Displays the control storage address that was current at the time the menu displayed.

Support Utilities (Continued)

Maintenance Adapter Commands

```
SELECT:
1=MA REGS  2=MP CMDS
3=MA CMDS
```

Enter a 3: The following screen displays MA command controls:

Warning: The following selections should be used in non-concurrent maintenance mode only (except ADR SYNC and RESET MA).

. . . . . .

. . . . . .

. . . . . .

```
1=IGN ERR 2=CHK STOP
3=CK2=CK1 4=RST MCR
5=AD STOP 6=ADR SYNC
7=RESET MA
```

- IGN ERR: Ignore error
  - Prevents the microprocessor from stopping when a hard (Check 1) error is detected
  - Turns MCR bit 0 on
- CHK STOP: Check stop
  - Prevents the microprocessor from restarting after a Check 1 error
  - Turns MCR bit 2 on
- CHK2=CHK1: Check 2 = Check 1
  - Allows a Check 2 error to be handled as a Check 1 error
  - Turns MCR bit 3 on
- RST MCR: Reset Maintenance Control Register
  - Resets all MCR bits
- AD STOP: Address Stop
  - Causes the microprocessor to stop when the address compare equal latch comes on
  - Turns MCR bit 1 on
- ADR SYNC: Address Synchronize
  - Turns MSB bit 3 on when the address compare equal latch comes on when the address selected is executed.
  - Causes a sync pulse to be generated on the '+ Address Compare Signal' line (MA003, 01A A1E2 Z12) when the address selected is executed.
  - Microprocessor does not stop.
- RESET MA: Reset Maintenance Adapter
  - Resets the ignore error, check 2 equals check 1, and check stop bits in the maintenance control register (MCR)
  - Resets the maintenance tag in (MTI) register
  - Resets the force-branch function
  - Resets the maintenance adapter level 0 interrupt request

Support Utilities

Subsystem Dump

Dump files may be created for the control unit, the drive or from the CHK1DMP file on the IML diskette. This interactive utility will assembly the data from the selected area and move it to the MD support diskette. Dump functions are available in the concurrent (microcode operational and running) or non-concurrent modes (microcode stopped or hung). The CHK1DMP file from the IML diskette is only available in the concurrent mode. The MD will automatically try the concurrent mode first as this mode is faster and then default to the non-concurrent mode.

If a file (CHK1DMP) exists on the IML diskette, the MD will request an offline drive to perform the dump process. This is required for the microcode to allocate interrupts for maintenance purposes.

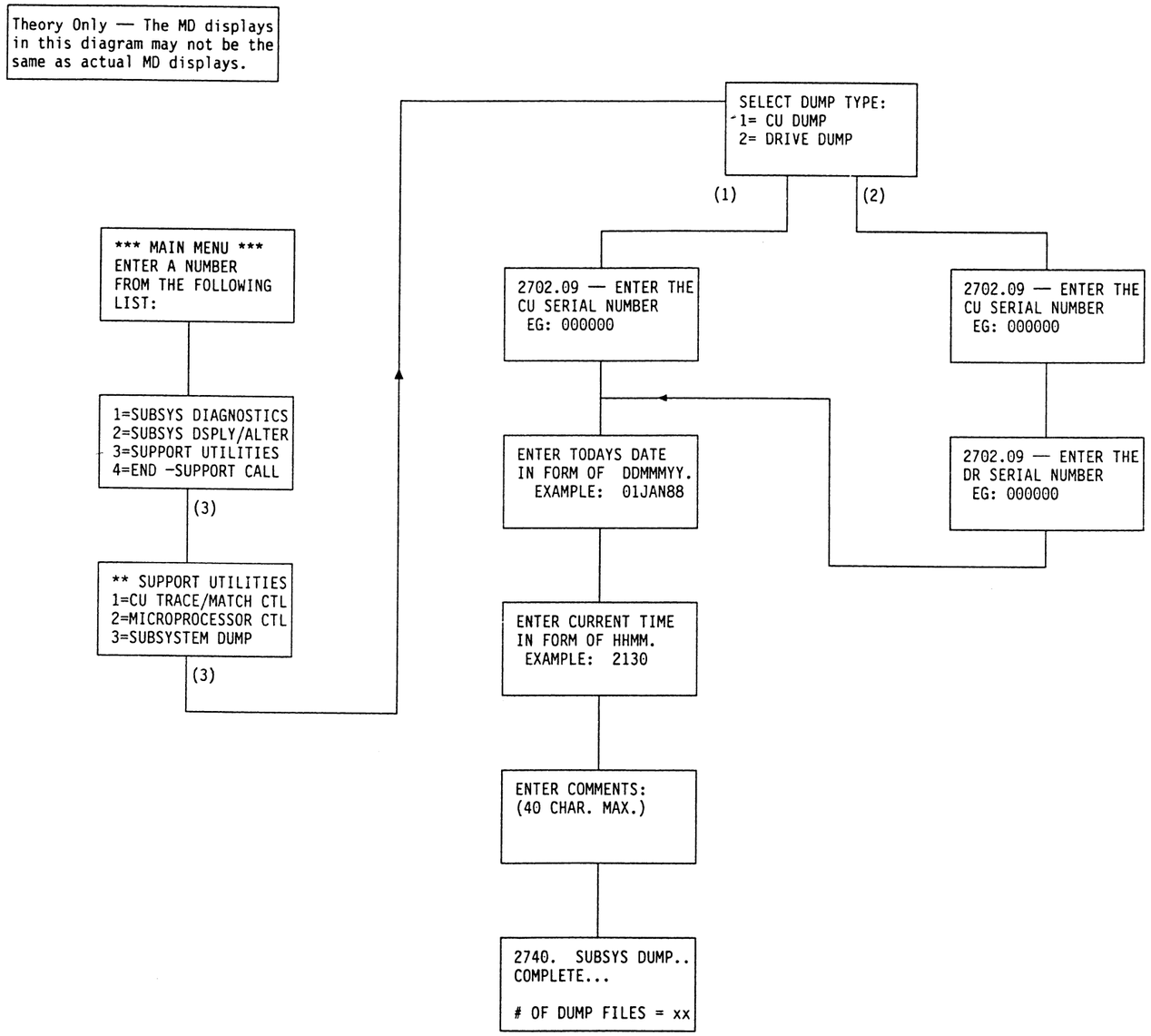
Multiple dump files may be taken and stored on the MD diskette. An error message will display if the dump area is full. The user may then choose to overwrite (destroy) existing dump files. The MD creates a dump header file which defines the actual location of the dump data on the diskette.

The following procedure is used to run the subsystem dump utility:

1. Insert and IPL the support diskette.
2. Press ENTER until the main menu selection screen displays.
3. Enter a 3 (SUPPORT UTILITIES).
4. Enter a 3 (SUBSYSTEM DUMP) from the support utilities menu.
5. Select the type of dump needed.

   1 = Control unit storage dump
   2 = Drive storage dump

6. Follow instructions provided by the MD.



Notes SDISK 170

Notes SDISK 170

Contents

Subsystem Diagnostics

The subsystem diagnostics exercise the subsystem. Four sets of diagnostic exercisers are available:

- Drive command exerciser
- MD/MA diagnostic
- Basic CU Test
- Support diagnostics.

You can be directed to run particular subsystem diagnostics by some other part of this Maintenance Information, for example, from the EAD section or the FSI section. Or you can select diagnostics from what is known about the problem.

Drive Command Exerciser

The drive command exerciser is a group of programs on the support diskette that permits you to enter and perform chains of tape drive commands. The drive command exerciser operates in concurrent maintenance mode.

The chains of commands can be used to isolate drive motion problems or failures caused by a particular sequence of commands. You can use either of two sequences of commands that have already been selected, or you can make your own sequence. The commands are entered from the maintenance device keyboard/display.

See "Drive Command Exerciser" on DIAG 1 to find detailed information about how to use the drive command exerciser.

MD/MA Diagnostic

The maintenance device/maintenance adapter diagnostic tests the part of the maintenance adapter card that connects to the MD and tests the communication path between the MD and the maintenance adapter card. You can use this diagnostic when:

- The MD does not seem to communicate with the control unit.
- The maintenance adapter card has been replaced.

See "Maintenance Device/Maintenance Adapter Diagnostic" on DIAG 1 for detailed information about the MD/MA diagnostic.

Basic CU Test

The basic control unit test verifies:

- The correct function of the maintenance adapter connections to the processor and control store
- The control unit's ability to execute the microcode and forces the executing of the ROS control store checkout.

You can use this diagnostic to verify correct subsystem operation after the maintenance adapter, processor, or control store cards have been replaced. See "Basic Control Unit Test" on DIAG 1 for detailed information.

Support Diagnostics

The support diagnostics are microprograms that can operate the different parts of the subsystem independently of the subsystem command operation. That is, the diagnostics:

- Consist of microcode
- Replace the functional microcode
- Test the parts of the subsystem.

Because they replace the functional microcode, the support diagnostics cannot be used for concurrent maintenance in a single-control-unit subsystem. In a dual control unit subsystem, those support diagnostics that test only the internal control unit can be run on one control unit while the other control unit continues to operate with the host processor. Subsystem diagnostics that test the interconnections between control units or that test the interconnections between the control unit and the tape units cannot be used for concurrent maintenance on a dual control unit subsystem. You can use the support diagnostics when:

- The error analysis diagram or FSI section calls for the diagnostic
- The product maintenance package does not fix a problem
- You finish installation
- Unless indicated in a specific diagnostic, the contents of external registers may differ from the original diagnostic display.

How the Support Diagnostics Are Organized

The support diagnostics test many parts of the subsystem. Because you may not need to test everything in the subsystem, the support diagnostics are divided into sections and routines. The sections and routines can be selected to test only those parts of the subsystem that are suspected of failing.

Diagnostic routines and diagnostic sections are identified by an identification code of EE plus a hexadecimal number. An E010 is also assigned that runs a basic set of diagnostics that can be run without disturbing a dual control unit subsystem.

Diagnostic Sections

Diagnostic sections consist of a group of diagnostic routines that run in sequence. The sequences test particular areas of the subsystem, such as the control unit data flow, the control unit to magnetic tape drive interconnections, or the control unit buffer. The diagnostic sections are useful when a general area is suspected, but the specific function that may be failing within that area is not known.

Diagnostic Routines

Diagnostic routines are the actual sets of microcode instructions that perform tests on the parts of the subsystem. Some, but not all, diagnostic routines can be called by diagnostic sections.

Diagnostic Identification Code

The table on DIAG 3 lists the identification code, the page on which detailed explanations of the diagnostic sections and routines begin, and the purpose of each diagnostic section or routine. Also listed are the approximate run times, failure ID examples for each routine, and prerequisite diagnostics. In addition the table shows whether the routine or section can be run in one control unit of a dual control unit subsystem while the other control unit operates with the host processor (Type 1) or whether the *complete subsystem* must be offline to run the diagnostic (Type 2). Note that even Type 1 sections and routines require you to take the subsystem offline to run support diagnostics in a single-control-unit subsystem. Use this table to select the identification code you want to use if you were not sent to a particular diagnostic by another part of the maintenance package.

E010 — CU Functions Test

This identification code causes the diagnostic control program to run the diagnostic routines that test the internal circuits of the control units. It does not test the tape units themselves and does not test those circuits that can interfere with operations of a dual control unit subsystem. This identification code can be used on one control unit of a dual control unit subsystem while the other control unit operates with the host processor.

E010 runs control unit and tape unit data path diagnostic routines in the following order: EE12, EE13, EE14, EE32, EE33, EE52, EE53, EE64, EE85, EE92, and EE93.

When E010 runs, the diagnostic routines included in E010 use their built in defaults. Parameter entries such as channel and drive addresses and pattern numbers are neither required nor allowed.

To rerun E010, use option 1 (RESTART DIAG.) on the DIAG.11 screen.

Note: You must take both control units offline (thus making the *complete subsystem* unavailable to the customer) to run any support diagnostic routines that are not included in E010, except for channel wrap diagnostic routine EE62 (see instructions for setup).

EE10 — Processor Basic Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE30 — Data Buffer Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE40 — Control Unit to Drive Test

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE50 — Data Path Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE60 — Channel Adapter Test

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE90 — Status Store Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EEA0 — Tape Movement Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

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- The maintenance adapter card has been replaced.

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The support diagnostics are microprograms that can operate the different parts of the subsystem independently of the subsystem command operation. That is, the diagnostics:

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Because they replace the functional microcode, the support diagnostics cannot be used for concurrent maintenance in a single-control-unit subsystem. In a dual control unit subsystem, those support diagnostics that test only the internal control unit can be run on one control unit while the other control unit continues to operate with the host processor. Subsystem diagnostics that test the interconnections between control units or that test the interconnections between the control unit and the tape units cannot be used for concurrent maintenance on a dual control unit subsystem. You can use the support diagnostics when:

- The error analysis diagram or FSI section calls for the diagnostic
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How the Support Diagnostics Are Organized

The support diagnostics test many parts of the subsystem. Because you may not need to test everything in the subsystem, the support diagnostics are divided into sections and routines. The sections and routines can be selected to test only those parts of the subsystem that are suspected of failing.

Diagnostic routines and diagnostic sections are identified by an identification code of EE plus a hexadecimal number. An E010 is also assigned that runs a basic set of diagnostics that can be run without disturbing a dual control unit subsystem.

Diagnostic Sections

Diagnostic sections consist of a group of diagnostic routines that run in sequence. The sequences test particular areas of the subsystem, such as the control unit data flow, the control unit to magnetic tape drive interconnections, or the control unit buffer. The diagnostic sections are useful when a general area is suspected, but the specific function that may be failing within that area is not known.

Note: Loop until error is the only available option for this section.

Diagnostic Routines

Diagnostic routines are the actual sets of microcode instructions that perform tests on the parts of the subsystem. Some, but not all, diagnostic routines can be called by diagnostic sections.

Note: Loop until error, and loop and bypass error are the only available options for this routine.

Diagnostic Identification Code

The table on DIAG 3 lists the identification code, the page on which detailed explanations of the diagnostic sections and routines begin, and the purpose of each diagnostic section or routine. Also listed are the approximate run times, failure ID examples for each routine, and prerequisite diagnostics. In addition the table shows whether the routine or section can be run in one control unit of a dual control unit subsystem while the other control unit operates with the host processor (Type 1) or whether the *complete subsystem* must be offline to run the diagnostic (Type 2). Note that even Type 1 sections and routines require you to take the subsystem offline to run support diagnostics in a single-control-unit subsystem. Use this table to select the identification code you want to use if you were not sent to a particular diagnostic by another part of the maintenance package.

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This identification code causes the diagnostic control program to run the diagnostic routines that test the internal circuits of the control units. It does not test the tape units themselves and does not test those circuits that can interfere with operations of a dual control unit subsystem. This identification code can be used on one control unit of a dual control unit subsystem while the other control unit operates with the host processor.

E010 runs control unit and tape unit data path diagnostic routines in the following order: EE12, EE13, EE14, EE32, EE33, EE52, EE53, EE64, EE85, EE92, and EE93.

When E010 runs, the diagnostic routines included in E010 use their built in defaults. Parameter entries such as channel and drive addresses and pattern numbers are neither required nor allowed.

To rerun E010, use option 1 (RESTART DIAG.) on the DIAG.11 screen.

Note: You must take both control units offline (thus making the *complete subsystem* unavailable to the customer) to run any support diagnostic routines that are not included in E010, except for channel wrap diagnostic routine EE62 (see instructions for setup).

EE10 — Processor Basic Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE30 — Data Buffer and Buffer Adapter Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3. The Improved Data Recording Capability tests run automatically if the Improved Data Recording Capability feature is installed.

EE40 — Control Unit to Drive Test

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE50 — Data Path Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE60 — Channel Adapter Test

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EE90 — Status Store Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

EEA0 — Tape Movement Tests

For control options, see the individual routines listed under this diagnostic section on DIAG 3.

0 0 0 0 0 0 0 0 0 0

Diagnostic Identification Code Table

ID Code *	Page	Type (See Note)	Purpose	Load and Run Times (Approximate)	Failure ID Example	Prerequisite Diagnostics **
(MD/MA)	DIAG 20	1	Maintenance Device/Maintenance Adapter Diagnostic. (MD/MA)	10 seconds	MD10xx	None
(BCU)	DIAG 30	1	Basic control unit test. CU functions test, diagnostic section. Runs diagnostic routines EE12, EE13, EE14, EE32, EE33, EE52, EE53, EE64, EE85, EE92, and EE93.	5 minutes	CB10xx	None
EE10		1	Processor basic tests, diagnostic section. Runs routines EE12, EE13, EE14, and EE85.	1 minute and 5 seconds		BCU
EE12	DIAG 50	1	Processor function test.	18 seconds	HC20xx	BCU
EE13	DIAG 55	1	Interrupt level test.	18 seconds	HC30xx	BCU, EE12
EE14	DIAG 65	1	Processor external register test.	18 seconds	HC40xx	BCU, EE12, EE13
EE15	DIAG 70	1	CAF wrap test.	45 seconds	KL 4021	EE14
EE20			Reserved.			
EE30		1	Data buffer tests, diagnostic section. Runs routines EE32 and EE33.	42 seconds		BCU, EE10
EE32	DIAG 100	1	Data buffer data path test.	1 minute 30 seconds	BU20xx	BCU, EE10
EE33	DIAG 110	1	Data buffer controls.	40 seconds	BU30xx	BCU, EE10, EE32
EE40		2	Control Unit to drive tests, diagnostic section. Runs routines EE42, EE43, and EE44.	2 minutes (16 drives)		BCU
EE42	DIAG 150	2	Control Unit to drive bus out and driver wrap test.	18 seconds	DI20xx	BCU
EE43	DIAG 160	2	Control Unit to drive bus and tag test.	19 seconds	DI30xx	BCU, EE42
EE44	DIAG 170	2	Control Unit to drive serial test.	1 minute and 23 seconds (16 drives)	DI40xx	BCU, EE42, EE43
EE50		2	Data path tests, diagnostic section. Runs routines EE52, EE53, and EE54.	54 seconds		EE10, BCU, EE30, EE40
EE52	DIAG 200	1	Short loop write to read pattern test.	18 seconds	LW20xx	BCU, EE10, EE30
EE53	DIAG 218	1	Short loop write to read timing test.	18 seconds	LW30xx	BCU, EE10, EE30, EE52
EE54	DIAG 220	2	Long loop write to read test.	18 seconds	LW40xx	BCU, EE10, EE30, EE52, EE53, EE40
EE60			Channel Adapter test, diagnostic section. Runs routine EE64.			BCU, EE10, EE30
EE62	DIAG 300	3	Channel interface wrap test.	45 seconds	CI20xx	BCU, EE10, EE30, EE64
EE64	DIAG 320	1	Channel Adapter function test.	51 seconds	CI40xx	BCU, EE10, EE30
EE70			Reserved.			

ID Code *	Page	Type (See Note)	Purpose	Load and Run Times (Approximate)	Failure ID Example	Prerequisite Diagnostics **
EE72			Reserved.			
EE85	DIAG 400	1	External register bus addressing and data pattern test.	19 seconds	XB50xx	BCU, EE12, EE13, EE14
EE90		1	Status store tests, diagnostic section. Runs routines EE92 and EE93.	36 seconds		BCU, EE10
EE92	DIAG 450	1	Status store wrt/rd RAM storage test.	18 seconds	SS20xx	BCU, EE10
EE93	DIAG 460	1	Status store order test.	18 seconds	SS30xx	BCU, EE10, EE92
EEA0		2	Tape movement tests, diagnostic section. Runs routines EEA2, EEA3, and EEA4.	7 minutes and 30 seconds		BCU, EE40, EE10
EEA2	DIAG 500	2	Basic tape motion test.	18 seconds	TM20xx	BCU, EE40, EE10
EEA3	DIAG 510	2	Write/Read Exerciser.	3 minutes and 47 seconds	TM30xx	BCU, EE40, EE10, EEA2
EEA4	DIAG 550	2	Write/Read Exerciser.	4 minutes and 30 seconds	TM60xx	BCU, EE40, EE10, EEA2
EEF0	DIAG 600	2	Scope loop utility.	Continuous		None.
(EEF1)	DIAG 620	Not Applicable	Drive Patch Load Utility.	Not Applicable	None.	None.

Note: Single Control Unit Subsystems

- Type 1 and 2 Diagnostics
  - The subsystem must be taken offline and made unavailable for customer use.
- Type 3 Diagnostics
  - The host processor channel cables must be disconnected before running this diagnostic.

Dual Control Unit Subsystems

- Type 1 Diagnostics
  - Diagnostics can run in one control unit while the other control unit operates with the host processor.
- Type 2 Diagnostics
  - The complete subsystem must be taken offline and made unavailable for customer use. Due to drive interface interaction, run diagnostics from only one MD at a time.
- Type 3 Diagnostics
  - The host processor channel cables must be disconnected before running this diagnostic.
  - Diagnostics can run in one control unit while the other control unit operates with the host processor.

* ID codes within parenthesis cannot be used for diagnostic selection.

** The prerequisite diagnostics for a routine must be run, in the correct order, and error free.

0 0 0 0 0 0 0 0 0 0

Diagnostic Identification Code Table

ID Code *	Page	Type (See Note)	Purpose	Load and Run Times (Approximate)	Failure ID Example	Prerequisite Diagnostics **
(MD/MA)	DIAG 20	1	Maintenance Device/Maintenance Adapter Diagnostic. (MD/MA) EE12, EE13, EE14, EE32, EE33, EE52, EE53, EE64, EE85, EE92, and EE93. See "E010 – CU Functions Test."	2 minutes		BCU
EE10		1	Processor basic tests, diagnostic section. Runs routines EE12, EE13, EE14, and EE85.	1 minute and 5 seconds		BCU
EE12	DIAG 50	1	Processor function test.	18 seconds	HC20xx	BCU
EE13	DIAG 55	1	Interrupt level test.	18 seconds	HC30xx	BCU, EE12
EE14	DIAG 65	1	Processor external register test.	18 seconds	HC40xx	BCU, EE12, EE13
EE20			Reserved.			
EE30		1	Data buffer tests, diagnostic section. Runs routines EE32 and EE33.	42 seconds		BCU, EE10
EE32	DIAG 100	1	Data buffer data path test.	34 seconds	BU20xx	BCU, EE10
EE33	DIAG 110	1	Data buffer controls test.	24 seconds	BU30xx	BCU, EE10, EE32
EE40		2	Control Unit to drive tests, diagnostic section. Runs routines EE42, EE43, and EE44.	2 minutes (16 drives)		BCU
EE42	DIAG 150	2	Control Unit to drive bus out and driver wrap test.	18 seconds	DI20xx	BCU
EE43	DIAG 160	2	Control Unit to drive bus and tag test.	19 seconds	DI30xx	BCU, EE42
EE44	DIAG 170	2	Control Unit to drive serial test.	1 minute and 23 seconds (16 drives)	DI40xx	BCU, EE42, EE43
EE50		2	Data path tests, diagnostic section. Runs routines EE52, EE53, and EE54.	54 seconds		EE10, BCU, EE30, EE40
EE52	DIAG 200	1	Short loop write to read pattern test.	18 seconds	LW20xx	BCU, EE10, EE30
EE53	DIAG 218	1	Short loop write to read timing test.	18 seconds	LW30xx	BCU, EE10, EE30, EE52
EE54	DIAG 220	2	Long loop write to read test.	18 seconds	LW40xx	BCU, EE10, EE30, EE52, EE53, EE40
EE60			Channel Adapter test, diagnostic section. Runs routine EE64.			BCU, EE10, EE30
EE62	DIAG 300	3	Channel interface wrap test.	45 seconds	CI20xx	BCU, EE10, EE30, EE64
EE64	DIAG 320	1	Channel Adapter function test.	51 seconds	CI40xx	BCU, EE10, EE30
EE70			Reserved.			
EE72			Reserved.			
EE85	DIAG 400	1	External register bus addressing and data pattern test.	19 seconds	XB50xx	BCU, EE12 EE13, EE14
EE90		1	Status store tests, diagnostic section. Runs routines EE92 and EE93.	36 seconds		BCU, EE10
EE92	DIAG 450	1	Status store wrt/rd RAM storage test.	18 seconds	SS20xx	BCU, EE10
EE93	DIAG 460	1	Status store order test.	18 seconds	SS30xx	BCU, EE10, EE92
EEA0		2	Tape movement tests, diagnostic section. Runs routines EEA2, EEA3, and EEA4.	7 minutes and 30 seconds		BCU, EE40, EE10
EEA2	DIAG 500	2	Basic tape motion test.	18 seconds	TM20xx	BCU, EE40, EE10

ID Code *	Page	Type (See Note)	Purpose	Load and Run Times (Approximate)	Failure ID Example	Prerequisite Diagnostics **
EEA3	DIAG 510	2	Write/Read Exerciser.	3 minutes and 47 seconds	TM30xx	BCU, EE40, EE10, EEA2
EEA4	DIAG 550	2	Write/Read Exerciser.	4 minutes and 30 seconds	TM60xx	BCU, EE40, EE10, EEA2
EEF0	DIAG 600	2	Scope loop utility.	Continuous		None.
(EEF1)	DIAG 620	Not Applicable	Drive Patch Load Utility.	Not Applicable	None.	None.

Note: Single Control Unit Subsystems

- Type 1 and 2 Diagnostics
  - The subsystem must be taken offline and made unavailable for customer use.
- Type 3 Diagnostics
  - The host processor channel cables must be disconnected before running this diagnostic.

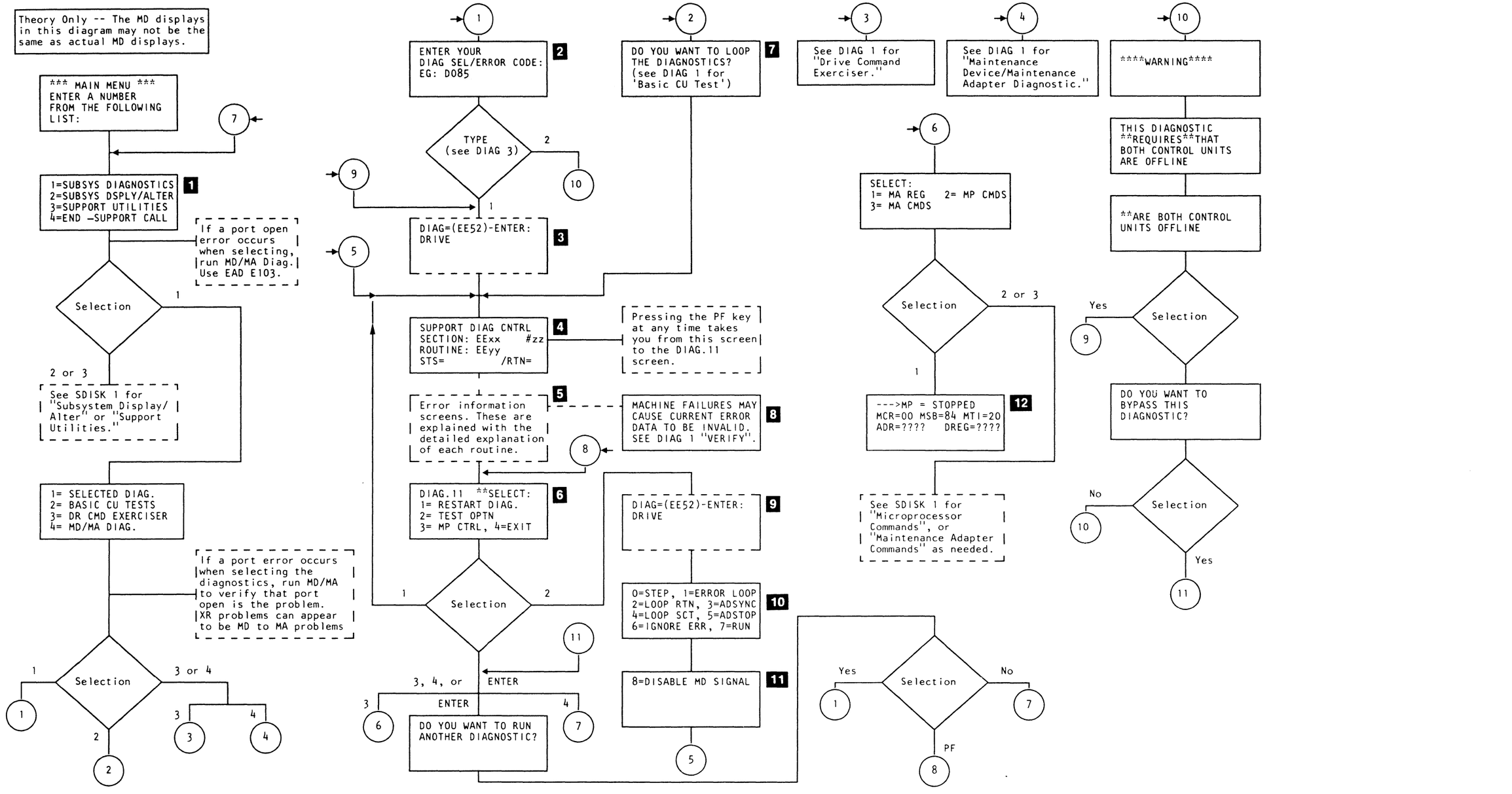
Dual Control Unit Subsystems

- Type 1 Diagnostics
  - Diagnostics can run in one control unit while the other control unit operates with the host processor.
- Type 2 Diagnostics
  - The complete subsystem must be taken offline and made unavailable for customer use. Due to drive interface interaction, run diagnostics from only one MD at a time.
- Type 3 Diagnostics
  - The host processor channel cables must be disconnected before running this diagnostic.
  - Diagnostics can run in one control unit while the other control unit operates with the host processor.

* ID codes within parenthesis cannot be used for diagnostic selection.

** The prerequisite diagnostics for a routine must be run, in the correct order, and error free.

How to Use the Support Diagnostics DIAG 4



Support Diagnostic Flow

The flowchart on DIAG 4 shows the order of proceeding through the support diagnostics. It does not show all the menus because many of the menus are self-explanatory. The flowchart is keyed to the text on this and the next two pages. The test explains what the screens mean and gives some suggestions about how to interpret them.

To use the support diagnostics, you must know:

- How the diagnostic programs are controlled.
- How to run the diagnostics for single-control-unit subsystems and for dual-control-unit subsystems.
- What information the diagnostics will supply to you, and how to use it.
- How to verify error data that may not be valid.
- What options you have for controlling the diagnostics.
- How to end use of the diagnostics.

Control of the Support Diagnostics

The diagnostic control program in the MD controls the running of the support diagnostics. To permit you to control the way the MD runs the diagnostics, the MD presents screens on the keyboard/display and reacts to your entries from the keyboard.

After you have made your selections, the diagnostic control program selects the diagnostic routines and controls the order in which they run. You can control which routines are run and the order in which they run by entering:

- A diagnostic section identification code
- A diagnostic routine identification code
- An error code
- A fault symptom code (FSC).

You can get the error code from:

- The drive display
- The operator's console printout
- EREP
- OLT.

You can get the fault symptom code from the MD keyboard/display.

If you enter an error code or a fault symptom code (FSC), the diagnostic control program selects diagnostic routines appropriate for that error code.

When the routine has been selected, the MD replaces the functional microcode in the control unit with the diagnostic routine microcode. Because the diagnostic routine microcode replaces the functional microcode, you cannot perform concurrent maintenance using the support diagnostics.

Note: Once the diagnostic microcode has been loaded, you must perform an IML on that control unit before normal operation can be started again.

Running Support Diagnostics

In the following discussions, the reference keys refer to the flowchart on DIAG 4.

Note: When you are through running the diagnostics:

- Put the Normal/Test switch in the Normal position.
- Put the channel Enable/Disable switch in the Enable position.
- Follow the instructions in "How to End Use of the Diagnostics," located on DIAG 7, before putting the CU Offline/CU Online switch in the CU Online position.

Single-Control-Unit Subsystem

Use this procedure when you run the diagnostics on a single-control-unit subsystem or when you run the basic control unit tests (E010) on a dual-control-unit subsystem.

1. Set the CU Offline/CU Online switch to CU Offline.
2. Now you are ready to run the support diagnostics.

Dual-Control-Unit Subsystem

Use this procedure when you run any support diagnostic other than those included in the basic control unit tests (E010) on a dual-control-unit subsystem.

1. Set the CU Offline/CU Online switch to CU Offline on both control units.
2. On the control unit with the MD not attached, set the Normal/Test switch to Test and press the IML switch. (This causes the control unit to stop and avoids interference with the drives while the diagnostics run from the other control unit.)
3. On the control unit with the MD attached, set the Normal/Test switch to Normal.
4. Now you are ready to run the support diagnostics.

Getting the Diagnostics Running

Connect the MD to the control unit that is to be tested, and begin using the support diskette as explained in the SDISK section of this maintenance information. Select the option of using diagnostics by selecting option 1 from the main menu **1**.

When the diagnostic is in the process of loading from the diskette and storing into control storage, problems can interfere with the communications between the control unit and the MD, causing 'Fast Load' to stop. The control program then displays a screen asking 'PMA FORCE LOAD IT'.

- A **Yes** response causes a 'Slow Load' of the diagnostics
- A **No** response causes a return to **1**.

You may run 'Basic CU Test', see E010 on DIAG 3.

Controlling the Diagnostics

The diagnostics supply two controls at the start of the diagnostics and several control options when the diagnostic finishes the first pass.

Controls at the Start of the Diagnostics

When you start running the Basic CU tests, the diagnostic control program lets you select whether to loop the diagnostics **7**. If you choose to loop the diagnostics, the diagnostics loop until an error occurs.

When you choose to run selected diagnostics, the diagnostic control program lets you specify the diagnostics to be run. You enter your selection on a diagnostic selection menu **2**. You can enter the identification code for a diagnostic section or a diagnostic routine, or you can enter an error code or a fault symptom code. Following the selection of certain diagnostic sections or diagnostic routines, you can select the drive, channel, and test pattern that you want to use **3** **9**.

Controls at the End of the First Pass

When the diagnostic stops, either because of an error or because it ran without errors, you can select from a number of options. The first menu **6** permits you to select changes in the way the diagnostic is running or to look at certain information. If you want to change the control options for the diagnostic (selection 2), you can get the drive, channel, and pattern selection menu **3** **9**, and you get the test options menu **10** **11**. The selections from the test options menu cause the following results.

The last routine (of a section), will be the first routine run when an option, drive address, channel address, or test pattern is changed.

Option	Result
STEP	Permits stepping through a diagnostic section by stopping at the end of each diagnostic routine. Each time the ENTER key on the MD keyboard/display is pressed, the next diagnostic routine runs. You can also use this option with the loop routine option to stop the routine after each run.
ERROR LOOP	Causes the diagnostic routine to run to the point of error and then restart the test. The routine loops until the PF key on the MD keyboard/display is pressed. Error loop causes the routine to loop if no errors are detected.
LOOP RTN	Loop routine. Causes the last routine run to restart and loop until the MD keyboard/display PF key is pressed. If an error is detected, the loop ends and an error screen is displayed unless IGNORE ERR has also been selected.
ADSYNC	Address sync. Permits entering an address for oscilloscope synchronization.
LOOP SCT	Loop section. Permits looping a section of one or more diagnostic routines. Looping continues until an error is detected or the PF key on the MD keyboard/display is pressed.
ADSTOP	Address stop. Causes the microprogram in progress to stop when the storage address you have entered is reached.
IGNORE ERR	Ignore error. Disables the check 1 error stop. If this option is used at the same time as the loop routine option, the routine restarts when an error occurs.
DISABLE MD SIGNAL	Ends diagnostic to MD signalling. This option can be used with the ADSYNC and LOOP RTN options to increase the oscilloscope triggering rate.
RUN	This option starts the diagnostic operating under the conditions that you have established with your other option selections. This option must be entered as the last option selected. The last routine (of a section), will be the first routine run when an option, drive address, channel address, or test pattern is changed.

Information Supplied by the Support Diagnostics

The support diagnostics supply three kinds of information:

- A status screen
- Error screens
- Common stop addresses

Status Screen

When a diagnostic routine is running or ends, with or without an error, the status screen **4** (see DIAG 4) displays. If the routine did not have an error and more than one routine is to run, the screen displays only momentarily, then it is replaced with the loading screen from the next routine. If an error occurred or no more screens are to run, the diagnostic stops with the status screen displayed. The status screen displays:

- SECTION = The name of the diagnostic section
- ROUTINE = The name of the diagnostic routine
- # = Control options

  ZZ No options

  EL Error loop

  LR Loop routine

  IE Ignore errors

  EI Error loop and ignore errors

  LI Loop routine and ignore errors

  AD Address sync

  EA Error loop and address sync

  LA Loop routine and address sync

  AI Address sync and ignore errors

  EX Error loop and address sync and ignore errors

  LX Loop routine and address sync and ignore errors.

- STS = Status of diagnostics

  RUNNING Diagnostics running

  STOPPED Diagnostics stopped

  CK1STOP Check 1 error, stopped

  LOOPING Diagnostic looping

  ERROR Error has occurred (see note 1)

  GOOD Diagnostic complete with no errors

  DATA(XX) Expected data, actual data is shown in the /RTN field

  PGMFLAG Program flag

  MTIERR Maintenance-tags-in error (see note 1)

  LOOPREQ Error loop request

  CHECK1 Check 1 error, not stopped (see note 1)

- /RET = Return code

  40 Good return

  03 Error

  ... Press ENTER for message from the diagnostic

Note 1:
- If STS = DATA(XX), /RTN = actual byte received.
- If STS = CK1STOP or CHECK1, /RTN = maintenance status byte (MSB) (see note 2).
- If STS = MTIERR, /RTN = maintenance tags in (MTI) (see note 2).
- If STS = PGMFLAG, /RTN =
  - 80 = Loop routine (diagnostic)
  - 40 = Loop on error
  - 20 = Ignore error.

Note 2:
- See "Error Screens" if no screens are available.
- See EAD 1 for E100 or Fnnn.

Error Screens

In addition to the status screen, each diagnostic can supply you with error screens **5** (see DIAG 4). The error screens follow the status screen only if an error occurred. The error screens are made for the particular diagnostic, so they are explained in the description of each diagnostic.

Common Stop Addresses

When a diagnostic routine completes its run, it branches to a stop address. The stop addresses supply diagnostic test result indications.

To obtain the stop address at which a diagnostic routine has stopped, you must select 3 from the DIAG.11 screen **6** (see DIAG 4) and display the MA REGS. The address shown on the MP = STOPPED screen **12** is the stop address.

The following stop addresses are common to all diagnostic routines except EEA4 (where Y = 6), and EEF0 (where Y = 0). The y represents the second hexadecimal digit following the EE in the name of the diagnostic routine as shown on the status screen **4** (see DIAG 4).

Address	Meaning
y011	The branch operation did not work. The microprocessor has failed. See the FSI section for "Error Code E100."
y012	A test failed in this routine.
y013	A get pointer error occurred. Indicates a microprogram error.
y014	The routine ended successfully **(Normal end)**.
y015	Reserved.
y016	A command that was not valid was received from the MD. Rerun the routine. If the routine runs successfully, ignore the error. If the routine fails repeatedly, see FSI section for "Error Code E100."
y017	The MD connection is broken.
y018	The maintenance adapter card detected an error during microprocessor to MD communications.

How to Use the Information Supplied by the Support Diagnostics

When an error occurs while running the diagnostics, the diagnostic stops with the status screen displayed. When the status is ERROR, use the information from the error screens as follows:

1. Press the enter key to advance to the first error screen.
2. Write down the information from the error screen.
3. Press ENTER to advance to any following error screens and write down the information from those screens.
4. Look at the first six characters from the first error screen. These constitute a failure ID code.
5. Look up the failure ID code in the chart that is part of the description of the routine in this section of the maintenance information. The chart tells you what failure occurred and sends you to the error analysis diagram (EAD) that guides you in troubleshooting that error. The other information recorded from the error screens is used to analyze the error using the EAD.
6. When the failure has been repaired, load functional microcode into the control unit, insert the product diskette into the MD, and select the Unit Test option to verify that the subsystem operates correctly.

For example, if you were running EE32 and the diagnostic stopped with ERROR displayed as the status on the status display:

1. Press the ENTER key to display the first error screen.
2. Assume the first six characters on the first error screen are BU2021.
3. Look in the chart in the description of EE32 and find BU2021.
4. The chart explains that a buffer channel status error occurred and that the FSI section for error code D5nn should be used.

Verify

Some error screens can send you to the following reference screen.

```
MACHINE FAILURES MAY
CAUSE CURRENT ERROR
DATA TO BE INVALID.
SEE DIAG 1 "VERIFY".
```

This message is referred to by routines EE12, EE13, EE14, and EE85. The message tells you to make sure that the data displayed by the error displays is correct.

Either XR address bus or XR data bus errors can occur that can cause the data that is read by the microprocessor to be invalid. The microprocessor then displays this invalid data as the data on the error screen. To make sure that you know that you have the correct data, you must verify the error screen display.

1. Write down the error display data as explained under "How to Use the Information Supplied by the Diagnostics."
2. Display the control unit scan rings. Note that the XRA register information is formatted differently on the scan ring display than it is on the diagnostic display. See SDISK 1 for "Control Unit Scan Rings." and DF 1 for "XRA Register."
3. Write down the data in ERA, ERB, and the XRA registers. Also write down the value of the XR error bit (PSR bit 0).
4. Compare the data from the scan rings with the data from the error display.
5. If the data is different, use the data from the scan rings.
6. If the data from the error display is valid, you do not need to verify the data again while diagnosing the failure.

How to Use the Diagnostic Test Options

The test options for the support diagnostics are very versatile, but you must understand some features of the programs to use the options most effectively. The control program in the MD interacts with the diagnostic programs to control the way the options function. The options perform somewhat differently for running a diagnostic section than they do for running a diagnostic routine.

In running a diagnostic section or running from an error code entry, the MD selects a group of routines to be run. The MD then gives you the opportunity to select step mode or to loop the section. Selecting either of these options at this time (before the routines have started running) affects all of the routines. Selections made after the routines are running can affect a single routine or all the routines.

In running a diagnostic routine, you cannot select run options until after the first pass of the routine. Any option selected applies only to the one routine because only one routine is running.

Each routine contains indicators called flags that the MD sets and tests to determine what control options are effective for each run of a routine. If step mode or loop section options are selected at the beginning of the run, the MD sets the corresponding flags on in *each* routine in the section. During the run, other options can be selected that affect single routines in the section. Selecting run with no other options selected clears all the options for that routine.

Some Examples of Using the Diagnostic Test Options

The following discussion does not give all the possible combinations for use of test options. It illustrates two ways in which the options can be used so that you can see how to devise other uses for them.

Using Step Mode, Loop Routine, and Error Loop

Refer to the figure on this page. Let us assume that we selected a diagnostic section and answered yes to the questions "Do you want to loop the section?" and "Do you want to run in step mode?"

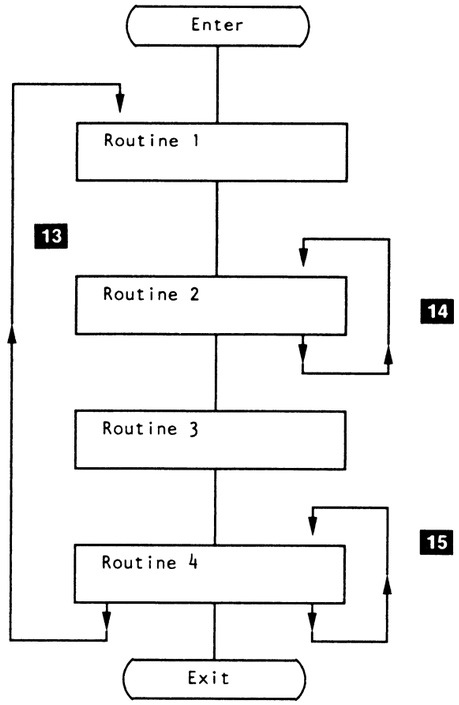
When the section starts, routine 1 runs and stops. When you press the ENTER key, routine 2 runs and stops. Presuming that we have no errors on the first pass, routines 3 and 4 run in the same way as routines 1 and 2. When you press ENTER after routine 4 stops, routine 1 starts again as shown by loop **13**.

Now, on the second pass, let us say that an error occurs in routine 2, so routine 2 stops with the error indication. You can modify the run options at this time by using selection 2 from the DIAG.11 screen (**6** on DIAG 4).

Let us say that you select ERROR LOOP. The routine enters loop **14**, and you can analyze the failure. After you analyze the failure, you can get to the DIAG.11 screen again by pressing PF. Let us say that you select RUN with no other options. This selection clears step mode and loop routine from the flags in routine 2. Now, routines 3 and 4 continue in step mode and we return to loop **13** where routine 1 runs in step mode. However, routine 2 does not stop to permit you to press enter before routine 3 starts. (Remember, you cleared step mode in routine 2.)

Using Loop Routine

See the figure on this page again. This time let us say that we selected a diagnostic section and will loop the section but not in step mode. When the section begins, routine 1 runs, followed by routines 2, 3, and 4, then loop **13** starts the operation again. Let us say that on one of the passes an error occurs in routine 4. The diagnostics stop in routine 4 and you select LOOP RTN as a test option. This selection starts us in loop **15**. Let us say that you cannot get a failure while running in the LOOP RTN options, so you press the PF key to get to the DIAG.11 screen to select another option. To return to loop **13**, you must select LOOP SCT for the test option. (Remember, if you just select RUN, you clear all the control options for that routine.)



How to End Use of the Diagnostics

When you are through running diagnostics, go to DIAG.11 either by pressing the PF key on the MD keyboard/display or by pressing the ENTER key if you are stopped with GOOD displayed on the status screen **4** (see DIAG 4). Selection 4 on the DIAG.11 screen **6** (see DIAG 4) takes you to the support diskette main menu **1** (see DIAG 4). You can then choose to use some other facility from the support diskette or you can end the call (selection 4 on the main menu).

To end the call:

1. If you have repaired the failure:
   a. Remove the support diskette from the MD.
   b. IML the functional microcode into the control unit.
   c. Insert the product diskette into the MD.
   d. Select the unit test option to verify that the subsystem operates correctly.
   e. Return the CU Offline/CU Online switch to the CU Online position.
   f. Return the subsystem to the customer.
2. If you have not repaired the failure, follow the defer call procedure or other procedure to continue with the analysis of the failure.

Maintenance Device/Maintenance Adapter Diagnostic

This diagnostic tests the communication path between the maintenance device and the maintenance adapter card in the control unit. The diagnostic tests the cables and the part of the maintenance adapter card that communicates with and responds to the MD.

When the maintenance device/maintenance adapter diagnostic is selected (selection 4 on the subsystem diagnostics screen), all tests are automatically run. When the diagnostic stops, one of the following screens will be displayed:

- Test complete screen
- Tag active screen (failure ID= MD1020)
- Function error screen (failure ID = MD2025).

Pressing Enter from any of these screens takes you to a selection screen.

Selection Screen

```
** SELECT: 1.RESTART
2.PUT TEST 3.GET TST
4.OPEN TEST
5.STATUS OUT TEST
```

This screen permits you to select the tests you want to run. Selection 1 restarts the complete maintenance device/maintenance adapter diagnostic. The other selections run the tests identified. PF1 stops the tests and returns you to the main menu.

Open Test

This test shifts a data byte of hexadecimal 5A from the maintenance device through the maintenance adapter shift register.

Put Test

This Test sends a hexadecimal 55 (Load Data Reg 1) command to the maintenance adapter with a data byte of hexadecimal 5A.

Get Test

This test sends a hexadecimal 5E (Unload The MTI Reg) command to the maintenance adapter and receives a data byte of hexadecimal 20.

Status Out Test

This test sends a data byte with bad parity to the maintenance adapter and checks that the maintenance adapter signals that the byte is wrong.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
MD1020	MD display lines 2-4 indicate that one or more inbound signal lines are active (zero volts). This error message will vary depending on the state of each signal line named.	An active level (zero volts) on 'status in' will force 'read' active. 'Status in' is controlled by the MD. Test this line at the maintenance adapter card if 'read' is active. These signal lines may be held active (zero volts) by the microcode in the CU. To eliminate this as the cause of the problem, do a power on reset (POR) to the control unit by removing the IML diskette, and pressing the IML switch. The test may be restarted by pressing enter on the MD keyboard and responding "YES" to the "RETRY" message.	FRU115 FRU117 FRU135 FRU169	MD1020 ** ERROR MD 'WRITE' ACTIVE MD 'READ' ACTIVE MD 'STS OUT' ACTIVE
MD1035	The program detected that an internal MD failure has occurred.	Replace the MD.	MD	MD1035 ** ERROR THE MD IS FAILING
MD1025	The Port function indicated by the 'xxxx' field has failed. The order of testing is: OPEN, PUT, GET, and STAT. The error Status Byte (aa) definition is: 48 = Timed out waiting for the function to complete. (Caused by a missing signal.) 81 = If the 'xxxx' field = OPEN, this status byte means the serial data path has failed. If the 'xxxx' field = PUT, GET, or STAT, this sense byte means an error condition occurred. (Caused by an unexpected active signal.)	1. Execute the MD diagnostic tests. See the "IBM Maintenance Device Maintenance Information." 2. See EAD 1 for E103 errors. 3. See OPER 1, "Maintenance Device to 3480 Maintenance Adapter Communication Path," for the signal lines used during the OPEN, PUT, GET, AND STAT tests. Use this information to find the failing line, and use the status byte (aa) to show what type of failure occurred on that line.	FRU115 FRU117 FRU134 FRU135 FRU169	MD2025 ** ERROR PORT 'xxxx' FAILED.. STAT= aa (ENTER = LOOP) xxxx = OPEN PUT GET STAT aa = Status Byte

Basic Control Unit Test

The purpose of the basic control unit test is to assure that the maintenance adapter, processor, and control storage functional areas operate correctly.

This test consists of two major sections. The first section uses the maintenance adapter to MD interconnection to test:

- The MA data and address registers
- The control unit control storage data bus
- All control storage address bus
- The control unit microprocessor's ability to execute the resident IML microcode.

The IML microcode will detect errors in the microprocessor, external registers, and control storage areas.

The second section of the test loads and executes all the basic support micro-diagnostics that are defined in E010 - CU Functions Test (see DIAG 1).

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

```
*** MAIN MENU ***
ENTER A NUMBER
FROM THE FOLLOWING
LIST:

1=SUBSYS DIAGNOSTICS
2=SUBSYS DSPLY/ALTER
3=SUPPORT UTILITIES
   *END OF LIST*

1= SELECTED DIAG.
2= BASIC CU TESTS
3= DR CMD EXERCISER
4= MD/MA DIAG.

27100  ** DO YOU
WANT TO LOOP THE
DIAGNOSTICS
```

If 'no' is the answer, the CU Basic and E010 linked tests run one pass.

If 'yes' is the answer, the CU Basic and E010 tests will run on the first pass, and on the second and succeeding passes only E010 will run.

If no failures are detected, the following message is displayed after the diagnostics have completed: 'BASIC CU DIAG RAN ERROR FREE'.

Basic CU Test Messages

```
****
TESTING THE MA REGS

TEST DATA=xx
```

xx Test data is:
- 00
- FE
- AA
- 55
- B2
- C4

```
****
TESTING CONTROL
STORAGE . .
PATTERN=xxxx
```

xxxx Test data pattern is:
- 0000
- FEFE
- AAAA
- 5555
- B2B2
- C4C4

```
****
RUNNING THE IML

DIAGNOSTICS
```

```
** CU BASIC TEST
RAN ERROR FREE
```

Basic Control Unit Test (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see the EAD 1 for error code Fnnn.		
CB1023	MD display line 1 can also show: CB1023 **DATA COMPARE. Data is written to and read back from four maintenance adapter card registers (rrrrr). If the EXPECTED data equals the ACTUAL data, the parity bit (which is not shown) is causing the error.	1. Remove the IML diskette from the control unit, then press the IML switch to cause a power on reset. 2. Respond YES to the RETRY message on the MD display to restart the test.	FRU115 FRU169 FRU139	CB1023 **DATA PARITY ERROR.. (rrrrr) EXPECTED DATA = (xx) ACTUAL DATA = (xx) rrrrr = DREG1 DREG2 AREG1 AREG2
CB1025	MD display line 1 can also show: CB1025 **ADDR PARITY CB1025 **DATA PARITY CB1025 **CS DATA BUS Data is written to and read back from control store, and the EXPECTED and ACTUAL values are displayed if an error occurs. If the EXPECTED data equals the ACTUAL data, the parity bit (which is not shown) is causing the error.	See the FSI section for error code E100.	FRU134 FRU135 FRU115 FRU117 FRU139	CB1025 **ADDRESS BUS ERROR.. EXPECTED = (xxxx) ACTUAL = (xxxx)
CB1026	The extended operation bit in the maintenance status byte (MSB) register did not reset after a 'Stepmp' operation.	1. Remove the IML diskette, then press the IML switch to cause a power-on reset. 2. Select and run the "Basic CU Test" option again. 3. Check the top card connectors on the logic card FRUs listed for this error.	FRU117 FRU115 FRU139	CB1026 ** MP FAILURE . . .
CB1027	The instruction executed bit in the maintenance status byte (MSB) register did not activate after a Force Instruction and 'Stepmp' command operation.	1. Remove the IML diskette, then press the IML switch to cause a power-on reset. 2. Select and run the "Basic CU Test" option again. 3. Check the top card connectors on the logic card FRUs listed for this error.	FRU117 FRU115 FRU139	CB1027 ** MP FAILURE . . .
CB1028	MD display line 2 can also show: ERROR..**ADDR PARITY A reset is issued to the MP followed by two 'Step' commands. This results in a hardware forced branch to address 0000 and the execution of the first PROM instruction. If the EXPECTED data equals the ACTUAL data, the parity bit (which is not shown) is causing the error.	Go to the PWR section, "MAP 0100--Power Start," entry point A, and follow the power MAPs. Run diagnostic 'E010'. Check the top card connectors on the logic card FRUs listed for this error.	FRU117 FRU115 FRU139	CB1028 ** MP RESET ERROR..**INVALID ADR EXPECTED = (xxxx) ACTUAL = (xxxx)

Basic Control Unit Test (Continued)

Basic Control Unit Test (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see the EAD 1 for error code Fnnn.		
CB1036	This error is generated by the PROM diagnostic program that tests CU Control Storage. MD display line 2 will contain a "#CK1" if a check 1 condition occurred. Register data is defined in the maintenance information DF section.	Run diagnostic E010.	FRU135 FRU134 FRU115 FRU117 FRU139	CB1036 ** CS FAILURE ERA=aa) ERB=bb) #CK1 DATA ADDRESS= (xxxx) DATA PATTERN= (xxxx)

CB1037	This error is generated by the PROM diagnostic program while testing basic CU functions.
	
	MD display line 2 will contain a "#CK1" if a check 1 condition occurred.
	
	Register data is defined in the maintenance information DF section.
		Run diagnostic E010.	FRU117
			FRU115
			FRU121
			FRU085[1]
			FRU114
			FRU120
			FRU116
			FRU119
			FRU188
			FRU139
				CB1037 ** MP FAILURE
				ERA=aa) ERB=bb) #CK1
				XRA=xx) MTI=tt)
				PSR=pp PCR=cc PER=ee

CB1038	This error is generated by the PROM diagnostic program while testing basic CU functions.
	
	MD display line 2 will contain a "#CK1" if a check 1 condition occurred.
	
	Register data is defined in the maintenance information DF section.
		See EAD 1 for error code Fnnn.
		
		XR errors can cause ERA and ERB errors. Use routine EE85 to check the ERA and ERB registers.
		
		Run diagnostic E010.
			FRU121
			FRU118
			FRU117
			FRU115
			FRU114
			FRU120
			FRU119
			FRU116
			FRU134
			FRU135
			FRU157
			FRU158
			FRU159
			FRU139
				CB1038 ** XR FAILURE
				ERA=aa) ERB=bb) #CK1
				XRA=xx) MTI=tt)
				PSR=pp PCR=cc PER=ee

CB1041	An error occurred while trying to read error data from the control unit.	1. Remove the IML diskette from the control unit, then press the IML switch to cause a power on reset. 2. Respond YES to the RETRY message on the MD display to restart the test. See DIAG 1 for "Maintenance Device/Maintenance Adapter Diagnostic."	FRU115 FRU117 FRU169 FRU139	CB1041 MA CONNECTION ERROR.. -RESET THE CU. (ENTER = RETRY)
CB1045	The PROM diagnostic failed to complete successfully, and the error code is invalid.	1. Remove the IML diskette from the control unit, then press the IML switch to cause a power on reset. 2. Press the enter key on the MD. 3. Select and run the "Basic CU Tests" option again.	FRU115 FRU117 FRU169 FRU139	CB1045 **INVALID IML ERROR CODE = (xxxx) . .

[1] This FRU is EC sensitive. See CARR-DR 4.

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine provides a general check of the microprocessor data flow, including:

- Branching
- Local storage access and storage capabilities
- Paths to external registers
- Control storage access and storage capabilities.

Routine Start Address: 2010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
HC2021	Failure occurred when testing branch conditions for active and reset conditions.	1. Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE12 again. 2. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. Also see action number 4 of this Additional Actions column. 3. If PSR bit 0 = 1, see EAD 1 for error code Fnnn. 4. If a diagnostic failure occurs and no errors are detected by the hardware, see the FSI section for error code E100 and perform the procedures for the microprocessor and control storage. 5. XR errors (PSR bit 0 = 1) can cause ERA and ERB errors. Use diagnostic EE85 to check the ERA and ERB registers.	FRU121 FRU118 FRU117 FRU115 FRU114 FRU120 FRU119 FRU116 FRU134 FRU135 FRU157 FRU158 FRU159 FRU139	nnnnnn ERA ACT = xx,EXP= yy ERB ACT = xx,EXP= yy PSR ACT = xx,EXP= yy PER ACT = xx,EXP= yy MTI ACT = xx,EXP= yy XRA ACT = xx,EXP= yy MDI= md,WR= dw,RD=dr MACHINE FAILURES MAY CAUSE CURRENT ERROR DATA TO BE INVALID. SEE DIAG 1 "VERIFY". This screen is explained on DIAG 6. nnnnnn = Failure ID xx = The actual contents of the external register yy = The expected contents of the external register md = Contents of the maintenance data in register dw = Data written dr = Data read

Interrupt Level Test - Routine EE13

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine tests the microprocessor interrupt handling for interrupt levels 0 through 7.

Routine Start Address: 3010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
HC3021	Failure occurred when testing if interrupts can be suspended.	1. Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE13 again. 2. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. Also see step 4 of this Additional Actions column. 3. If PSR bit 0 = 1, see EAD 1 for error code Fnnn. 4. If a diagnostic failure occurs and no errors are detected by the hardware, see the FSI section for error code E100 and perform the procedures for the microprocessor and control storage. 5. XR errors (PSR bit 0 = 1) can cause ERA and ERB errors. Use routine EE85 to check the ERA and ERB registers.	FRU121 FRU118 FRU117 FRU115 FRU114 FRU120 FRU119 FRU116 FRU134 FRU135 FRU157 FRU158 FRU159 FRU139	nnnnnn ERA ACT = xx,EXP= yy ERB ACT = xx,EXP= yy PSR ACT = xx,EXP= yy PER ACT = xx,EXP= yy MTI ACT = xx,EXP= yy XRA ACT = xx,EXP= yy MDI= md,WR= dw,RD=dr MACHINE FAILURES MAY CAUSE CURRENT ERROR DATA TO BE INVALID. SEE DIAG 1 "VERIFY". This screen is explained on DIAG 6. nnnnnn = Failure ID xx = The actual contents of the external register yy = The expected contents of the external register md = Contents of the maintenance data in register dw = Data written dr = Data read
HC3022	Invalid subroutine return code.			
HC3023	The interrupt mask register (IMR) has bits that won't change. They are fixed in either an ON or an OFF position.			
HC3024	While using the interrupt mask register (IMR) an XR error is detected.			
HC3025	The local store page was not saved correctly or a PSW swap occurred to the wrong interrupt level.			
HC3026	An XR error occurred while exercising the processor external registers.			
HC3027	The interrupts occurred in the wrong sequence. The PSR current and/or previous values are wrong.			
HC3028	Extend bits for external register addressing were not saved and set/reset correctly.			
HC3029	Extend bits for external register addressing were not saved and set/reset correctly.			
HC302A	The local store page was not saved correctly or a PSW swap occurred to the wrong interrupt level.			
HC302B	An XR error occurred while exercising the processor external registers.			
HC302C	The interrupts occurred in the wrong sequence. The PSR current and/or previous values are wrong.			
HC302D	Extend bits for external register addressing were not saved and set/reset correctly.			
HC302E	The condition code is not set correctly in the PSW.			
HC302F	The local store page was not saved correctly or a PSW swap occurred to the wrong interrupt level.			

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
HC3030	Extend bits for external register addressing were not saved and set/reset correctly.	1. Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE13 again. 2. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. Also see step 4 of this Additional Actions column. 3. If PSR bit 0 = 1, see EAD 1 for error code Fnnn. 4. If a diagnostic failure occurs and no errors are detected by the hardware, see the FSI section for error code E100 and perform the procedures for the microprocessor and control storage. 5. XR errors (PSR bit 0 = 1) can cause ERA and ERB errors. Use routine EE85 to check the ERA and ERB registers.	FRU121 FRU118 FRU117 FRU115 FRU114 FRU120 FRU119 FRU116 FRU134 FRU135 FRU157 FRU158 FRU159 FRU139	See the "Error Displays" column on DIAG 55.
HC3031	The interrupts occurred in the wrong sequence. The PSR current and/or previous values are wrong.			
HC3032	The interval timer failed during interrupt handling.			
HC3033	The interval timer failed during interrupt handling.			
HC3034	The interval timer failed during interrupt handling.			
HC3035	An XR error occurred while exercising the processor external registers.			
HC3036	Check 1 error occurred during the interrupt test.			
HC3037	Check 1 error occurred during the interrupt test.			
HC3038	An XR error occurred while exercising the processor external registers.			

0 0 0 0 0 0 0 0 0 0

Processor External Register Test - Routine EE14

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine provides a check of the microprocessor external registers function and error handling.

Routine Start Address: 4010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
HC4021	Jump address high register failed.	1. Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE14 again. 2. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. Also see action number 4 of this Additional Actions column. 3. If PSR bit 0 = 1, see EAD 1 for error code Fnnn. 4. If a diagnostic failure occurs and no errors are detected by the hardware, see the FSI section for error code E100 and perform the procedures for the microprocessor and control storage. 5. XR errors (PSR bit 0 = 1) can cause ERA and ERB errors. Use diagnostic EE85 to check the ERA and ERB registers.	FRU121 FRU118 FRU117 FRU115 FRU114 FRU120 FRU119 FRU116 FRU134 FRU135 FRU157 FRU158 FRU159 FRU139	nnnnnn ERA ACT = xx,EXP= yy ERB ACT = xx,EXP= yy PSR ACT = xx,EXP= yy PER ACT = xx,EXP= yy MTI ACT = xx,EXP= yy XRA ACT = xx,EXP= yy MDI= md,WR= dw,RD=dr MACHINE FAILURES MAY CAUSE CURRENT ERROR DATA TO BE INVALID. SEE DIAG 1 "VERIFY". This screen is explained on DIAG 6. nnnnnn = Failure ID xx = The actual contents of the external register yy = The expected contents of the external register md = Contents of the maintenance data in register dw = Data written dr = Data read
HC4022	Force jump operation failed.			
HC4023	Jump address low register failed.			
HC4024	Interval timer registers A and/or B failed.			
HC4025	Interval timer A and/or B timings wrong.			
HC4026	Processor control register (PCR) failed.			
HC4027	Interrupt mask register (IMR) failed.			
HC4028	Processor diagnostic register (PDR) failed.			
HC4029	Local storage page register (LSP) failed.			
HC402A	ERA or ERB is incorrect, or the ERA or ERB could not be reset, or the PSW error indication is incorrect. See step 1 under the Additional Actions column of this chart.			
HC402B	Level 1 interrupt problem.			

Data Buffer Data Path Test - Routine EE32

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine contains three modules that test the data buffer operation. The modules test the data paths into and out of the buffer, the buffer CRC character generation, and the ability to address all locations in the buffer.

Routine Start Address: 2010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Data Buffer Data Path Test

This module consists of four tests that check each of the four data paths into the data buffer.

- **Test 1** uses the channel adapter write data path to write data into the buffer and the drive read data path to read data from the buffer.
- **Test 2** uses the drive write data path to write data into the buffer and the channel adapter read data path to read data from the buffer.
- **Test 3** writes 256 bytes of ripple data using the channel adapter write data path and reads the data back using the drive read data path.
- **Test 4** writes 256 bytes of ripple data using the drive write data path and reads the data back using the channel adapter read data path.

A 256 byte data pattern of each hexadecimal character from hexadecimal 00 to hexadecimal FF is written into one data buffer data path and read through another data path. The expected data (written) is then compared to the actual data (read).

Data Buffer Check Character Test

This module tests the CRC character generation. A record is written and the CRC character is stored. The same record is then read and the calculated CRC character is compared with the stored CRC character.

Data Buffer Memory Test

This module tests the addressability of the data buffer by writing into and reading out of every buffer location. It also tests the segment looping function of the data buffer.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

Data Buffer Data Path Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113
BU2021	A buffer channel status error occurred during a write operation through the channel write data path.	See the FSI section for error code D5nn.	
BU2022	A buffer device status error occurred during a read operation through the drive read data path.	See the FSI section for error code D6nn.	
BU2023	A buffer device status error occurred on the last pass during a read operation through the drive read data path.	See the FSI section for error code D6nn.	
BU2024	Data read from the buffer did not equal the data written into the buffer.	If any errors are set, ignore the data compare error and troubleshoot the errors set by the hardware. See the FSI section for error code D5nn.	
BU2025	The BDSE status bit 0 (device pointer stop) was not active after a read operation through the drive read data path.	See the FSI section for error code D6nn.	
BU2026	Channel - pointer = Stop was not on after an MP read.	See the FSI section for error code D5nn.	
BU2027	A buffer device status error occurred during a write operation through the drive write data path.	See the FSI section for error code D6nn.	
BU2028	A buffer channel status error occurred during a write operation through the channel write data path.	See the FSI section for error code D5nn.	
BU2029	A buffer channel status error occurred on the last pass during a read operation through the channel read data path.	See the FSI section for error code D5nn.	
BU202A	Data read from the buffer did not equal the data written into the buffer.	If any errors are set, ignore the data compare error and troubleshoot the errors set by the hardware. See the FSI section for error code D5nn.	
BU202B	'Service in' did not become active or 'data in' is active on a channel operation.	See the FSI section for error code D5nn.	
BU202C	'Data in' did not become active or 'service in' is active on a channel operation.	See the FSI section for error code D5nn.	
BU202D	Channel 1 stop bit was not active after a channel operation.	See the FSI section for error code D5nn.	
BU202E	'Microprocessor write complete' did not become active on a channel write operation.	See the FSI section for error code D5nn.	
BU202F	Buffer channel status error occurred during a channel write operation.	See the FSI section for error code D5nn.	

ERROR DISPLAYS

```
nnnnnn
ERA=ra,          ERB=rb
PSR=xx, PER=pp, XRA=aa
MTI=mm, MDI=md
```

nnnnnn Failure ID

**	No errors were set
ra	Contents of error register A
rb	Contents of error register B
xx	Contents of the processor status register
pp	Contents of the processor error register
aa	Contents of the external address register
mm	Contents of the maintenance tag in register
md	Contents of the maintenance data in register

```
BCSE = abcde
BDSE = fghij
BWRP = cc
```

*	No errors were set
a	Buffer channel status and error register bits 0 - 3
b	BCSE channel error group 0
c	BCSE channel error group 1
d	BCSE channel error group 2
e	BCSE channel error group 3
f	BCSE device status and error register bits 0 - 3
g	BDSE device error group 0
h	BDSE device error group 1
i	BDSE device error group 2
j	BDSE device error group 3
cc	Contents of the buffer wrap register

```
DATA EXP/WRT=aaaa
DATA READ   =bbbb
BUFFER adr  =cccc
```

aaaa	Data written into the buffer
bbbb	Data read from the buffer
cccc	Current buffer address

NOTE: You will see the following error displays only if the Data Compaction Feature is installed.

```
CMS = aa,  CTXE = ee
CMM = bb,  CMD0 = ff
CHM = cc,  CMD1 = gg
CTE0 = dd, CMFL = hh
```

aa	Contents of the CCMP status register
bb	Contents of the CCMP mode register
cc	Contents of the Channel mode register
dd	Contents of the C3P0 error register
ee	Contents of the C3P0 XR error register
ff	Contents of the CCMP diagnostic 0 register
gg	Contents of the CCMP diagnostic 1 register
hh	Contents of the CCMP feature level register

```
CP0E0 = aa, CP2E0 = ee
CP0E1 = bb, CP2E1 = ff
CP1E0 = cc, CP3E0 = gg
CP1E1 = dd, CP3E1 = hh
```

aa	Contents of the Comp 0 error 0 register
bb	Contents of the Comp 0 error 1 register
cc	Contents of the Comp 1 error 0 register
dd	Contents of the Comp 1 error 1 register
ee	Contents of the Comp 2 error 0 register
ff	Contents of the Comp 2 error 1 register
gg	Contents of the Comp 3 error 0 register
hh	Contents of the Comp 3 error 1 register

```
CP0C = aa,   CP0D = ee
CP1C = bb,   CP1D = ff
CP2C = cc,   CP2D = gg
CP3C = dd,   CP3D = hh
```

aa	Contents of the Comp0 configuration register
bb	Contents of the Comp1 configuration register
cc	Contents of the Comp2 configuration register
dd	Contents of the Comp3 configuration register
ee	Contents of the Comp0 diagnostic register
ff	Contents of the Comp1 diagnostic register
gg	Contents of the Comp2 diagnostic register
hh	Contents of the Comp3 diagnostic register

```
CBC CM0 = aaaaaaaa
CBC CM1 = bbbbbbbb
CBC CM2 = cccccccc
CBC CM3 = dddddddd
```

aaaaaaaa = Channel byte count for Comp 0
bbbbbbbb = Channel byte count for Comp 1
cccccccc = Channel byte count for Comp 2
dddddddd = Channel byte count for Comp 3

* These FRUs are EC sensitive. FRU112 may not be present. See CARR-CU 7.

0 0 0 0 0 0 0 0 0 0

Data Buffer Data Path Test - Routine EE32 (Continued)

Data Buffer Data Path Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.
BU2021	A buffer channel status error occurred during a write operation through the channel write data path.	See the FSI section for error code D5nn.
BU2022	A buffer device status error occurred during a read operation through the drive read data path.	See the FSI section for error code D6nn.
BU2023	A buffer device status error occurred on the last pass during a read operation through the drive read data path.	See the FSI section for error code D6nn.
BU2024	Data read from the buffer did not equal the data written into the buffer.	If any errors are set, ignore the data compare error and troubleshoot the errors set by the hardware. See the FSI section for error code D5nn.
BU2025	The BDSE status bit 0 (device pointer stop) was not active after a read operation through the drive read data path.	See the FSI section for error code D6nn.
BU2026	Channel - pointer = Stop was not on after an MP read.	See the FSI section for error code D5nn.
BU2027	A buffer device status error occurred during a write operation through the drive write data path.	See the FSI section for error code D6nn.
BU2028	A buffer channel status error occurred during a write operation through the channel write data path.	See the FSI section for error code D5nn.
BU2029	A buffer channel status error occurred on the last pass during a read operation through the channel read data path.	See the FSI section for error code D5nn.
BU202A	Data read from the buffer did not equal the data written into the buffer.	If any errors are set, ignore the data compare error and troubleshoot the errors set by the hardware. See the FSI section for error code D5nn.
BU202B	'Service in' did not become active or 'data in' is active on a channel operation.	See the FSI section for error code D5nn.
BU202C	'Data in' did not become active or 'service in' is active on a channel operation.	See the FSI section for error code D5nn.
BU202D	Channel 1 stop bit was not active after a channel operation.	See the FSI section for error code D5nn.
BU202E	'Microprocessor write complete' did not become active on a channel write operation.	See the FSI section for error code D5nn.
BU202F	Buffer channel status error occurred during a channel write operation.	See the FSI section for error code D5nn.

FRUS: FRU114, FRU120, *FRU112, *FRU113

ERROR DISPLAYS

Note: You will see this error display only if the 4.5 Mb/s buffer adapter card is installed.

```
CMS = AA, CTXE = EE
CMM = BB, CMD0 = FF
CHM = CC, CMD1 = GG
CTE0= DD, CMFL = HH
```

AA Contents of the CCMP Status Register
BB Contents of the CCMP Mode Register
CC Contents of the Channel Mode Register
DD Contents of the C2P0 Error 0 Register
EE Contents of the C2P0 XR Error Register
FF Contents of the CCMP Diagnostic 0 Register
GG Contents of the CCMP Diagnostic 1 Register
HH Contents of the CCMP Feature Level Register

```
nnnnnn
ERA=ra,ERB=rb
PSR=xx,PER=pp,XRA=aa
MTI=mm,MDI=md
```

nnnnnn = Failure ID
** = no error set

aa = Contents of XRA reg
md = Contents of MDI reg
mm = Contents of MTI reg
ra = Contents of ERA reg
rb = Contents of ERB reg
pp = Contents of PER reg
xx = Contents of PSR reg

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
```

aaaa = Data written into buffer
bbbb = Data read from buffer
cccc = Current buffer address

```
BCSE=abcde
BDSE=fghij
BWRP=cc
```

* = No errors were set
a = Buffer channel status and error register bits 0-3
b = BCSE channel error group 0
c = BCSE channel error group 1
cc = Contents of the buffer wrap register
d = BCSE channel error group 2
e = BCSE channel error group 3
f = Buffer device status and error register bits 0-3
g = BDSE device error group 0
h = BDSE device error group 1
i = BDSE device error group 2
j = BDSE device error group 3

* These FRUs are EC sensitive. FRU112 may not be present. See CARR-CU 7.

Data Buffer Data Path Test (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. 2. If PSR bit 0 = 1 see EAD 1 for error code Fnnn.	FRU114 FRU120 FRU112[1] FRU113[1]	See the "Error Displays" column on DIAG 102.
BU2030	Buffer channel status error occurred after a Store CRC command.	See the FSI section for error code D5nn.		
BU2031	Data read from the buffer did not equal the data written into the buffer.	If any errors are set, ignore the data compare error and troubleshoot the errors set by the hardware. See the FSI section for error code D6nn.		
BU2032	'Device pointer stop' or 'device complete' was not active after a read operation through the drive read data path.	See the FSI section for error code D6nn.		
BU2033	Buffer device status error occurred during a read operation through the drive read data path.	See the FSI section for error code D6nn.		
BU2034	Buffer device status error occurred during a write operation through the drive write data path.	See the FSI section for error code D6nn.		
BU2035	'Device read end' and 'device data transfer complete' bits were not on after a write operation through the drive write data path.	See the FSI section for error code D6nn.		
BU2036	'Service in' did not become active or 'data in' is active on a channel operation.	See the FSI section for error code D5nn.		
BU2037	'Data in' did not become active or 'service in' is active on a channel operation.	See the FSI section for error code D5nn.		
BU2038	Data read from the buffer did not equal the data written into the buffer.	If any errors are set, ignore the data compare error and troubleshoot the errors set by the hardware. See the FSI section for error code D5nn.		
BU2039	Buffer channel status error occurred during a write operation through the channel write data path.	See the FSI section for error code D5nn.		
BU203A	Channel pointer equals stop was not on in the buffer channel status and error (BCSE) register after a channel operation.	See the FSI section for error code D5nn.		

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Check Character Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. 2. If PSR bit 0 = 1 see EAD 1 for error code Fnnn.	FRU114 FRU120	See the "Error Display" column on DIAG 102.
BU203B	Ending sequence error after a channel write operation.	See the FSI section for error code D5nn.	*FRU112	
BU203C	Ending sequence error after a channel read operation.	See the FSI section for error code D5nn.	*FRU113	
BU203D	A failure was detected by the buffer channel status and error (BCSE) or the buffer device status and error (BDSE) after an MP channel read or write operation.	See the FSI section for error code D5nn or D6nn.		
BU203E	Buffer channel remainder value is incorrect.	See the FSI section for error code D5nn.		
BU203F	The CRC character generated by the data transfer hardware and the expected CRC character are not equal. Errors are not checked.	See the FSI section for error code D5nn.		
BU2040	A failure was detected by the buffer channel status and error (BCSE) or the buffer device status and error (BDSE) after an MP device write operation.	See the FSI section for error code D5nn or D6nn.		
BU2041	Buffer channel remainder value is incorrect.	See the FSI section for error code D6nn.		
BU2042	The CRC character generated by the data transfer hardware and the expected CRC character are not equal. Errors are not checked.	See the FSI section for error code D6nn.		

* This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

0 0 0 0 0 0 0 0 0 0

Data Buffer Data Path Test - Routine EE32 (Continued)

Check Character Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. 2. If PSR bit 0 = 1 see EAD 1 for error code Fnnn.	FRU114 FRU120	See the "Error Display" column on DIAG 102.
BU203B	Ending sequence error after a channel write operation.	See the FSI section for error code D5nn.	*FRU112	
BU203C	Ending sequence error after a channel read operation.	See the FSI section for error code D5nn.	*FRU113	
BU203D	A failure was detected by the buffer channel status and error (BCSE) or the buffer device status and error (BDSE) after an MP channel write operation.	See the FSI section for error code D5nn or D6nn.		
BU203E	Buffer channel remainder value is incorrect.	See the FSI section for error code D5nn.		
BU203F	The CRC character generated by the data transfer hardware and the expected CRC character are not equal. Errors are not checked.	See the FSI section for error code D5nn.		
BU2040	A failure was detected by the buffer channel status and error (BCSE) or the buffer device status and error (BDSE) after an MP channel write operation.	See the FSI section for error code D5nn or D6nn.		
BU2041	Buffer channel remainder value is incorrect.	See the FSI section for error code D6nn.		
BU2042	The CRC character generated by the data transfer hardware and the expected CRC character are not equal. Errors are not checked.	See the FSI section for error code D6nn.		

* This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Data Buffer Data Path Test - Routine EE32 (Continued)

Memory Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. 2. If PSR bit 0 = 1 see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	See the "Error Displays" column on DIAG 102.
BU2043	A buffer channel status error was received after a write of modulo 32 addresses into the buffer.	See the FSI section for error code D5nn.		
BU2044	A buffer device status error was received after a read of the modulo 32 addresses just written into the buffer.	See the FSI section for error code D6nn.		
BU2045	The address read out of the buffer does not equal the expected address.	See the FSI section for error code D5nn.		
BU2046	Buffer channel status error was received after a specified data pattern was written into the buffer.	See the FSI section for error code D5nn.		
BU2047	A buffer device status error was received after a specified data pattern was read from the buffer.	See the FSI section for error code D6nn.		
BU2048	The data read out of the buffer does not equal the expected data.	See the FSI section for error code D5nn.		
BU2049	A buffer channel status error was received after a channel wrap write test.	See the FSI section for error code D5nn.		
BU204A	The buffer channel pointer and the actual buffer address are not equal after a buffer wrap write test.	Check the DLR switch setting (see CARR-CU 1189). See the FSI section for error code D5nn.	FRU114 FRU120	
BU2048	A buffer device status error was received after a buffer wrap read test.	See the FSI section for error code D6nn.	FRU114 FRU120 *FRU112 *FRU113	
BU204C	The buffer device pointer and the actual buffer address are not equal after a buffer wrap read test.	See the FSI section for error code D6nn.		

* This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine consists of five tests that check various control features of the data buffer.

Routine Start Address: 3010

If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Tests

'Suppress Out' and 'Data Stop' (Read Forward) Test

This test checks the response of the buffer to the 'suppress out' and 'data stop' signals. The diagnostic writes 135 data bytes to the buffer through the channel write data path. The diagnostic then reads the data back (with a read forward command) through the channel read data path. When the diagnostic has read one third of the data, it activates the 'suppress out' signal to the buffer and checks to ensure that the data transfer has stopped. The diagnostic then deactivates 'suppress out' and reads data again. After reading another one third of the data, the diagnostic activates 'data stop' and checks to ensure that the buffer has stopped transferring data. When the data transfer is complete, the diagnostic checks for any errors in the buffer channel status and error (BCSE) register and checks that the buffer is addressing the correct storage location.

'Suppress Out' and 'Data Stop' (Read Backward) Test

This test checks the response of the buffer to the 'suppress out' and 'data stop' signals. The diagnostic writes 135 data bytes to the buffer through the channel write data path. The diagnostic then reads the data back (with a read backward command) through the channel read data path. When the diagnostic has read one third of the data, it activates the 'suppress out' signal to the buffer and checks to ensure that the data transfer has stopped. The diagnostic then deactivates 'suppress out' and reads data again. After reading another one third of the data, the diagnostic activates 'data stop' and checks to ensure that the buffer has stopped transferring data. When the data transfer is complete, the diagnostic checks for any errors in the buffer channel status and error (BCSE) register and checks that the buffer is addressing the correct storage location.

Read Overrun Test

This test checks the circuits that recognize an overrun condition during a read operation. The diagnostic performs a read forward operation through the channel read data path, of 257 bytes. The address pointer is reset to address 6. The diagnostic then performs a read operation through the drive data path, of 257 bytes, which is placed in the buffer at address 6. After the read operation through the drive data path is completed, the diagnostic checks to ensure that the needed errors are set, and that the address pointers for the channel data path and the drive data path are correct.

Write Overrun Test

This test checks the circuits that detect overrun conditions during write operations. The diagnostic program performs a write operation of 257 bytes through the channel data path. The diagnostic then sets the buffer address pointer for the drive data path to address 6, and performs a write operation of 257 bytes through the buffer to the drive data path. The diagnostic then checks to ensure the needed errors are set and that the buffer address pointers are correct for the channel data path and the drive data path.

Separation Test

This test checks that the channel does not take data from the buffer before the drive has transferred the data to the buffer. The diagnostic program reads 262 bytes into the buffer through the drive to buffer data path. With the drive to buffer data path still active, the diagnostic performs a read forward operation for 256 bytes using the buffer to channel data path. With the channel data path still active, the diagnostic performs two consecutive 128-byte read forward operations and checks to ensure no errors have occurred. The diagnostic then performs another 256-byte read forward operation and checks for errors and to ensure that the address pointers are correct for both the channel and drive data paths. The diagnostic then performs a complete reset of the buffer.

4.5 Mb/s Channel Tests

4.5 Mb/s Buffer Adapter XR Reset Test

The 4.5 Mb/s buffer adapter tests run automatically if the 4.5 Mb/s buffer adapter card is installed.

This test verifies that each register on the 4.5 Mb/s buffer adapter card can be reset correctly. This is done by first writing to the register, then issuing the reset and verifying that the register is reset.

Checkers Tests

This test section forces errors and checks all the error detecting circuitry on the 4.5 Mb/s buffer adapter card.

Improved Data Recording Capability Tests

Note: The Improved Data Recording Capability tests will run automatically if the Improved Data Recording Capability feature is installed.

Buffer Adapter Improved Data Recording Capability XR Reset Test

This test verifies that each register on the buffer adapter Improved Data Recording Capability card can be reset properly. This is accomplished by first writing to the register, issuing the reset and then verifying the register is reset.

Buffer Adapter Improved Data Recording Capability RAM Tests

This test verifies that the data RAM's (random access memory) functions properly. This is accomplished by writing special data patterns into each RAM address then reading back and comparing the data written to the data read. Finally a unique address is written to each RAM and is then read back to verify their addressability.

Buffer Adapter Improved Data Recording Capability Checkers Test

This text section forces errors and checks all the error detecting circuitry on the buffer adapter card.

Buffer Adapter Improved Data Recording Capability Tests

The Improved Data Recording Capability function is verified by writing incremental, fixed and random data patterns with the Improved Data Recording Capability enabled. Then the data is read back, and compared to the original write data. The channel byte count registers are also verified during this test.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

Routine EE33 displays different combinations of the screens shown under ERROR DISPLAY in the following charts. The different failures and the different tests determine which screens are displayed. You can step through the screens you receive on your maintenance device, and locate the matching screen and its explanation in the chart.

If the 4.5 Mb/s Channel or the Improved Data Recording Capability features are installed and an error occurs, additional error displays show the actual and expected contents of the buffer adapter card external registers.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

0 0 0 0 0 0 0 0 0 0

Data Buffer Controls Test - Routine EE33

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine consists of five tests that check various control features of the data buffer.

Routine Start Address: 3010

Error Looping: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Tests

'Suppress Out' and 'Data Stop' (Read Forward) Test

This test checks the response of the buffer to the 'suppress out' and 'data stop' signals. The diagnostic writes 135 data bytes to the buffer through the channel write data path. The diagnostic then reads the data back (with a read forward command) through the channel read data path. When the diagnostic has read one third of the data, it activates the 'suppress out' signal to the buffer and checks to ensure that the data transfer has stopped. The diagnostic then deactivates 'suppress out' and reads data again. After reading another one third of the data, the diagnostic activates 'data stop' and checks to ensure that the buffer has stopped transferring data. When the data transfer is compiete, the diagnostic checks for any errors in the buffer channel status and error (BCSE) register and checks that the buffer is addressing the correct storage location.

'Suppress Out' and 'Data Stop' (Read Backward) Test

This test checks the response of the buffer to the 'suppress out' and 'data stop' signals. The diagnostic writes 135 data bytes to the buffer through the channel write data path. The diagnostic then reads the data back (with a read backward command) through the channel read data path. When the diagnostic has read one third of the data, it activates the 'suppress out' signal to the buffer and checks to ensure that the data transfer has stopped. The diagnostic then deactivates 'suppress out' and reads data again. After reading another one third of the data, the diagnostic activates 'data stop' and checks to ensure that the buffer has stopped transferring data. When the data transfer is complete, the diagnostic checks for any errors in the buffer channel status and error (BCSE) register and checks that the buffer is addressing the correct storage location.

Read Overrun Test

This test checks the circuits that recognize an overrun condition during a read operation. The diagnostic performs a read forward operation through the channel read data path, of 257 bytes. The address pointer is reset to address 6. The diagnostic then performs a read operation through the drive data path, of 257 bytes, which is placed in the buffer at address 6. After the read operation through the drive data path is completed, the diagnostic checks to ensure that the needed errors are set, and that the address pointers for the channel data path and the drive data path are correct.

Write Overrun Test

This test checks the circuits that detect overrun conditions during write operations. The diagnostic program performs a write operation of 257 bytes through the channel data path. The diagnostic then sets the buffer address pointer for the drive data path to address 6, and performs a write operation of 257 bytes through the buffer to the drive data path. The diagnostic then checks to ensure the needed errors are set and that the buffer address pointers are correct for the channel data path and the drive data path.

Separation Test

This test checks that the channel does not take data from the buffer before the drive has transferred the data to the buffer. The diagnostic program reads 262 bytes into the buffer through the drive to buffer data path. With the drive to buffer data path still active, the diagnostic performs a read forward operation for 256 bytes using the buffer to channel data path. With the channel data path still active, the diagnostic performs two consecutive 128-byte read forward operations and checks to ensure no errors have occurred. The diagnostic then performs another 256-byte read forward operation and checks for errors and to ensure that the address pointers are correct for both the channel and drive data paths. The diagnostic then performs a complete reset of the buffer.

4.5 Mb/s Channel Tests

4.5 Mb/s Buffer Adapter XR Reset Test

The 4.5 Mb/s buffer adapter tests run automatically if the 4.5 Mb/s buffer adapter card is installed.

This test verifies that each register on the 4.5 Mb/s buffer adapter card can be reset correctly. This is done by first writing to the register, then issuing the reset and verifying that the register is reset.

Checkers Tests

This test section forces errors and checks all the error detecting circuitry on the 4.5 Mb/s buffer adapter card.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

Routine EE33 displays different combinations of the screens shown under ERROR DISPLAY in the following charts. The different failures and the different tests determine which screens are displayed. You can step through the screens you receive on your maintenance device, and locate the matching screen and its explanation in the chart.

If the 4.5 Mb/s buffer adapter card is installed and an error occurs, an additional error display shows the contents of the buffer adapter card external registers.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

Data Buffer Data Path Test - Routine EE33 (Continued)

Read Forward Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113
BU4021	This error is set when either the CMS or CMFL installed bits are not on when expected.	See steps 1 and 2 at the top of this column.	
BU4022	This error is set when the CMS reg compbusy bit does not come on after a reset.	See steps 1 and 2 at the top of this column.	
BU4023	This error is set when the CMS reg compbusy bit does not go off within 30 usec of a reset.	See steps 1 and 2 at the top of this column.	
BU4024	This error is set when either the CMS or CMFL installed bits are on when not expected.	See steps 1 and 2 at the top of this column.	
BU4025	After writing 255 data bytes through the channel write data path, the hardware detected errors.	See the FSI section for error code D5nn.	
BU4026	The hardware detected a data compare error. The data written did not compare with the data read.	See the FSI section for error code D6nn.	
BU4027	The hardware detected an error after reading 255 bytes of data to initialize intermediate storage.	See the FSI section for error code D6nn.	
BU4028	The hardware detected an error after a 135 byte write of X'87' through X'01' followed by a channel store crc.	See the FSI section for error code D5nn.	
BU4029	'Service in' or 'Data in' did not become active within 520 microseconds during a read operation.	See the FSI section for error code D5nn.	
BU402A	After the first 45 bytes of data have been read, suppress out is activated and data in or service became active before 61 microseconds expired.	See the FSI section for error code D5nn.	
BU402B	The buffer channel is stopped and a ck 1, xr, or buffer device error was detected by hardware.	See the FSI section for error code D6nn.	
BU402C	The BCSE contains an unexpected value. The actual value is displayed. The expected value is either X'C0000' or X'20000'.	See the FSI section for error code D5nn.	
BU402D	The buffer channel pointer does not = X'0005' indicating data transfer did not end correctly	See the FSI section for error code D5nn.	
BU402E	The status bits are not correct during the ending sequence of a channel read operation.	See steps 1 and 2 at the top of this column.	
BU402F	Reserved		
BU4030	The cmp allowed bit is on in the CMS External Register when not expected.	See steps 1 and 2 at the top of this column.	

ERROR DISPLAYS

Note: You will see this error display only if the 4.5 Mb/s buffer adapter card is installed.

```
CMS = AA, CTXE = EE
CMM = BB, CMD0 = FF
CHM = CC, CMD1 = GG
CTE0= DD, CMFL = HH
```

AA Contents of the CCMP Status Register
BB Contents of the CCMP Mode Register
CC Contents of the Channel Mode Register
DD Contents of the C2P0 Error 0 Register
EE Contents of the C2P0 XR Error Register
FF Contents of the CCMP Diagnostic 0 Register
GG Contents of the CCMP Diagnostic 1 Register
HH Contents of the CCMP Feature Level Register

```
nnnnnn
ERA=ra,ERB=rb
PSR=xx,PER=pp,XRA=aa
MTI=mm,MDI=md
```

nnnnnn = Failure ID
** = no error set

aa = Contents of XRA reg
md = Contents of MDI reg
mm = Contents of MTI reg
ra = Contents of ERA reg
rb = Contents of ERB reg
pp = Bits 0-3 of PER reg
xx = Contents of PSR reg

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
```

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
BDG1 = dd
```

aaaa = Expected write data bbbb = Data that was read
cccc = Buffer address of the data in error
dd = Contents of the BDG1 register

```
nnnnnn
    BCP   BDP
EXP kkll  oopp
ACT iijj  mmnn
```

nnnnnn = Failure ID

ii = Actual buffer channel pointer high
jj = Actual buffer channel pointer low
kk = Expected buffer channel pointer high value
ll = Expected buffer channel pointer low value
mmnn = Actual buffer device pointer contents
oopp = Expected buffer device pointer contents

```
BCSE=abcde
BDSE=fghij
BWRP=cc
```

```
nnnnnn
    BCSE   BDSE
EXP klmno  pqrst
ACT abcde  fghij
```

nnnnnn = Failure ID
* = No errors were set
a = Buffer channel status and error register bits 0-3
b = BCSE channel error group 0
c = BCSE channel error group 1
cc = Contents of the buffer wrap register
d = BCSE channel error group 2
e = BCSE channel error group 3
f = Buffer device status and error register bits 0-3
g = BDSE device error group 0
h = BDSE device error group 1
i = BDSE device error group 2
j = BDSE device error group 3
k = Expected buffer channel status and error register bits 0-3
l = Expected BCSE channel error group 0
m = Expected BCSE channel error group 1
n = Expected BCSE channel error group 2
o = Expected BCSE channel error group 3
p = Expected buffer device status and error
q = Expected BDSE device error group 0
r = Expected BDSE device error group 1
s = Expected BDSE device error group 2
t = Expected BDSE device error group 3

* These FRUs are EC sensitive. FRU112 may not be present. See CARR-CU 7.

Error Displays

ERROR DISPLAYS

Note: This error display is only present if you have either

data compaction or a 4.5 mb/s channel feature.

```
CMS  = AA, CTXE = EE
CMM  = BB, CMD0 = FF
CIM  = CC, CMD1 = GG
CTE0 = DD, CMFL = HH
```

AA	Contents of the CCMP Status Register	EE	Contents of the C3P0 Error Register
BB	Contents of the CCMP Mode Register	FF	Contents of the CCMP Diagnostic 0 Register
CC	Contents of the Channel Mode Register	GG	Contents of the CCMP Diagnostic 1 Register
DD	Contents of the C3P0 Error 0 Register	HH	Contents of the CCMP Feature Level Register

Note: This error display is only present if you have the data compaction feature.

```
CP0E0 = AA, CP2E0 = EE
CP0E1 = BB, CP2E1 = FF
CP1E0 = CC, CP3E0 = GG
CP1E1 = DD, CP3E1 = HH
```

AA	Contents of the Comp0 Error 0 Register	EE	Contents of the Comp2 Error 0 Register
BB	Contents of the Comp0 Error 1 Register	FF	Contents of the Comp2 Error 1 Register
CC	Contents of the Comp1 Error 0 Register	GG	Contents of the Comp3 Error 0 Register
DD	Contents of the Comp1 Error 1 Register	HH	Contents of the Comp3 Error 1 Register

Note: This error display is only present if you have the data compaction feature.

```
CP0C = AA, CP0D = EE
CP1C = BB, CP1D = FF
CP2C = CC, CP2D = GG
CP3C = DD, CP3D = HH
```

AA	Contents of the Comp0 Configuration Register	EE	Contents of the Comp0 Diagnostic Regiister
BB	Contents of the Comp1 Configuration Register	FF	Contents of the Comp1 Diagnostic Regiister
CC	Contents of the Comp2 Configuration Register	GG	Contents of the Comp2 Diagnostic Regiister
DD	Contents of the Comp3 Configuration Register	HH	Contents of the Comp3 Diagnostic Regiister

Note: This error display is only present if you have the data compaction feature.

```
CP0B0-3 = AAAAAAAA
CP1B0-3 = BBBBBBBB
CP2B0-3 = CCCCCCCC
CP3B0-3 = DDDDDDDD
```

AAAAAAAA = Channel Byte Count for Comp 0
BBBBBBBB = Channel Byte Count for Comp 1
CCCCCCCC = Channel Byte Count for Comp 2
DDDDDDDD = Channel Byte Count for Comp 3

ERROR DISPLAYS

```
nnnnnn
ERA=ra, ERB=rb
PSR=xx, PER=pp, XRA=aa
MTI=md, MDI=mm
```

nnnnnn = Failure ID
** = no error set

aa = Contents of XRA reg ra = Contents of ERA reg
md = Contents of MDI reg rb = Contents of ERB reg
mm = Contents of MTI reg pp = Contents of PER reg
                          xx = Contents of PSR reg

```
DATA
DATA READ   = bbbb
BUFFER ADR  = cccc
```

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
REM = gg, EXP = hh
```

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
BDG1 = dd
```

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
BCSS = ee EXP = ff
```

aaaa = Expected write data
bbbb = Data that was read
cccc = Buffer address of data in error
dd = Contents of the BDG1 register
ee = Contents of the BCSS register
ff = Expected contents of the BCSS register
gg = Remainder register count
hh = Expected remainder register count

```
nnnnnn
     BCP   BDP
EXP kkll   oopp
ACT iijj   mmnn
```

nnnnnn = Failure ID

ii = Actual buffer channel pointer high
jj = Actual buffer channel pointer low
kk = Expected buffer channel pointer low value
mmnn = Actual buffer device pointer contents
oopp = Expected buffer device pointer contents

```
BCSE = abcde
BDSE = fjhij
BWRP = cc
```

```
nnnnnn
    BCSE   BDSE
EXP klmno pqrst
ACT abcde fghij
```

nnnnnn = Failure ID
* = No errors were set
a = Buffer channel status and error register bits 0-3
b = BCSE channel error group 0
c = BCSE channel error group 1
cc = Contents of the buffer wrap register
d = BCSE channel error group 2
e = BCSE channel error group 3
f = Buffer device status and error register bits 0-3
g = BDSE channel error group 0
h = BDSE channel error group 1
i = BDSE channel error group 2
j = BDSE channel error group 3
k = Expected buffer channel status and error register bits 0-3
l = Expected BCSE channel error group 0
m = Expected BCSE channel error group 1
n = Expected BCSE channel error group 2
o = Expected BCSE channel error group 3
p = Expected buffer device status and error
q = Expected BCSE channel error group 0
r = Expected BCSE channel error group 1
s = Expected BCSE channel error group 2
t = Expected BCSE channel error group 3

```
BDG1 = dd
BCSS = ee
EXP  = ff
```

dd = Contents of the BDG1 register
ee = Contents of the BCSS register
ff = Expected contents of the BCSS register

0 0 0 0 0 0 0 0 0 0

Note: See the error displays on DIAG 112.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	See error display on DIAG 112
BU4021	This error is set when either the CMS or CMFL installed bits are not on when expected.	See steps 1 and 2 at the top of this column.		
BU4022	This error is set when the CMS reg compbusy bit does not come on after a reset.	See steps 1 and 2 at the top of this column.		
BU4023	This error is set when the CMS reg compbusy bit does not go off within 30 usec of a reset.	See steps 1 and 2 at the top of this column.		
BU4024	This error is set when either the CMS or CMFL installed bits are on when not expected.	See steps 1 and 2 at the top of this column.		
BU4025	After writing 255 data bytes through the channel write data path, the hardware detected errors.	See the FSI section for error code D5nn.		
BU4026	The hardware detected a data compare error. The data written did not compare with the data read.	See the FSI section for error code D6nn.		
BU4027	The hardware detected an error after reading 255 bytes of data to initialize intermediate storage.	See the FSI section for error code D6nn.		
BU4028	The hardware detected an error after a 135 byte write of X'87' through X'01' followed by a channel store crc.	See the FSI section for error code D5nn.		
BU4029	'Service in' or 'Data in' did not become active within 520 microseconds during a read operation.	See the FSI section for error code D5nn.		
BU402A	After the first 45 bytes of data have been read, suppress out is activated and data in or service became active before 61 microseconds expired.	See the FSI section for error code D5nn.		
BU402B	The buffer channel is stopped and a ck 1, xr, or buffer device error was detected by hardware.	See the FSI section for error code D6nn.		
BU402C	The BCSE contains an unexpected value. The actual value is displayed. The expected value is either X'C0000' or X'20000'.	See the FSI section for error code D5nn.		
BU402D	The buffer channel pointer does not = X'0005' indicating data transfer did not end correctly	See the FSI section for error code D5nn.		
BU402E	The status bits are not correct during the ending sequence of a channel read operation.	See steps 1 and 2 at the top of this column.		
BU402F	Reserved			
BU4030	The Improved Data Recording Capability allowed bit is on in the CMS External Register when not expected.	See steps 1 and 2 at the top of this column.		

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	See error display on DIAG 112
BU4031	The hardware detected errors after a 135 byte write of X'87' through X'01' followed by a channel store crc.	See FSI section for error code D5nn.		
BU4032	'Service in' or 'data in' did not become active within 520 microseconds while reading backward	See FSI section for error code D5nn.		
BU4033	The first 45 bytes have been read, and 'suppress out' is activated. Either 'data in' or 'service in' was active before a 61 microseconds period ended.	See FSI section for error code D5nn.		
BU4034	The buffer channel operation is stopped and the hardware has detected check 1, XR, or a device buffer error.	See steps 1 and 2 at the top of this chart. or see the FSI section for error code D6nn.		
BU4035	The BCSE contains an unexpected value. The actual value is displayed. The expected value is X'C0000'.	See the FSI section for error code D5nn.		
BU4036	The buffer channel pointer is not X'0005' after stop out is activated, which indicates that the data transfer did not end correctly.	See the FSI section for error code D5nn.		
BU4037	The pad counter value in the BCSS register is incorrect on a Read Backward command.	See the FSI section for error code D5nn.		
BU4038	The status bits are not correct during the ending sequence of a channel read backwards operation.	See steps 1 and 2 at the top of this chart.		

* These FRUs are EC sensitive. FRU112 may not be present.
See CARR-CU 7.

0 0 0 0 0 0 0 0 0 0

Data Buffer Data Path Test - Routine EE33 (Continued)

Read Backward Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113
BU4031	The hardware detected errors after a 135 byte write of X'87' through X'01' followed by a channel store crc.	See FSI section for error code D5nn.	
BU4032	'Service in' or 'data in' did not become active within 520 microseconds while reading backward	See FSI section for error code D5nn.	
BU4033	The first 45 bytes have been read, and 'suppress out' is activated. Either 'data in' or 'service in' was active before a 61 microseconds period ended.	See FSI section for error code D5nn.	
BU4034	The buffer channel operation is stopped and the hardware has detected check 1, XR, or a device buffer error.	See steps 1 and 2 at the top of this chart. or see the FSI section for error code D6nn.	
BU4035	The BCSE contains an unexpected value. The actual value is displayed. The expected value is X'C0000'.	See the FSI section for error code D5nn.	
BU4036	The buffer channel pointer is not X'0005' after stop out is activated, which indicates that the data transfer did not end correctly.	See the FSI section for error code D5nn.	
BU4037	The pad counter value in the BCSS register is incorrect on a Read Backward command.	See the FSI section for error code D5nn.	
BU4038	The status bits are not correct during the ending sequence of a channel read backwards operation.	See steps 1 and 2 at the top of this chart.	

ERROR DISPLAYS

Note: You will see this error display only if the 4.5 Mb/s buffer adapter card is installed.

```
CMS = AA, CTXE = EE
CMM = BB, CMD0 = FF
CHM = CC, CMD1 = GG
CTE0= DD, CMFL = HH
```

AA Contents of the CCMP Status Register
BB Contents of the CCMP Mode Register
CC Contents of the Channel Mode Register
DD Contents of the C2P0 Error 0 Register
EE Contents of the C2P0 XR Error Register
FF Contents of the CCMP Diagnostic 0 Register
GG Contents of the CCMP Diagnostic 1 Register
HH Contents of the CCMP Feature Level Register

```
nnnnnn
ERA=ra,ERB=rb
PSR=xx,PER=pp,XRA=aa
MTI=mm,MDI=md
```

nnnnnn = Failure ID
** = no error set

aa = Contents of XRA reg
md = Contents of MDI reg
mm = Contents of MTI reg
ra = Contents of ERA reg
rb = Contents of ERB reg
pp = Bits 0-3 of PER reg
xx = Contents of PSR reg

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
```

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
BDG1 = dd
```

aaaa = Expected write data bbbb = Data that was read
cccc = Buffer address of the data in error
dd = Contents of the BDG1 register

```
nnnnnn
     BCP   BDP
EXP kkll   oopp
ACT iijj   mmnn
```

nnnnnn = Failure ID

ii = Actual buffer channel pointer high
jj = Actual buffer channel pointer low
kk = Expected buffer channel pointer high value
ll = Expected buffer channel pointer low value
mmnn = Actual buffer device pointer contents
oopp = Expected buffer device pointer contents

```
BCSE=abcde
BDSE=fghij
BWRP=cc
```

```
nnnnnn
     BCSE   BDSE
EXP klmno   pqrst
ACT abcde   fghij
```

nnnnnn = Failure ID
* = No errors were set
a = Buffer channel status and error register bits 0-3
b = BCSE channel error group 0
c = BCSE channel error group 1
cc = Contents of the buffer wrap register
d = BCSE channel error group 2
e = BCSE channel error group 3
f = Buffer device status and error register bits 0-3
g = BDSE device error group 0
h = BDSE device error group 1
i = BDSE device error group 2
j = BDSE device error group 3
k = Expected buffer channel status and error register bits 0-3
l = Expected BCSE channel error group 0
m = Expected BCSE channel error group 1
n = Expected BCSE channel error group 2
o = Expected BCSE channel error group 3
p = Expected buffer device status and error
q = Expected BDSE device error group 0
r = Expected BDSE device error group 1
s = Expected BDSE device error group 2
t = Expected BDSE device error group 3

* These FRUs are EC sensitive. FRU112 may not be present. See CARR-CU 7

Read Overrun Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113
BU4039	An XR error or a Check 1 was detected.	See steps 1 and 2 at the top of this column.	
BU403A	The content of the BCSE does not equal the expected content. The content is displayed. The expected content is 1400, any channel error, channel overrun error, and host channel adapter error.	See the FSI section for error code D5nn.	
BU403B	The buffer channel pointer is expected to contain 0008 after an overrun is detected. The content of the buffer channel pointer is displayed.	See the FSI section for error code D5nn.	
BU403C	The content of the BDSE does not equal the expected content. The content is displayed. The expected content is 5C800, any device error, device overrun error, and read data flow error.	See the FSI section for error code D6nn.	
BU403D	The buffer device pointer is expected to contain 0008 after an overrun is detected. The content of the buffer device pointer is displayed.	See the FSI section for error code D6nn.	

ERROR DISPLAYS

Note: You will see this error display only if the 4.5 Mb/s buffer adapter card is installed.

```
CMS = AA, CTXE = EE
CMM = BB, CMD0 = FF
CHM = CC, CMD1 = GG
CTE0= DD, CMFL = HH
```

AA	Contents of the CCMP Status Register	EE	Contents of the C2PO XR Error Register
BB	Contents of the CCMP Mode Register	FF	Contents of the CCMP Diagnostic 0 Register
CC	Contents of the Channel Mode Register	GG	Contents of the CCMP Diagnostic 1 Register
DD	Contents of the C2PO Error 0 Register	HH	Contents of the CCMP Feature Level Register

```
nnnnnn
ERA=ra, ERB=rb
PSR=xx, PER=pp,XRA=aa
MTI=mm,MDI=md
```

nnnnnn = Failure ID
** = No errors were set
aa = Contents of the external register address
md = Contents of the maintenance data in register
mm = Contents of the maintenance tag in register
ra = Contents of error register A
rb = Contents of error register B
pp = Contents of processor error register bits 0-3
xx = Contents of the processor status register register

```
nnnnnn
     BCP    BDP
EXP kkll    oopp
ACT iijj    mmnn
```

nnnnnn = Failure ID
ii = Contents of buffer channel pointer low
jj = Contents of buffer channel pointer high
kk = Expected contents of buffer channel pointer high
ll = Expected contents of buffer channel pointer low
mmnn = Contents of buffer device pointer
oopp = Expected contents of buffer device pointer

```
nnnnnn
     BCSE    BDSE
EXP klmno    pqrst
ACT abcde    fghij
```

nnnnnn = Failure ID
* = No errors were set
a = Buffer channel status and error register bits 0-3
b = BCSE channel error group 0
c = BCSE channel error group 1
d = BCSE channel error group 2
e = BCSE channel error group 3
f = Buffer device status and error register bits 0-3
g = BDSE device error group 0
h = BDSE device error group 1
i = BDSE device error group 2
j = BDSE device error group 3
k = Expected buffer channel statu and error register bits 0-3
l = Expected BCSE channel error group 0
m = Expected BCSE channel error group 1
n = Expected BCSE channel error group 2
o = Expected BCSE channel error group 3
p = Expected buffer device status and error
q = Expected BDSE device error group 0
r = Expected BDSE device error group 1
s = Expected BDSE device error group 2
t = Expected BDSE device error group 3

* This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Write Overrun Test

Note: See the error displays on DIAG 112.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	See error display on DIAG 112
BU4039	An XR error or a Check 1 was detected.	See steps 1 and 2 at the top of this column.		
BU403A	The content of the BCSE does not equal the expected content. The content is displayed. The expected content is 1400, any channel error, channel overrun error, and host channel adapter error.	See the FSI section for error code D5nn.		
BU403B	The buffer channel pointer is expected to contain 0008 after an overrun is detected. The content of the buffer channel pointer is displayed.	See the FSI section for error code D5nn.		
BU403C	The content of the BDSE does not equal the expected content. The content is displayed. The expected content is 5C800, any device error, device overrun error, and read data flow error.	See the FSI section for error code D6nn.		
BU403D	The buffer device pointer is expected to contain 0008 after an overrun is detected. The content of the buffer device pointer is displayed.	See the FSI section for error code D6nn.		
BU403E	An XR error or a Check 1 was detected.	See steps 1 and 2 at the top of this column.		
BU403F	The content of the BCSE does not equal the expected content. The content is displayed. The expected content is 1C100, any channel error, channel overrun error, and host channel adapter error.	See the FSI section for error code D5nn.		
BU4040	The buffer channel pointer is expected to contain 0008 after an overrun is detected. The content of the buffer channel pointer is displayed.	See the FSI section for error code D5nn.		
BU4041	The content of the BDSE does not equal the expected content. The content is displayed. The expected content is 1C800, any device error, device overrun error, and read data flow error.	See the FSI section for error code D6nn.		
BU4042	The buffer device pointer is expected to contain 0008 after an overrun is detected. The content of the buffer device pointer is displayed.	See the FSI section for error code D6nn.		

* This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Write Overrun Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113
BU403E	An XR error or a Check 1 was detected.	See steps 1 and 2 at the top of this column.	
BU403F	The content of the BCSE does not equal the expected content. The content is displayed. The expected content is 1C100, any channel error, channel overrun error, and host channel adapter error.	See the FSI section for error code D5nn.	
BU4040	The buffer channel pointer is expected to contain 0008 after an overrun is detected. The content of the buffer channel pointer is displayed.	See the FSI section for error code D5nn.	
BU4041	The content of the BDSE does not equal the expected content. The content is displayed. The expected content is 1C800, any device error, device overrun error, and read data flow error.	See the FSI section for error code D6nn.	
BU4042	The buffer device pointer is expected to contain 0008 after an overrun is detected. The content of the buffer device pointer is displayed.	See the FSI section for error code D6nn.	

ERROR DISPLAYS

Note: You will see this error display only if the 4.5 Mb/s buffer adapter card is installed.

```
CMS = AA, CTXE = EE
CMM = BB, CMD0 = FF
CHM = CC, CMD1 = GG
CTE0= DD, CMFL = HH
```

AA	Contents of the CCMP Status Register	EE	Contents of the C2P0 XR Error Register
BB	Contents of the CCMP Mode Register	FF	Contents of the CCMP Diagnostic 0 Register
CC	Contents of the Channel Mode Register	GG	Contents of the CCMP Diagnostic 1 Register
DD	Contents of the C2P0 Error 0 Register	HH	Contents of the CCMP Feature Level Register

```
nnnnnn
ERA=ra, ERB=rb
PSR=xx, PER=pp,XRA=aa
MTI=mm,MDI=md
```

nnnnnn = Failure ID
** = No errors were set
aa = Contents of the external register address
md = Contents of the maintenance data in register
mm = Contents of the maintenance tag in register
ra = Contents of error register A
rb = Contents of error register B
pp = Contents of processor error register bits 0-3
xx = Contents of the processor status register register

```
BCSE = abcde
BDSE = fghi
BWRP = cc
```

nnnnnn = Failure ID
* = No errors were set
a = Buffer channel status and error register bits 0-3
b = BCSE channel error group 0
c = BCSE channel error group 1
cc = Contents of the buffer wrap register
d = BCSE channel error group 2
e = BCSE channel error group 3
f = Buffer device status and error register bits 0-3
g = BDSE device error group 0
h = BDSE device error group 1
i = BDSE device error group 2
j = BDSE device error group 3
k = Expected buffer channel statu and error register bits 0-3
l = Expected BCSE channel error group 0
m = Expected BCSE channel error group 1
n = Expected BCSE channel error group 2
o = Expected BCSE channel error group 3
p = Expected buffer device status and error
q = Expected BDSE device error group 0
r = Expected BDSE device error group 1
s = Expected BDSE device error group 2
t = Expected BDSE device error group 3

```
nnnnnn
    BCSE    BDSE
EXP klmno   pqrst
ACT abcde   fghij
```

```
nnnnnn
    BCP     BDP
EXP kkll    oopp
ACT iijj    mmnn
```

nnnnnn = Failure ID
ii = Contents of buffer channel pointer low
jj = Contents of buffer channel pointer high
kk = Expected contents of buffer channel pointer high
ll = Expected contents of buffer channel pointer low
mmnn = Contents of buffer device pointer
oopp = Expected contents of buffer device pointer

* This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Separation Test

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	Note: You will see this error display only if the 4.5 Mb/s buffer adapter card is installed. CMS = AA, CTXE = EE CMM = BB, CMD0 = FF CHM = CC, CMD1 = GG CTE0= DD, CMFL = HH AA Contents of the CCMP Status Register BB Contents of the CCMP Mode Register CC Contents of the Channel Mode Register DD Contents of the C2PO Error 0 Register EE Contents of the C2PO XR Error Register FF Contents of the CCMP Diagnostic 0 Register GG Contents of the CCMP Diagnostic 1 Register HH Contents of the CCMP Feature Level Register
BU4043	'Service in' or 'data in' did not become active in 703 microseconds.	See the FSI section for error code D5nn.		nnnnnn ERA=ra,ERB=rb PSR=xx,PER=pp,XRA=aa MTI=mm, MDI=md nnnnnn = Failure ID ** = no error set aa = Contents of XRA reg ra = Contents of ERA reg md = Contents of MDI reg rb = Contents of ERB reg mm = Contents of MTI reg pp = Bits 0-3 of PER reg xx = Contents of PSR reg
BU4044	The channel read more than 128 bytes, which indicates the channel is overrunning the drive.	See the FSI section for error code D5nn.		BCSE=abcde BDSE=fghij BWRP=cc nnnnnn BCSE BDSE EXP klmno pqrst ACT abcde fghij
BU4045	An XR error or check 1 was detected.	See steps 1 and 2 at the top of this chart.		nnnnnn = Failure ID * = No errors were set a = Buffer channel status and error register bits 0-3 b = BCSE channel error group 0 c = BCSE channel error group 1 cc = Contents of the buffer wrap register d = BCSE channel error group 2 e = BCSE channel error group 3 f = Buffer device status and error register bits 0-3 g = BDSE device error group 0 h = BDSE device error group 1 i = BDSE device error group 2 j = BDSE device error group 3 k = Expected buffer channel status and error register bits 0-3 l = Expected BCSE channel error group 0 m = Expected BCSE channel error group 1 n = Expected BCSE channel error group 2 o = Expected BCSE channel error group 3 p = Expected buffer device status and error q = Expected BDSE device error group 0 r = Expected BDSE device error group 1 s = Expected BDSE device error group 2 t = Expected BDSE device error group 3
BU4046	The content of the BDSE does not = the expected content. The expected content is 70000. The content of the BCSR does not = the expected content. The expected content is 90000.	See the FSI section for error code D6nn.		
BU4047	The buffer device remainder register does not = 05 after the last read of six bytes.	See the FSI section for error code D6nn.		
BU4048	The buffer device pointer expected content is 0008. The buffer channel pointer expected content is 0009.	See the FSI section for error code D6nn.		
BU4049	The BCSS content doe not = the expected content. The expected content is 07.	See the FSI section for error code D5nn.		DATA EXP/WRT= aaaa DATA READ = bbbb BUFFER ADR = cccc REM = gg, EXP = hh DATA EXP/WRT= aaaa DATA READ = bbbb BUFFER ADR = cccc BCSS = ee, EXP = ff aaaa = Expected write data bbbb = Data that was read cccc = Buffer address of the data in error ee = Contents of the buffer channel intermediate storage address register ff = Expected contents of the buffer channel intermediate storage address register hh = Remainder register expected count
				nnnnnn BCP BDP EXP kkll oopp ACT iijj mmnn nnnnnn = Failure ID ii = Actual buffer channel pointer high jj = Actual buffer channel pointer low kk = Expected buffer channel pointer high value ll = Expected buffer channel pointer low value mmnn = Actual buffer device pointer contents oopp = Expected buffer device pointer contents

* These FRUs are EC sensitive. FRU112 may not be present. See CARR-CU 7.

0 0 0 3 0 0 0 0 3 0

Separation Test

Note: See the error displays on DIAG 112.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	See error display on DIAG 112
BU4043	'Service in' or 'data in' did not become active in 703 microseconds.	See the FSI section for error code D5nn.		
BU4044	The channel read more than 128 bytes, which indicates the channel is overrunning the drive.	See the FSI section for error code D5nn.		
BU4045	An XR error or check 1 was detected.	See steps 1 and 2 at the top of this chart.		
BU4046	The content of the BDSE does not = the expected content. The expected content is 70000. The content of the BCSR does not = the expected content. The expected content is 90000.	See the FSI section for error code D6nn.		
BU4047	The buffer device remainder register does not = 05 after the last read of six bytes.	See the FSI section for error code D6nn.		
BU4048	The buffer device pointer expected content is 0008. The buffer channel pointer expected content is 0009.	See the FSI section for error code D6nn.		
BU4049	The BCSS content doe not = the expected content. The expected content is 07.	See the FSI section for error code D5nn.		

* These FRUs are EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	See error display on DIAG 112
BU404A	A channel control reset failed during an external register reset test.	See steps 1 and 2 at the top of this chart.		
BU404B	A check 4 reset failed during an external register reset test.	See steps 1 and 2 at the top of this chart.		
BU404C	A check 5 reset failed during an external register reset test.	See steps 1 and 2 at the top of this chart.		
BU404D	A hardware reset failed during an external register reset test	See steps 1 and 2 at the top of this chart.		
BU404E	A buffer register that can be reset by a POR reset only is found in a reset state and no POR reset was issued.	See steps 1 and 2 at the top of this chart.		
BU404F	The 300NS clock ring error indicator (CTEO Reg bit 2) is not turned on when forced.	See steps 1 and 2 at the top of this chart.		
BU4050	The any error bit indicator (CMS Reg Bit 7) is not turned on by one of the other errors.	See steps 1 and 2 at the top of this chart.		
BU4051	The feature level parity error indicator (CTEO Reg bit 6) is not turned on when forced.	See steps 1 and 2 at the top of this chart		
BU4052	The channel overrun error indicator (CTEO Reg Bit 0) is not working correctly.	See steps 1 and 2 at the top of this chart		
BU4053	The transferr complete/overrun error indicator (CMS Reg Bit 3) is not working correctly.	See steps 1 and 2 at the top of this chart		
BU4054	The check 5 reset does not work correctly during a channel operation.	See steps 1 and 2 at the top of this chart		
BU4055	Service in or data in is not working correctly during a channel operation.	See steps 1 and 2 at the top of this chart		
BU4056	The bc toggle error indicator (CTEO Reg Bit 4) is not on when forced.	See steps 1 and 2 at the top of this chart		
BU4057	Either the C3PO data parity error or the BC channel parity error indicators (Comp Error 1 Reg Bits 0 or 3) are not on when forced.	See steps 1 and 2 at the top of this chart		
BU4058	Either the BC data parity error or the channel data parity error indicators (CTEO Reg Bits 3 and 5) are not on when forced.	See steps 1 and 2 at the top of this chart		

0 0 0 0 0 0 0 0 0 0

Data Buffer Controls Test - Routine EE33 (Continued)

Buffer Adapter Tests

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.
BU404A	A channel control reset failed during an external register reset test.	See steps 1 and 2 at the top of this chart.
BU404B	A check 4 reset failed during an external register reset test.	See steps 1 and 2 at the top of this chart.
BU404C	A check 5 reset failed during an external register reset test.	See steps 1 and 2 at the top of this chart.
BU404D	A hardware reset failed during an external register reset test	See steps 1 and 2 at the top of this chart.
BU404E	A buffer register that can be reset by a POR reset only is found in a reset state and no POR reset was issued.	See steps 1 and 2 at the top of this chart.
BU404F	The 300NS clock ring error indicator (CTEO Reg bit 2) is not turned on when forced.	See steps 1 and 2 at the top of this chart.
BU4050	The any error bit indicator (CMS Reg Bit 7) is not turned on by one of the other errors.	See steps 1 and 2 at the top of this chart.
BU4051	The feature level parity error indicator (CTEO Reg bit 6) is not turned on when forced.	See steps 1 and 2 at the top of this chart
BU4052	The channel overrun error indicator (CTEO Reg Bit 0) is not working correctly.	See steps 1 and 2 at the top of this chart
BU4053	The transferr complete/overrun error indicator (CMS Reg Bit 3) is not working correctly.	See steps 1 and 2 at the top of this chart
BU4054	The check 5 reset does not work correctly during a channel operation.	See steps 1 and 2 at the top of this chart
BU4055	Service in or data in is not working correctly during a channel operation.	See steps 1 and 2 at the top of this chart
BU4056	The bc toggle error indicator (CTEO Reg Bit 4) is not on when forced.	See steps 1 and 2 at the top of this chart
BU4057	Either the C3PO data parity error or the BC channel parity error indicators (Comp Error 1 Reg Bits 0 or 3) are not on when forced.	See steps 1 and 2 at the top of this chart
BU4058	Either the BC data parity error or the channel data parity error indicators (CTEO Reg Bits 3 and 5) are not on when forced.	See steps 1 and 2 at the top of this chart

FRUs: FRU114, FRU120, *FRU112, *FRU113

Note: You will see this error display only if the 4.5 Mb/s buffer adapter card is installed.

```
CMS = AA, CTXE = EE
CMM = BB, CMD0 = FF
CHM = CC, CMD1 = GG
CTEO= DD, CMFL = HH
```

AA Contents of the CCMP Status Register
BB Contents of the CCMP Mode Register
CC Contents of the Channel Mode Register
DD Contents of the C2PO Error 0 Register
EE Contents of the C2PO XR Error Register
FF Contents of the CCMP Diagnostic 0 Register
GG Contents of the CCMP Diagnostic 1 Register
HH Contents of the CCMP Feature Level Register

```
nnnnnn
ERA=ra,ERB=rb
PSR=xx,PER=pp,XRA=aa
MTI=mm,MDI=md
```

nnnnnn = Failure ID
** = no error set

aa = Contents of XRA reg
md = Contents of MDI reg
mm = Contents of MTI reg
ra = Contents of ERA reg
rb = Contents of ERB reg
pp = Bits 0-3 of PER reg
xx = Contents of PSR reg

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
```

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
BDG1 = dd
```

aaaa = Expected write data bbbb = Data that was read
cccc = Buffer address of the data in error
dd = Contents of the BDG1 register

```
nnnnnn
    BCP   BDP
EXP kkll  oopp
ACT iijj  mmnn
```

nnnnnn = Failure ID

ii = Actual buffer channel pointer high
jj = Actual buffer channel pointer low
kk = Expected buffer channel pointer high value
ll = Expected buffer channel pointer low value
mmnn = Actual buffer device pointer contents
oopp = Expected buffer device pointer contents

```
BCSE=abcde
BDSE=fghij
BWRP=cc
```

```
nnnnnn
    BCSE   BDSE
EXP klmno  pqrst
ACT abcde  fghij
```

nnnnnn = Failure ID
* = No errors were set
a = Buffer channel status and error register bits 0-3
b = BCSE channel error group 0
c = BCSE channel error group 1
cc = Contents of the buffer wrap register
d = BCSE channel error group 2
e = BCSE channel error group 3
f = Buffer device status and error register bits 0-3
g = BDSE device error group 0
h = BDSE device error group 1
i = BDSE device error group 2
j = BDSE device error group 3
k = Expected buffer channel status and error register bits 0-3
l = Expected BCSE channel error group 0
m = Expected BCSE channel error group 1
n = Expected BCSE channel error group 2
o = Expected BCSE channel error group 3
p = Expected buffer device status and error
q = Expected BDSE device error group 0
r = Expected BDSE device error group 1
s = Expected BDSE device error group 2
t = Expected BDSE device error group 3

* These FRUs are EC sensitive. FRU112 may not be present. See CARR-CU 7

Buffer Adapter Tests

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for err code E100 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	Note: You will see this error display only if the 4.5 Mb/s buffer adapter card is installed.
BU4059	Reserved			
BU405A	The write data parity error indicator (CTXE Bit 1) is not on when forced.	See steps 1 and 2 at the top of this chart.		
BU405B	Either the read data parity error or the xr output parity error indicators (CTXE Bits 2 & 3) are not on when forced.	See steps 1 and 2 at the top of this chart.		

```
CMS = AA, CTXE = EE
CMM = BB, CMD0 = FF
CHM = CC, CMD1 = GG
CTEQ= DD, CMFL = HH
```

AA Contents of the CCMP Status Register
BB Contents of the CCMP Mode Register
CC Contents of the Channel Mode Register
DD Contents of the C2PO Error 0 Register
EE Contents of the C2PO XR Error Register
FF Contents of the CCMP Diagnostic 0 Register
GG Contents of the CCMP Diagnostic 1 Register
HH Contents of the CCMP Feature Level Register

```
nnnnnn
ERA=ra,ERB=rb
PSR=xx,PER=pp,XRA=aa
MTI=mm,MDI=md
```

nnnnnn = Failure ID
** = no error set

aa = Contents of XRA reg ra = Contents of ERA reg
md = Contents of MDI reg rb = Contents of ERB reg
mm = Contents of MTI reg pp = Bits 0-3 of PER reg
xx = Contents of PSR reg

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
```

```
DATA EXP/WRT= aaaa
DATA READ   = bbbb
BUFFER ADR  = cccc
BDG1 = dd
```

aaaa = Expected write data bbbb = Data that was read
cccc = Buffer address of the data in error
dd = Contents of the BDG1 register

```
nnnnnn
    BCP   BOP
Exp kkll  oopp
ACT iijj  mmnn
```

nnnnnn = Failure ID
ii = Actual buffer channel pointer high
jj = Actual buffer channel pointer low
kk = Expected buffer channel pointer high value
ll = Expected buffer channel pointer low value
mmnn = Actual buffer device pointer contents
oopp = Expected buffer device pointer contents

```
BCSE=abcde
BDSE=fghij
BWRP=cc
```

```
nnnnnn
    BCSE   BDSE
EXP klmno  pqrst
ACT abcde  fghij
```

nnnnnn = Failure ID
* = No errors were set
a = Buffer channel status and error register bits 0-3
b = BCSE channel error group 0
c = BCSE channel error group 1
cc = Contents of the buffer wrap register
d = BCSE channel error group 2
e = BCSE channel error group 3
f = Buffer device status and error register bits 0-3
g = BDSE device error group 0
h = BDSE device error group 1
i = BDSE device error group 2
j = BDSE device error group 3
k = Expected buffer channel status and error register bits 0-3
l = Expected BCSE channel error group 0
m = Expected BCSE channel error group 1
n = Expected BCSE channel error group 2
o = Expected BCSE channel error group 3
p = Expected buffer device status and error
q = Expected BDSE device error group 0
r = Expected BDSE device error group 1
s = Expected BDSE device error group 2
t = Expected BDSE device error group 3

* These FRUs are EC sensitive. FRU112 may not be present. See CARR-CU 7

Note: See the error displays on DIAG 112.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING OTHER ACTIONS:	1. If ERA or ERB is not 00 go to FSI for error code E100 2. If PSR bit 0 = 1, see EAD 1 for error code code Fnnn.	FRU114 FRU120 *FRU112 *FRU113	See error display on DIAG 112
BU4059	The comp xr error (CTXE Bit 0) is not on when forced.	See steps 1 and 2 at the top of this chart.		
BU405A	The write data parity error indicator (CTXE Bit 1) is not on when forced.	See steps 1 and 2 at the top of this chart.		
BU405B	Either the read data parity error or the xr output parity error indicators (CTXE Bits 2 & 3) are not on when forced.	See steps 1 and 2 at the top of this chart.		
BU405C	CMS Register bit 0 (Comp busy) cannot be reset.	See FSI section for error code DAnn.		
BU405D	An error was detected in the data in or service in tag lines during a read or write operation in Improved Data Recording Capability mode.	See FSI section for error code DAnn.		
BU405E	An ending sequence error was detected during a channel write or a channel read operation.	See FSI section for error code D5nn.		
BU405F	The actual channel byte count does not equal the expected channel byte count.	See FSI section for error code D5nn.		
BU4060	The channel byte count registers in each module do not compare.	See FSI section for error code DAnn.		
BU4061	The Improved Data Recording Capability record trailor does not equal the calculated value.	See FSI section for error code DAnn.		
BU4062	The data read does not equal the data written in Improved Data Recording Capability mode.	See FSI section for error code D6nn.		
BU4063	An error was detected in the service in or data in tag lines.	See FSI section for error code DAnn.		
BU4064	A data compare error was detected in the RAM diagnostic tests.	See FSI section for error code DAnn.		
BU4065	The any error bit (CMS bit 7) was on after running the RAM diagnostic tests.	See FSI section for error code DAnn.		
BU4066	Cannot force the encode does not equal decode error (Comp Error 0 bit 7).	See FSI section for error code DAnn.		
BU4067	Cannot force the initialization error (Comp error 0 bit 6).	See FSI section for error code DAnn.		
BU4068	The any error bit (CMS Bit 7) was not turned on by another Improved Data Recording Capability error.	See FSI section for error code DAnn.		
BU4069	Cannot force the channel adapter interface overflow error (Comp error 1 bit 7).	See FSI section for error code DAnn.		
BU406A	Cannot force the channel byte count overflow error (Comp error 1 bit 6).	See FSI section for error code DAnn.		
BU406B	Cannot force a ca or bc master transfer error (Comp error 1 bits 1 or 4).	See FSI section for error code DAnn.		
BU406C	Cannot force a crc error (Comp error 0 bits 1 through 5).	See FSI section for error code DAnn.		
BU406D	A check 5 reset did not work properly during a channel operation.	See FSI section for error code DAnn.		

0 0 0 0 0 0 0 0 0 0

Control Unit to Drive Bus Out Driver Wrap Test - Routine EE42

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine tests the control unit/drive interconnection as follows:

1. Activates 'select out' to degate all 'bus in' lines from the drives attached to the control unit and tests the 'bus in' lines to make sure that none are active. If any 'bus in' lines are active, the routine issues a clamp command to each drive, one at a time, to isolate the drive with the active 'bus in' lines.

2. Tests the tag-in lines to make sure that none are active. If any tag-in lines are active, the routine issues a clamp command to each drive, one at a time, to isolate the drive with the active tag-in lines.

3. Ripples 'bus out' through all possible bit patterns. The data is then read through the control unit device interrupt register and compared.

Routine Start Address: 2010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Addressing: If a drive address is entered, only that drive is tested. If no drive address is entered, the routine tests all drives in the subsystem. The following screen is used to enter a drive address.

```
DIAG=(EE42)-ENTER:
DRIVE
(xx)
```

Valid Parameters:

xx Drive address (0-F, or 00-0F).
Enter FF to run all drives.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
DI2021	When 'select out' was presented to the drive, bits were still active on the device data bus 'bus in'. A clamp command was sent to all drives, but the active bit condition was not removed from the bus.	See the FSI section for error code 8005. See EAD 1, "Drive Interconnections."	FRU085[1] FRU199 FRU248 FRU118	DI2021 BUS IN = vv INTF x SEL OUT ACTIVE AND ALL DRIVES 'CLAMPED' vv Value of 'bus in' active bits x L for drives 0 through 7, H for drives 8 through F
DI2022	The active device data bus 'bus in' bits were removed from the bus following a clamp command to the drive that was causing the active bits.	See the FSI section for error code 8005. See EAD 1, "Drive Interconnections."	FRU085[1] FRU199 FRU248 FRU118	DI2022 (DR a) ON INTF x HAS BUS IN BITS vv ACTIVE WITH SEL OUT a Drive address x L for drives 0 through 7, H for drives 8 through F vv Value of 'bus in' active bits
DI2023	During the "electronic wrap" of the control unit/drive BI-DI bus, the data returned to the device interrupt register (DIR) did not equal the data sent to the device control bus (DCB) register.	See the FSI section for error code 800A. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU134 FRU115	DI2023 BUS IN DID NOT EQUAL BUS OUT ON INTF x BUS O =vv BUS I =yyy x L for drives 0 through 7, H for drives 8 through F vv Value of 'bus out' bits yy Value of 'bus in' bits
DI2024	A parity error was detected in the device status/error (DSE) register.	See the FSI section for error code 8Bnn. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU116 FRU134	DI2024 PARITY ERROR OCCURRED ON INTF x DATA = vv 'DSE' REG = yy x L for drives 0 through 7, H for drives 8 through F vv Value of 'bus out'/'bus in' yy Value in the DSE register
DI2025	While trying to determine if the subsystem is configured with a dual or single control unit, a status store time-out occurred.	See the FSI section for error code 5360.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	DI2025 TIMEOUT OCCURRED WHILE TRYING TO READ STATUS STORE

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
D12026	Active tag lines were found after setting the device tag register (DTR) to zero. A clamp command was sent to all drives on the serial interconnection, but the active bit condition was not cleared from the DTR register.	See the FSI section for error code 800A. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU134 FRU115	D12026 DTR = vv INTF =x WITH ALL DRIVES 'CLAMPED' vv Value of bits in the device tag register x L for drives 0 through 7, H for drives 8 through F
D12027	The active 'gap in' bit was removed from the device data bus following a clamp command to the drive.	See the FSI section for error code 7502. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118	D12027 (DR a) ON INTF x GAP IN TAG IS ACTIVE x L for drives 0 through 7, H for drives 8 through F a Drive address
D12028	The active 'address in' tag was removed from the device data bus following a clamp command to the drive.	See the FSI section for error code 8009. See EAD 1, "Drive Interconnections."	FRU085[1] FRU199 FRU248 FRU118	D12028 (DR a) ON INTF x ADDRESS IN TAG IS ACTIVE x L for drives 0 through 7, H for drives 8 through F a Drive address
D12029	The active 'status in' tag was removed from the device data bus following a clamp command to the drive.	See the FSI section for error code 8C07. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU116 FRU134	D12029 (DR a) ON INTF x STATUS IN TAG IS ACTIVE x L for drives 0 through 7, H for drives 8 through F a Drive address
D1202A	The active 'clock B in' tag was removed from the device data bus following a clamp command to the drive.	See the FSI section for error code 840C. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU199 FRU248	D1202A (DR a) ON INTF x CLOCKB IN TAG IS ACTIVE x L for drives 0 through 7, H for drives 8 through F a Drive address

[1] This FRU is EC sensitive. See CARR-DR 4.

Control Unit to Drive Bus and Tag Test - Routine EE43

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine checks all tags to and from the drives during initial selection to ensure correct response.

Following selection, 17 bytes of data are transferred to the drive display with the message '********'. (This test does not remove the message on the drive display.) The routine then de-selects the drive and checks all tags to and from the drive during an ending sequence to ensure correct response.

All bits on the BI-DI and tag buses, except device tag register (DTR) bit 4 ('gap in', 'gap out') are tested.

Routine Start Address: 3010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Addressing: If a drive address is entered, only that drive is tested. If no drive address is entered, the routine tests all drives in the subsystem. The following screen is used to enter a drive address.

```
DIAG=(EE43)-ENTER:
DRIVE
(xx)
```

Valid Parameters:

xx Drive address (0-F, or 00-0F).
Enter FF to run all drives.

Diagnostic Aid

The following sequence should be used when isolating difficult control unit to drive interconnection problems.

1. Let the default run the routine on all drives.
2. Check the drive displays and record the address of any drive that does not display the message '********'.
3. Select the routine again and enter the drive address that did not have the correct display. The routine will identify which lines are not responding correctly.

   Note: A valid address table is generated by selecting all drives on the subsystem and checking for 'address in'. If any drive in the subsystem does not respond, the drive will not be in the valid address table and it will not be tested when the "running all drives" default is used.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
DI3021	The drive did not return an 'address in' response to the control unit, after the control unit sent an 'address out' tag along with the drive address on the device data bus 'bus out'.	See the FSI section for error code 8007. See EAD 1, "Drive Interconnections."	FRU085[1] FRU059 FRU049 FRU108 FRU107 FRU105	DI3021 (DR a) ADDRESS IN WAS NOT RETURNED DURING SELECTION a Drive address
DI3022	The one's complement address sent from the drive on the device data bus 'bus in' on did not match the expected address. The expected address was generated from the address sent to the drive on the device data bus 'bus out'.	See the FSI section for error code 800C. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118	DI3022 (DR a) ADDR ON BUS IN IS NOT CORRECT BUS IN=vv EXPECT=xx a Drive address vv Address on device data bus 'bus in' xx Expected address device data bus 'bus out'
DI3023	The device data bus 'address in' from the drive did not drop when the control unit dropped device data bus 'address out.'	See the FSI section for error code 8009. See EAD 1, "Drive Interconnections."	FRU085[1] FRU199 FRU248 FRU118	DI3023 (DR a) ADDR IN STILL ACTIVE AFTER ADDR OUT WAS REMOVED a Drive address

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS		ERROR DISPLAYS
DI3024	The one's complement address sent from the drive on device data bus 'bus in' remained on the bus after the drive dropped device data bus 'address in'.	See the FSI section for error code 8009. See EAD 1, "Drive Interconnections."	FRU085[1] FRU199 FRU248 FRU118	DI3024 (DR a) AFTER ADDR IN BECAME INACTIVE, BUS IN=vv EXPECT=xx a Drive address vv Address on 'bus in' xx Expected address on 'bus out'
DI3025	The drive did not return status when the control unit set device data bus 'command out'.	See the FSI section for error code 8E05. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU116 FRU134	DI3025 (DR a) STATUS IN DID NOT BECOME ACTIVE WITH COMMAND OUT a Drive address
DI3026	The drive returned 'unit check' in the status byte at initial selection time.	See the FSI section for error code 8E06. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU116 FRU134	DI3026 (DR a) UNIT CHECK WAS ACTIVE DURING INITIAL SELECTION a Drive address
DI3027	The drive did not return 'clock B in' when the control unit set device data bus 'clock A out'.	See the FSI section for error code 840A. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU199 FRU248	DI3027 (DR a) CLOCKB IN WAS NOT RETURNED FOR CLOCKA OUT a Drive address
DI3028	'Clock B in' did not drop after the control unit dropped device data bus 'clock A out'.	See the FSI section for error code 8300. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU199 FRU248	DI3028 (DR a) CLOCKB IN WAS STILL ACTIVE AFTER CLOCKA OUT DROPPED a Drive address
DI3029	'Clock B in' did not set during the data transfer of the control byte (byte 0) to the drive.	See the FSI section for error code 840A. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU199 FRU248	DI3029 (DR a) CLOCKB DIDN'T RESPOND AS EXPECTED FOR CONTROL BYTE XFR a Drive address

[1] This FRU is EC sensitive. See CARR-DR 4.

Control Unit to Drive Bus and Tag Test - Routine EE43 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS		ERROR DISPLAYS
D1302A	'Clock B in' did not set during the transfer of 16 bytes of display information to the drive on the device data bus.	See the FSI section for error code 8300. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU199 FRU248	D1302A (DR a) CLOCKB DIDN'T RESPOND AS EXPECTED FOR THE 16 BYTE XFR a Drive address
D1302B	The drive hardware detected an error. Device data bus 'bus in' contains failure information from the drive.	See the FSI section for error code 89nn. See EAD 1, "Drive Interconnections."	FRU085[1] FRU199 FRU248 FRU118 FRU116 FRU134	D1302B (DR a) DR HARDWARE DETECTED CHECK 1 BUS IN = xx a Drive address xx Failure data on 'bus in'
D1302C	The drive did not set device data bus 'status in' during the de-selection sequence.	See the FSI section for error code 8C03. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU116 FRU134	D1302C (DR a) STATUS IN DID NOT BECOME ACTIVE DURING ENDING SEQ. a Drive address
D1302D	The drive did not set 'clock B in' during the ending sequence on the device data bus.	See the FSI section for error code 840A. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU199 FRU248	D1302D (DR a) CLOCKB DID NOT BECOME ACTIVE DURING ENDING SEQ. a Drive address
D1302E	'Clock B in' did not drop during the ending sequence on the device data bus.	See the FSI section for error code 840C. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU199 FRU248	D1302E (DR a) CLOCKB DID NOT FALL DURING THE ENDING SEQUENCE a Drive address

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
D1302F	Device data bus 'status in' did not drop during the ending sequence.	See the FSI section for error code 8C07. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU116 FRU134	D1302F (DR a) STATUS IN DID NOT FALL DURING THE ENDING SEQUENCE a Drive address
D13030	The drive microcode detected an error. Device data bus 'bus in' contains failure information from the drive.	See the FSI section for error code 8Fnn. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118 FRU116 FRU134 FRU199 FRU248	D130230 (DR a) DRIVE MICRO CODE DETECTED ERROR BUS IN = xx a Drive address xx Error information from the drive
D13031	'Unit check' was active in the ending status from the drive.	See the FSI section for error code 8C01.	FRU085[1] FRU118 FRU116 FRU134	D13031 (DR a) UNIT CHECK WAS ACTIVE DURING ENDING SEQUENCE a Drive address
D13032	When defaulting to all available drives, the table build module did not find any drive available. (No drive returned 'address in' during the selection sequence.)			D13032 ADDRESS DEFAULT NOT SUCCESSFUL, RESTART WITH VALID DR ADDR
D13033	The user entered a drive address that is not a valid drive address for this subsystem.			D13033 ADDRESS ENTERED WAS NOT VALID. ADDRESSES MUST BE '00' - 'xx' xx 0-7 for a single control unit subsystem, or 0-F for a dual control unit subsystem
D13034	A timeout occurred while reading status store to determine if this is a dual, or single control unit subsystem.	See the FSI section for error code 5360.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	D13034 TIMEOUT OCCURRED WHILE TRYING TO READ STATUS STORE

[1] This FRU is EC sensitive. See CARR-DR 4.

Control Unit to Drive Serial Test - Routine EE44

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine tests the serial interconnection as follows:

1. The drive is selected to ensure that it can communicate with the control unit.
2. The serial interconnection is used to issue a Clamp command to the drive. CLAMP is displayed on the drive message display.
3. The microcode attempts to re-select the drive using the BI-DI parallel interconnection. If the preceding Clamp command was recognized, the drive will not be available.
4. The serial interconnection is again used to issue an Unclamp command.
5. The drive is again selected using the BI-DI parallel interconnection. This time the drive should be available. UNCLAMP is displayed on the drive message display.
6. At the end of the routine, the drive display is returned to its normal unloaded display, *

Routine Start Address: 4010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Addressing: If a drive address is entered, only that drive will be tested. If no drive address is entered, the routine will run against all drives in the subsystem. The following screen is used to enter a drive address.

```
DIAG=(EE44)-ENTER:
DRIVE
(xx)
```

Valid Parameters:

xx Drive address (0-F, or 00-FF).
Enter FF to run all drives.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
DI4021	Selection of the drive was not successful.	1. Run the control unit to drive bus and tag test routine, EE43. 2. See the FSI section for error code 8E06.	FRU085[1] FRU118 FRU116 FRU134	DI4021 (DR a) INITIAL SELECTION WAS NOT SUCCESSFUL a = drive address
DI4022	Following a Clamp command sent over the serial interface to the drive, the next selection sequence was successful. This indicates that the Serial Clamp command did not operate correctly.	See the FSI section for error code 8803.	FRU085[1] FRU118	DI4022 (DR a) SELECTION WAS SUCCESSFUL AFTER 'CLAMPING' THE DR. a = drive address
DI4023	The selection sequence following the Unclamp command was unsuccessful, indicating that the Unclamp command did not operate correctly. This could be a drive problem rather than a serial interconnection problem if the preceding Clamp command operated correctly.	See the FSI section for error code 8803.	FRU085[1] FRU118	DI4023 (DR a) SELECTION WAS NOT SUCCESSFUL AFTER 'UNCLAMPING' THE DR. a = drive address
DI4024	When defaulting to all drives, the table build module did not find any drives available. (No drive returned 'address in' during selection.)	See the FSI section for error code 8807.		DI4024 ADDRESS DEFAULT NOT SUCCESSFUL, RESTART WITH VALID DR ADDR
DI4025	The user entered a drive address that is not a valid drive address for this subsystem.	Run diagnostic EE40 on all drive addresses to determine the pattern of the failure. Run Drive Command exercises (see DIAG 1).		DI4025 ADDRESS ENTERED WAS NOT VALID. ADDRESSES MUST BE '00' - 'xx' xx = 07 for a single control unit subsystem or 0F for a dual control unit subsystem
DI4026	A timeout occurred while reading status store to determine if this is a dual- or single-control-unit subsystem.	See the FSI section for error code 5360.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	DI4026 TIMEOUT OCCURRED WHILE TRYING TO READ STATUS STORE
DIAG.07	This screen is displayed several times (about every 8 seconds during normal diagnostic execution). If the total execution time is more than the normal run time (see "Diagnostic Identification Code Table" run times) see E103 in the FSI section.	None.	FRU117 FRU115 FRU121 FRU122	DIAG.07 WAITING FOR DIAG COMPLETION

[1] This FRU is EC sensitive. See CARR-DR 4.

Short Loop Write to Pattern Test - Routine EE52

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine tests the short loop write, in the control unit, from the write data flow to the read data flow. Microcode generated patterns test the data path and the response from the read detection circuits.

The routine consists of four tests:

- Test 1 performs initialization to set up the data path and registers for tests 2, 3, and 4.
- Test 2 operates in read forward mode using the short loop write to read controls.
- Test 3 operates in read backward mode using the short loop write to read controls.
- Test 4 operates in write mode using the short loop write to read controls.

Tests 2, 3, and 4 execute as follows:

- The data pattern is stored in the buffer with the buffer control set for Loop Write to Read.
- Write and read data flow controls are set.
- An IBG is written and followed by a microcode generated pattern.
- The read data flow is tested for the correct response.
- Hardware error registers BCSE, WSE, RER, and RSR are tested for error indications.

This sequence of operations is followed for each generated pattern. If an error or unexpected condition is detected, an error message displays on the maintenance device keyboard/display.

Routine Start Address: 2010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is desplayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Pattern Control

Note: *When running the loop write to read diagnostic routine normally,* ***do not*** *enter any test numbers or data patterns.*

Any one of the valid data patterns listed below can be specified for Tests 2, 3, and 4. Valid patterns are:

00 (see Note 1), 02, 04, 06, 08, 0A, 0C, 0E, 10 through 1F, 20 through 26, 28, 2A, 2C, 2E, 30, 32, 34, 36, 38, 3A, 3C, 3E, 40, 42, 44, 46, 48, 4A, 4C, 4E, 50, 52, 54, 56, 58, 5A, 5C, 5E.

Pattern Entry Display

```
DIAG=(EE52)-ENTER:
              PATTERN
               ttii
```

ttii Test data

A pattern can be specified by entering a test number (02, 03, or 04) at position tt and a valid pattern number from the list above at postion ii. For example, an entry of 023A would run test 2 with data pattern 3A.

Notes:

1. *Data pattern 00 has special significance. When a test number and data pattern number 00 are entered, all valid data patterns are run for the test specified. The test also runs if the BYPASS ERROR option is in effect. If errors are detected, the error data is saved and the Failing Patterns screens list all the failing patterns.*

Valid parameters for EE50:

If diagnostic section EE50 is specified, the valid drive address parameters are 0-F, or 00-0F.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the Data Fields (DF) section of this maintenance information.

Test 1 Error Display

```
LW2021
PARM ENTERED= xxxx,
IS NOT VALID.  EX:
0202, 0302, OR 0402
```

nnnnnn Failure ID
xxxx Parameter entered

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

Short Loop Write To Read Pattern Test - Routine EE52 (Continued)

Test 2

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW2021	The routine or pattern number is not valid.	See "Pattern Control" on DIAG 200 to verify that the routines and patterns were entered correctly.		
LW2022	An external register error occurred.	If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 FRU117 FRU115 FRU118 FRU121 FRU119 FRU116 FRU122	nnnnnn ERA=ra, ERB=rb PSR=xx, PER=pp XRA=aa MTI=mm, MDI=md nnnnnn = failure ID ** = no errors were set ra = contents of error register A rb = contents of error register B xx = contents of processor status register pp = contents of processor error register aa = contents of external register address register mm = contents of maintenance tag in register md = contents of the user's active register
LW2023	A check 1 error occurred.	See the FSI section for error code E100.	FRU117 FRU115 FRU114 FRU118 FRU121 FRU119 FRU116 FRU120 FRU122 FRU134 FRU135 FRU192	BCSE=abcde BDSE=fghij RER=rr, RSR=rs WSE EXP=xw, ACT=aw * = no errors were set ** = no errors were set a = buffer channel status and error register bits 0-3 b = BCSE channel error group 0 c = BCSE channel error group 1 d = BCSE channel error group 2 b = BCSE channel error group 3 f = buffer device and error register bits 0-3 g = BDSE channel error group 0 h = BDSE channel error group 1 i = BDSE channel error group 2 j = BDSE channel error group 3 rr = contents of read error register rs = contents of the read status register xw = expected data in the write status/error register aw = actual data in the write status/error register FAILING PATTERNS xx, xx, xx, xx, xx xx, xx, xx, xx, xx xx, xx xx = failing patterns Note: This screen always displays at least one pattern; however, if the number of failing patterns is more than can be displayed on a single screen, they will be listed on following screens.

PATTERN = ttii
RPRT DATA FOLLOWS:
EXP=nx, dx, vx, tx
ACT=na, da va, ta

ttii = test ID (tt) and pattern ID (ii) of the test recording the error
- tt = 01 not valid
  - 02 loop write to read test 2
  - 03 loop write to read test 3
  - 04 loop write to read test 4
  - 05-FF not valid

nx or na
- bit 0 IBG sensed
  - 1 tapemark sensed
  - 2 erase gap sensed
  - 3 reserved
  - 4 beginning of block sensed
  - 5 VOID sensed
  - 6 none of the above sensed
  - 7 reserved

dx or da
- bit 0 density mark sensed
  - 1 reserved
  - 2 reserved
  - 3 reserved
  - 4 beginning of block sensed
  - 5 VOID sensed
  - 6 none of the above sensed
  - 7 reserved

vx or va
- bit 0 VOID zone A
  - 1 VOID zone B
  - 2 VOID zone C
  - 3 VOID zone D
  - 4 VOID zone E
  - 5 VOID zone F
  - 6 reserved
  - 7 reserved

tx or ta
- bit 0 tone zone A
  - 1 tone zone B
  - 2 tone zone C
  - 3 tone zone D
  - 4 tone zone E
  - 5 tone zone F
  - 6 reserved
  - 7 reserved

Test 2 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW2024	A WSE register error occurred.	Do an Exclusive OR using the WSE register's expected and actual data. Test the bits of the results in the following order: 1. Bits 4, 5, and 7 - See the FSI section for error code D7nn and use these bits for nn (bit 6 is ignored and used as zero to build nn). See the FRUs under #1 in the 'FRUS' column. 2. Bit 0 - See the FSI section for error code 7141. See the FRUs under #2 in the 'FRUS' column. 3. Bit 1 - See the FSI section for error code 70E5. See the FRUs under #3 in the 'FRUS' column. 4. Bit 6 - (Normally a 1) forced on by this diagnostic if one frame of data has been processed. If no data has been processed by the write data flow, this bit is set to a zero. See the FSI section for error code D780. See the FRUs under #1 in the 'FRUS' column.	#1 FRU116 FRU118 FRU120 FRU114 FRU139 #2 FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013 #3 FRU085[1] FRU062[1] FRU064 FRU116 FRU118 FRU114 FRU120	See the "Error Displays" column on DIAG 202.
LW2025	Buffer status is incorrect or the buffer detected an error.	1. If BCSE errors are set, see the FSI section for error code D5nn. See the FRUs under #1 in the 'FRUS' column. 2. If BDSE errors are set, see the FSI section for error code D6nn. See the FRUs under #2 in the 'FRUS' column. 3. If WSE register bits 4, 5, and 7 are in error, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column. 4. If BCSE status bit 2 is not 1, the channel microprocessor write is not complete. See the FSI section for error code D5nn. See the FRUs under #1 in the 'FRUS' column. 5. If WSE register bit 0 and 1 are not set, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column. 6. If BDSE bits 0 and 2 are not set to 1, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column. Note: This failure can occur when the DLR external register is not correctly set. Verify CARR-CU 1189 DLR external register switch positon 6 is set per CARR-CU page 1189.	#1 FRU114 FRU120 FRU112[2] FRU113[2] FRU133 FRU136 FRU119 FRU118 FRU116 FRU126 FRU134 FRU152 FRU233 FRU195 FRU235 FRU196 FRU237 FRU121 FRU122 #2 FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU119 FRU118 FRU116 FRU134 FRU117 #3 FRU116 FRU118 FRU120 FRU114 FRU130 FRU131 FRU132 FRU139	
LW2026	A read data flow error occurred during a loop write to read operation.	1. Determine the failing zone. 2. See the FSI section for error code D8nn.	FRU064 FRU062[1] FRU085[1] FRU132 FRU131 FRU130 FRU123 FRU124 FRU125 FRU119 FRU111	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Test 2 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW2027	A read data flow error occurred during a loop write to read operation.	1. Determine the failing zone. 2. See the FSI section for error code D8nn. This failure can occur when the DLR external register is not correctly set. The RPRT expected = 08 08 00 00 actual = 04 04 A8 00 Verify that CARR-CU DLR external register switch position 6 is set per CARR-CU page 1189.	FRU064 FRU062[1] FRU085[1] FRU132 FRU131 FRU130 FRU123 FRU124 FRU125 FRU119 FRU111 FRU116 FRU249 FRU252 FRU253 FRU254	See the "Error Displays" column on DIAG 202.
LW2028	The return code was not valid after an error occurred during a loop write to read operation. This is an EE52 program error.	Call your next level of support.		

Test 3

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW2029	An external register error occurred.	If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 FRU117 FRU115 FRU118 FRU121 FRU119 FRU116 FRU122	See the "Error Displays" column on DIAG 202.
LW202A	A check 1 error occurred.	See the FSI section for error code E100.	FRU117 FRU115 FRU114 FRU118 FRU121 FRU119 FRU116 FRU120 FRU122 FRU134 FRU135 FRU192	

[1] This FRU is EC sensitive. See CARR-DR 4.

Test 3 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW202B	A WSE register error occurred.	Do an Exclusive OR using the WSE register's expected and actual data. Test the bits of the results in the following order: 1. Bits 4, 5, and 7 - See the FSI section for error code D7nn and use these bits for nn (bit 6 is ignored and used as zero to build nn). See FRUs under #1 in the 'FRUS' column. 2. Bit 0 - See the FSI section for error code 7141. See FRUs under #2 in the 'FRUS' column. 3. Bit 1 - See the FSI section for error code 70E5. See FRUs under #3 in the 'FRUS' column. 4. Bit 6 - (Normally a 1) forced on by this diagnostic if one frame of data has been processed. If no data has been processed by the write data flow, this bit is set to a zero. See the FSI section for error code D780. See the FRUs under #1 in the 'FRUS' column.	#1 FRU116 FRU118 FRU120 FRU114 FRU139 #2 FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013 #3 FRU085[1] FRU062[1] FRU064 FRU116 FRU118 FRU114 FRU120	See the "Error Displays" column on DIAG 202.
LW202C	Buffer status is incorrect or the buffer detected an error.	1. If BCSE errors are set, see the FSI section for error code D5nn. See the FRUs under #1 in the 'FRUS' column. 2. If BDSE errors are set, see the FSI section for error code D6nn. See the FRUs under #2 in the 'FRUS' column. 3. If WSE register bits 4, 5, and 7 are in error, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column. 4. If BCSE status bit 2 is not 1, the channel microprocessor write is not complete. See the FSI section for error code D5nn. See the FRUs under #1 in the 'FRUS' column. 5. If WSE register bit 0 and 1 are not set, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column. 6. If BDSE bits 0 and 2 are not set to 1, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column.	#1 FRU114 FRU120 FRU112[2] FRU113[2] FRU133 FRU136 FRU119 FRU118 FRU116 FRU126 FRU134 FRU152 FRU233 FRU195 FRU235 FRU196 FRU237 FRU121 FRU122 #2 FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU119 FRU118 FRU116 FRU134 FRU117 #3 FRU116 FRU118 FRU120 FRU114 FRU139	
LW202D	A read data flow error occurred during a loop write to read operation.	1. Determine the failing zone. 2. See the FSI section for error code D8nn.	FRU064 FRU062[1] FRU085[1] FRU132 FRU131 FRU130 FRU123 FRU124 FRU125 FRU119 FRU111 FRU116	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Test 3 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW202E	A read data flow error occurred during a loop write to read operation.	1. Determine the failing zone. 2. See the FSI section for error code D8nn.	FRU064 FRU062[1] FRU085[1] FRU132 FRU131 FRU130 FRU123 FRU124 FRU125 FRU119 FRU111 FRU116	See the "Error Displays" column on DIAG 202.
LW202F	The return code was not valid after an error occurred during a loop write to read operation. This is an EE52 program error.	Call your next level of support.		

Test 4

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW2030	An external register error occurred.	If PSR bit 0 = 1, see EAD 1 for error code Fnnn.	FRU114 FRU120 FRU117 FRU115 FRU118 FRU121 FRU119 FRU116 FRU122	See the "Error Displays" column on DIAG 202.
LW2031	A check 1 error occurred.	See the FSI section for error code E100.	FRU117 FRU115 FRU114 FRU118 FRU121 FRU119 FRU116 FRU120 FRU122 FRU134 FRU135 FRU192	

[1] This FRU is EC sensitive. See CARR-DR 4.

Test 4 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW2032	A WSE register error occurred.	Do an Exclusive OR using the WSE register's expected and actual data. Test the bits of the results in the following order: 1. Bits 4, 5, and 7 - See the FSI section for error code D7nn and use these bits for nn (bit 6 is ignored and used as zero to build nn). See FRUs under #1 in the 'FRUS' column. 2. Bit 0 - See the FSI section for error code 7141. See FRUs under #2 in the 'FRUS' column. 3. Bit 1 - See the FSI section for error code 70E5. See FRUs under #3 in the 'FRUS' column. 4. Bit 6 - (Normally a 1) forced on by this diagnostic if one frame of data has been processed. If no data has been processed by the write data flow, this bit is set to a zero. See the FSI section for error code D780. See the FRUs under #1 in the 'FRUS' column.	#1 FRU116 FRU118 FRU120 FRU114 FRU139 #2 FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013 #3 FRU085[1] FRU062[1] FRU064 FRU116 FRU118 FRU114 FRU120	See the "Error Displays" column on DIAG 202.
LW2033	Buffer status is incorrect or the buffer detected an error.	1. If BCSE errors are set, see the FSI section for error code D5nn. See the FRUs under #1 in the 'FRUS' column. 2. If BDSE errors are set, see the FSI section for error code D6nn. See the FRUs under #2 in the 'FRUS' column. 3. If WSE register bits 4, 5, and 7 are in error, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column. 4. If BCSE status bit 2 is not 1, the channel microprocessor write is not complete. See the FSI section for error code D5nn. See the FRUs under #1 in the 'FRUS' column. 5. If WSE register bit 0 and 1 are not set, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column. 6. If BDSE bits 0 and 2 are not set to 1, see the FSI section for error code D7nn. See the FRUs under #3 in the 'FRUS' column.	#1 FRU114 FRU120 FRU112[2] FRU113[2] FRU133 FRU136 FRU119 FRU118 FRU116 FRU126 FRU134 FRU152 FRU233 FRU195 FRU235 FRU196 FRU237 FRU121 FRU122 #2 FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU119 FRU118 FRU116 FRU134 FRU117 #3 FRU116 FRU118 FRU120 FRU114 FRU139	
LW2034	A read data flow error occurred during a loop write to read operation.	1. Determine the failing zone. 2. See the FSI section for error code D8nn.	FRU064 FRU062[1] FRU085[1] FRU132 FRU131 FRU130 FRU123 FRU124 FRU125 FRU119 FRU111 FRU116	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Test 4 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW2035	A read data flow error occurred during a loop write to read operation.	1. Determine the failing zone. 2. See the FSI section for error code D8nn.	FRU064 FRU062[1] FRU085[1] FRU132 FRU131 FRU130 FRU123 FRU124 FRU125 FRU119 FRU111 FRU116	See the "Error Displays" column on DIAG 202.
LW2036	The return code was not valid after an error occurred during a loop write to read operation. This is an EE52 program error.	Call your next level of support.		

[1] This FRU is EC sensitive. See CARR-DR 4.

Short Loop Write to Read Timing Test - Routine EE53

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine checks the read and write data flow in the control unit. A record consisting of 28 bytes is placed in the data buffer by the microprocessor and then sent to the write data flow card.

The write data flow card sends an IBG, preamble, 28 bytes of data, and a postamble to the read detection card using 18 special loop write to read signal lines.

This routine checks that the following events occur at the proper time:

- Beginning of Block
- Beginning Sync
- Ending Sync
- Generate Gap Out
- The next IBG.

A failure during this diagnostic indicates the problem is in the control unit being exercised and not in the tape units attached to this control unit.

Refer to the OPER section of the MI for more details on the loop write to read data flow.

Routine Start Address: 3010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the Data Fields (DF) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS
LW3021	An error was detected in the PER, PSR, or MTI register.	See the FSI section for error codes D1nn and D900.	FRU120
LW3022	An error was detected in the ERA or ERB register.	See the FSI section for error code E100	FRU114
LW3023	An error was detected in the WSE register.	See the FSI section for error code 7076.	FRU113[1]
LW3024	An error was detected in the BCSE or BDSE register.	See the FSI section for error codes D5nn and D6nn.	FRU112[1]
LW3025	An error was detected in the RER or RSR register.	See the FSI section for error codes D0nn and D8nn.	FRU116
LW3026	An error was detected in the WSE register prior to starting the write data flow.	See the FSI section for error code 7076.	FRU111
LW3027	An error was detected in the RSR register prior to starting the write data flow.	See the FSI section for error code D0nn.	FRU119
LW3028	An error was detected in the RER register prior to starting the write data flow.	See the FSI section for error code D8nn.	FRU123
LW3029	Beginning of block was not detected.	See the FSI section for error code 7142.	FRU124
LW302A	Beginning of block was detected too soon.	See the FSI section for error code 7142.	FRU125
LW302B	Beginning sync was not detected.	See the FSI section for error code 7071.	FRU130
LW302C	Beginning sync was detected too soon.	See the FSI section for error code 7071.	FRU131
LW302D	Ending sync was not detected.	See the FSI section for error code 74nn.	FRU132
LW302E	Ending sync was detected too soon.	See the FSI section for error code 74nn.	
LW302F	Generate gap out was not detected.	See the FSI section for error code 7163.	
LW3030	Generate gap out was detected too soon.	See the FSI section for error code 7163.	
LW3031	The next IBG was not detected.	See the FSI section for error code 7503.	
LW3032	The diagnostic produced an invalid error code.	This is a diagnostic program error.	

ERROR DISPLAYS

```
nnnnnn
ERA=aa    ERB=bb
MTI=cc    MDI=dd
PSR=ee    PER=ff
```

```
XRA=gg    WSE=hh
RER=ii    RSR=jj
 BCSE= a b c d e
 BDSE= f g h i j
```

```
RCR=kk    WCR=ll
RPR=mm
```

```
nnnnnn = failure ID
 * = No error is set
aa = Contents of the ERA register
bb = Contents of the ERB register
cc = Contents of the MTI register
dd = Contents of the MDI register
ee = Contents of the PSR register
ff = Contents of the PER register
gg = Contents of the XRA register
hh = Contents of the WSE register
ii = Contents of the RER register
jj = Contents of the RSR register
kk = Contents of the RCR register
ll = Contents of the WCR register
mm = Contents of the RPR register
 a = Bits 0-3 of the BCSE status
     register
 b = BCSE register error group 0
 c = BCSE register error group 1
 d = BCSE register error group 2
 e = BCSE register error group 3
 f = Bits 0-3 of the BDSE status
     register
 g = BDSE register error group 0
 h = BDSE register error group 1
 i = BDSE register error group 2
 j = BDSE register error group 3
```

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Short Loop Write to Read Timing Test - Routine EE53 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW3033	An error was detected in the WSE register prior to starting the write data flow.	See the FSI section for error code 7076.	FRU120 FRU114 FRU113[1] FRU112[1] FRU116 FRU111 FRU119 FRU123 FRU124 FRU125 FRU130 FRU131 FRU132	nnnnnn ERA=aa ERB=bb MTI=cc MDI=dd PSR=ee PER=ff XRA=gg WSE=hh RER=ii RSR=jj BCSE= a b c d e BDSE= f g h i j RCR=kk WCR=ll RPR=mm nnnnnn = failure ID * = No error is set aa = Contents of the ERA register bb = Contents of the ERB register cc = Contents of the MTI register dd = Contents of the MDI register ee = Contents of the PSR register ff = Contents of the PER register gg = Contents of the XRA register hh = Contents of the WSE register ii = Contents of the RER register jj = Contents of the RSR register kk = Contents of the RCR register ll = Contents of the WCR register mm = Contents of the RPR register a = Bits 0-3 of the BCSE status register b = BCSE register error group 0 c = BCSE register error group 1 d = BCSE register error group 2 e = BCSE register error group 3 f = Bits 0-3 of the BDSE status register g = BDSE register error group 0 h = BDSE register error group 1 i = BDSE register error group 2 j = BDSE register error group 3
LW3034	An error was detected in the RSR register prior to starting the write data flow.	See the FSI section for error code D0nn.		
LW3035	An error was detected in the RER register prior to starting the write data flow.	See the FSI section for error code D8nn.		
LW3036	Beginning of block was not detected.	See the FSI section for error code 7142.		
LW3037	Beginning of block was detected too soon.	See the FSI section for error code 7142.		
LW3038	Read condition was set too soon.			
LW3039	Read condition was set too late.			
LW303A	Beginning sync was not detected.	See the FSI section for error code 7071.		
LW303B	Beginning sync was detected too soon.	See the FSI section for error code 7071.		
LW303C	Ending sync was not detected.	See the FSI section for error code 74nn.		
LW303D	Ending sync was detected too soon.	See the FSI section for error code 74nn.		
LW303E	Generate gap out was not detected.	See the FSI section for error code 7163.		
LW303F	Generate gap out was detected too soon.	See the FSI section for error code 7163.		
LW3040	The next IBG was not detected.	See the FSI section for error code 7503.		
LW3041	Beginning of block was not set during the read condition test.	This failure can occur when the DLR external register is not correctly set. Verify CARR-CU DLR external register switch position 6 is off.		
LW3042	Read condition is set when a block is shorter than 15 microseconds.			
LW3043	Read condition is not set when a block is longer than 15 microseconds.			
LW3044	Read condition is set when a block is shorter than 15 microseconds.	This failure can occur when the DLR external register is not correctly set. Verify CARR-CU DLR external register switch position 6 is set.		
LW3045	Read condition is set, but not enabled.			

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Long Loop Write to Read Test - Routine EE54

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine checks the read and write data flow from the control unit to a tape unit and back to the control unit.

The write data flow card sends an IBG to the drive, the write bus, and the drive-adapter card. The drive-adapter card loops the data from write bus lines 0 and 1 to the read pre-amplifier card. The read pre-amplifier card sends the data over the read bus to the read detection card. The read detection card checks for the proper zones that indicate an IBG is present. An error is indicated if an IBG is not detected.

This routine also tests the control unit to tape unit interconnections because a drive must be selected and conditioned for the long loop write to read test by sending it the diagnose command. Errors are indicated if the drive responds incorrectly to the control unit.

A failure during this diagnostic indicates the problem may be in the control unit being tested or in the tape units attached to this control unit. This test may be run using the same control unit and a different drive to further isolate the problem. If you have a dual control unit configuration, this test may be run using the second control unit to exercise the failing drive.

Refer to the OPER section of the MI for more details on the loop write to read data flow.

Routine Start Address: 4010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Test Selection

The following screen displays after routine number EE54 has been entered to start the routine.

```
DIAG=(EE54)-ENTER:
DRIVE
(xx)
```

Valid parameters:

xx Drive address (0-F, or 00-0F).

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS
LW4021	An error was detected in the PER, PSR, or MTI register.	See the FSI section for error codes D0nn, and D1nn. See EAD 1 for error code Fnnn.
LW4022	An error was detected in the ERA or ERB register.	See the FSI section for error code E100.
LW4023	An error was detected in the WSE register.	See the FSI section for error code D7nn.
LW4024	An error was detected in the BCSE or BDSE register.	See the FSI section for error codes D5nn and D6nn.
LW4025	An error was detected in the RER or RSR register.	See the FSI section for error codes D0nn and D8nn.
LW4026	An error was detected in the WSE register prior to write data flow starting.	See the FSI section for error code D7nn.
LW4027	An error was detected in the RSR register prior to write data flow starting.	See the FSI section for error code D0nn.
LW4028	An error was detected in the RER register prior to write data flow starting.	See the FSI section for error code D8nn.
LW4029	An invalid address has been specified.	Valid drive addresses are 00 to 0F.
LW402A	The IBG was not detected.	See the FSI section for error codes 7093 and 7143.
LW402B	A timeout occurred while waiting for the drive to raise device data bus 'clock B in', indicating that the drive is ready to accept the diagnose command data.	See the FSI section for error codes 840A and 8300. See EAD 1, "Drive Interconnections."
LW402C	A timeout occurred while waiting for the drive to drop device data bus 'clock B in' indicating that the drive has accepted the diagnose command.	See the FSI section for error codes 8600 and 8601. See EAD 1, "Drive Interconnections."
LW402D	A timeout occurred while waiting for the drive to clear the device data bus of all interrupts.	See the FSI section for error code 8005. See EAD 1, "Drive Interconnections."
LW402E	A timeout occurred while waiting for the drive to raise device data bus 'address in', indicating that the drive has recognized its address on the bus.	See the FSI section for error code 8007. See EAD 1, "Drive Interconnections."
LW402F	The drive address returned in the device data bus DCB does not match the one's complement address.	See the FSI section for error code 800C. See EAD 1, "Drive Interconnections."

FRUs

FRU120
FRU114
FRU113[2]
FRU112[2]
FRU116
FRU118
FRU111
FRU119
FRU123
FRU124
FRU125
FRU130
FRU131
FRU132
FRU085[1]
FRU064

ERROR DISPLAYS

```
nnnnnn
ERA=aa     ERB=bb
MTI=cc     MDI=dd
PSR=ee     PER=ff
```

```
XRA=gg     WSE=hh
RER=ii     RSR=jj
 BCSE= a b c d e
 BDSE= f g h i j
```

```
RCR=kk     WCR=ll
RPR=mm
```

nnnnnn = failure
 * = No error is set
aa = Contents of the ERA register
bb = Contents of the ERB register
cc = Contents of the MTI register
dd = Contents of the MDI register
ee = Contents of the PSR register
ff = Contents of the PER register
gg = Contents of the XRA register
hh = Contents of the WSE register
ii = Contents of the RER register
jj = Contents of the RSR register
kk = Contents of the RCR register
ll = Contents of the WCR register
mm = Contents of the RPR register
 a = Bits 0-3 of the BCSE status register
 b = BCSE register error group 0
 c = BCSE register error group 1
 d = BCSE register error group 2
 e = BCSE register error group 3
 f = Bits 0-3 of the BDSE status register
 g = BDSE register error group 0
 h = BDSE register error group 1
 i = BDSE register error group 2
 j = BDSE register error group 3

The following two frames are displayed only when a drive unit check is detected.

```
DRV=dv     DSE=de
DCR=dr     DTR=dt
DCB=db     DIR=di
STS=gggg hhhh
```

 * No error is set
db Contents of the DCB register
de Contents of the DSE register
di Contents of the DIR register
dr Contents of the DCR register
dt Contents of the DTR register
dv Is the drive address
gggg Drive status byte
hhhh Drive status bytes for a sense command

```
DRSNS-  S8=b0,S19=b1
S18= b2, S2021= b4b5
         S2223= b6b7
S30= 21,    EC= 2223
```

NOTE: When no sense data is received from the drive, these bytes all contain FF.

The following sense data is described in the SENSE section (see formats 19 and 20).

b0 Contents of the drive error recovery byte (see sense byte 8).
b1 The contents of the drive features byte (see sense byte 19).
b2 Flags modifier to b4b5 (see sense byte 18).
b4b5 The first error the drive detected. B4 contains the drive command associated with this error, an EE to indicate a bus out parity error while loading a command or an FF to indicate that the error occurred when the drive was not performing a command. B5 contains the drive error code identifying this error (see sense bytes 20 and 21).
b6b7 The last error the drive detected. B6 contains the drive command associated with this error, an EE to indicate a bus out parity error while loading a command, or an FF to indicate that the error occurred when the drive was not performing a command. B7 contains the drive error code identifying this error (see sense bytes 22 and 23).
21 Logical drive address and physical drive address (contents of the thumbwheel switches). See sense byte 30.
2223 The drive EC level (contains the last four digits of the drive ROS module EC level).

The following frame is displayed only when a data compare error is detected. Each symbol (1A, 2A) indicates a data compare error has occurred on that track.

```
ERR TRK:1A, 2A, 3A,
4A, 5A, 6A, 7A, 8A,
9A, 1B, 2B, 3B, 4B,
5B, 6B, 7B, 8B, 9B.
```

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW4030	An error has been detected in the DSE register during selection.	See the FSI section for error codes 800A and 8Dnn. See EAD 1, "Drive Interconnections."	FRU120 FRU114	See the "Error Displays" column on DIAG 222.
LW4031	A timeout occurred waiting for the drive to drop device data bus 'address in', indicating that the drive recognized that device data bus 'address out' dropped.	See the FSI section for error code 8009. See EAD 1, "Drive Interconnections."	FRU113[2] FRU112[2]	
LW4032	The drive has raised device data bus 'address in' during a command, indicating that it has detected a hardware error.	See the FSI section for error codes 86F0, 86F1, and 89nn. See EAD 1, "Drive Interconnections."	FRU116 FRU118	
LW4033	An error has been detected in the DSE register during a command.	See the FSI section for error code 800A. See EAD 1, "Drive Interconnections."	FRU111	
LW4034	A timeout occurred while waiting for the drive to drop device data bus 'status in', in response to the control unit dropping 'select out'.	See the FSI section for error code 8C07. See EAD 1, "Drive Interconnections."	FRU119 FRU123	
LW4035	The drive has raised device data bus 'address in' during device data bus 'status in', indicating that it has detected a hardware error.	See the FSI section for error codes 86F0, 86F1, and 89nn. See EAD 1, "Drive Interconnections."	FRU124 FRU125	
LW4036	A timeout occurred while waiting for the drive to raise device data bus 'status in', indicating that the first status byte is available on the DCB.	See the FSI section for error code 8E05. See EAD 1, "Drive Interconnections."	FRU130 FRU131	
LW4037	A timeout occurred while waiting for the drive to raise device data bus 'clock B in', indicating that the second status byte is available on the DCB.	See the FSI section for error code 840A. See EAD 1, "Drive Interconnections."	FRU132 FRU085[1]	
LW4038	A timeout occurred while waiting for the drive to drop device data bus 'clock B in' in response to the control unit dropping 'clock A out'.	See the FSI section for error code 840C. See EAD 1, "Drive Interconnections."	FRU064	
LW4039	Status indicates a different address (HI or LO) than the one the control unit used. See DF1, "Drive Status Bits 0-15," and read the definition of bit 8.	See the FSI section for error code 86C0.		
LW403A	The drive external register cartridge present sensor is set using a read drive external register order.	1. Remove the cartridge and rerun this diagnostic. 2. Press the reset switch on the drive. 3. See the FSI section for CHK 02.		
LW403B	Status indicates a drive unit check.	Check the sense bytes for the cause of the check.		
LW403C	A timeout occurred while waiting for the drive to raise device data bus 'clock B in', indicating that a sense byte is available on the DCB.	See the FSI section for error codes 840A, 8600, and 8601. See EAD 1, "Drive Interconnections."		
LW403D	A timeout occurred while waiting for the drive to drop device data bus 'clock B in', in response to the control unit raising device data bus 'clock A out' during a sense operation.	See the FSI section for error codes 8600 and 8601. See EAD 1, "Drive Interconnections."		
LW403E	A timeout occurred while waiting for the drive to raise device data bus 'clock B in' indicating that a sense byte is available on the DCB.	See the FSI section for error code 8600. See EAD 1, "Drive Interconnections."		

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
LW403F	A timeout occurred while waiting for the drive to drop device data bus 'clock B in', in response to the control unit raising device data bus 'clock A out' during a sense operation.	See the FSI section for error code 8600. See EAD 1, "Drive Interconnections."	FRU120 FRU114	See the "Error Displays" column on DIAG 222.
LW4040	The diagnostic program has produced an invalid error code.	This is a diagnostic program error.	FRU113[2]	
LW4041	A timeout occurred while waiting for the drive to raise device data bus 'clock B in', indicating that a data byte is available on the DCB.	See the FSI section for error codes 840A, 8600, and 8601. See EAD 1, "Drive Interconnections."	FRU112[2] FRU116	
LW4042	A timeout occurred while waiting for the drive to drop device data bus 'clock B in', in response to the control unit raising device data bus 'clock A out' during a read drive external register command.	See the FSI section for error codes 8600 and 8601. See EAD 1, "Drive Interconnections."	FRU118 FRU111	
LW4043	A timeout occurred while waiting for the drive to raise device data bus 'clock B in', indicating that a data byte is available on the DCB.	See the FSI section for error code 8600. See EAD 1, "Drive Interconnections."	FRU119 FRU123	
LW4044	A timeout occurred while waiting for the drive to drop device data bus 'clock B in', in response to the control unit raising 'clock A out' during a read drive external register command.	See the FSI section for error code 8601. See EAD 1, "Drive Interconnections."	FRU124 FRU125	
LW4045	A drive unit check occurred during a sense command.	See the FSI section for error code 86A0.	FRU130 FRU131	
LW4046	The sense data from the drive contained an ERP code that is not permitted. Permitted errors are ERP = 66, ERP = 6C with error code 75, or ERP = 78 with error code 76.	Go to the FSI section with the error code listed for b5 or b7 of the DRSNS error display (see the Error Display Column).	FRU132 FRU085[1]	
LW4047	A Read External Register command was sent twice and a drive unit check was received both times.	Go to the FSI section with the error code listed for b5 or b7 of the DRSNS error display (see the Error Display Column).	FRU064	
LW4048	A Drive Set Diagnose command was sent twice and a drive unit check was received both times.	Go to the FSI section with the error code listed for b5 or b7 of the DRSNS error display (see the Error Display Column).		
LW4049	A Write command was sent and drive unit check was received.	Go to the FSI section with the error code listed for b5 or b7 of the DRSNS error display (see the Error Display Column).		
LW404A	A Drive Set Diagnose command was sent twice and a drive unit check was received both times.	Go to the FSI section with the error code listed for b5 or b7 of the DRSNS error display (see the Error Display Column).		
LW404B	The control unit hardware did not complete the execution of a device data bus 'Serial Reset A' command.	See the FSI section for error code 8803. See EAD 1, "Drive Interconnections."		

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRU LISTINGS		ERROR DISPLAYS
			LIST	FRU NUMBERS	See the error page DIAG 222.
LW404C	The first IBG is too long.	See the FSI section for error code 7152. See FRU list A			
LW404D	The first IBG is too short.	See the FSI section for error code 7151. See FRU list A	A	FRU120, FRU114, FRU113 (See Note 2), FRU112 (See Note 2), FRU116, FRU118, FRU111, FRU119, FRU123, FRU124, FRU125, FRU130, FRU131, FRU132 FRU085 (See Note 1), FRU064	
LW404E	The preamble is too long.	See the FSI section for error code 7071. See FRU list A			
LW404F	The preamble is too short.	See the FSI section for error code 7071. See FRU list A			
LW4050	Ending synch did not occur during the time allowed.	See the FSI section for error code 7155. See FRU list A	B	FRU132, FRU125	
LW4051	Ending synch occurred too soon.	See the FSI section for error code 7155. See FRU list A	C	FRU131, FRU124	
LW4052	Gapout did not occur during the time allowed.	See the FSI section for error code 7502. See FRU list A	D	FRU130, FRU123	
LW4053	Gapout occurred too soon.	See the FSI section for error code 7502. See FRU list A	E	FRU124, FRU131, FRU125, FRU132	
LW4054	The second IBG did not occur during the time allowed.	See the FSI section for error code 7152. See FRU list A	F	FRU123, FRU130, FRU125, FRU132	
LW4055	An error occurred in BDSE during long loop write to read.	See the FSI section for error code 7077. See FRU list A	G	FRU123, FRU130, FRU124, FRU131	
LW4056	An error occurred in the DSE register during long loop write to read.	See the FSI section for error code D4nn. See FRU list A	H	FRU123, FRU124, FRU125, FRU130 FRU130, FRU131, FRU132	
LW4057	BDSE status is incorrect at the end of long loop write to read.	See the FSI section for error code 7078. See FRU list A	I	FRU085 (See Note 1), FRU062, FRU064, FRU013, FRU088 or FRU092, FRU089 or FRU092, FRU087 or FRU094	
LW4058	BCSE status is incorrect at the end of long loop write to read.	See the FSI section for error code D5nn. See FRU list A			
LW4059	A data error occurred in group 3.	See the FSI section for error code E304. See FRU lists B and I See Note	Note: This problem can be caused by a problem on any drive attached to this interface (Local 'A') or (Remote 'B'). Pull drive TEE cables to isolate to a single failing drive. See LOC 1 and 2 for 'Read Adapter Cables'		
LW405A	A data error occurred in group 2.	See the FSI section for error code E302. See FRU lists C and I See Note			
LW405B	A data error occurred in group 1.	See the FSI section for error code E301. See FRU lists D and I See Note			
LW405C	Data errors occurred in groups 2 and 3.	See the FSI section for error code E306. See FRU lists E and I See Note			
LW405D	Data errors occurred in groups 1 and 3.	See the FSI section for error code E305. See FRU lists F and I See Note			
LW405E	Data errors occurred in groups 1 and 2.	See the FSI section for error code E303. See FRU lists G and I See Note			
LW405F	Data errors occurred in groups 1, 2, and 3.	See the FSI section for error code E307. See FRU lists H and I See Note			
LW4060	Incorrect byte count of (loop write to read) read data.	See the FSI section for error code 74nn. See FRU list A			
LW4061	WSE status did not contain complete.	See the FSI section for error code D7nn. See FRU list A			
LW4062	A level 2 interrupt did not occurr on the density separator.	See the FSI section for error code 7142. See FRU list A			
LW4063	The second IBG was not detected.	See the FSI section for error code 7052. See FRU list A			
LW4064	At the completion of the loop-write-to-read the RSR must contain 'ED' (hexadecimal) and the RER must contain '00' (hexadecimal).	See the FSI section for error code 7081. See FRU list A			
LW4065	The DLR external register and drive sense do not agree.	See CARR-CU 1189 for correct DLR external register switch setting.	FRU118		

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

Long Loop Write to Read Test-Routine EE54 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUs	ERROR DISPLAYS
LW4066 LW4067	A timeout error occurred during a TIO command to the drive. A drive status error occurred while sending code to the drive.	1. This program has minimum diagnostic capability during the drive patching procedure. 2. This error occurs when a cartridge loader is installed and a cartridge is present in the drive to be tested. 3. This error can be bypassed by loading the functional code into the control unit and setting the control unit on-line. Press unload switch of the drive being tested, reload diagnostic EE54 and run it. To avoid channel interference set all the channel enable/disable switches to disable. 4. If this error persists, run "Start Repair" on the product diskette.		See the "Error Displays" on DIAG 222.
LW4068 LW4069 LW406A	The correct level of code patches is not found on the IML diskette. The correct level of code patches is not found on the IML diskette. Unable to read the IML diskette due to an error.	1. Make sure the diskette in the diskette reader is the correct level. 2. This error occurs when a cartridge loader is installed and a cartridge is present in the drive to be tested. 3. This error can be bypassed by loading the functional code into the control unit and setting the control unit on-line. Press unload switch of the drive being tested, reload diagnostic EE54 and run it. To avoid channel interference set all the channel enable/disable switches to disable. Ensure that the control unit successfully loads code from the diskette. 4. If this error persists, run "Start Repair" on the product diskette.		

Channel Interface Wrap Test - Routine EE62

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

CAUTION:
Follow the "Setup Procedure for the Channel Wrap Test."

This routine tests the channel adapter bus and tag interface lines.

Wrap blocks are used to wrap the channel adapter bus and tag lines, and the diagnostic program generates bit patterns and sends them through the wrap path. The wrap path is:

- From the channel adapter to the bus and tag shoe card drivers
- Through the wrap blocks to the bus and tag shoe card receivers
- Back to the channel adapter.

The pattern received at the end of the wrap is compared with an expected pattern. A non-match produces an error and a maintenance device error display that provides data to define the error.

The routine executes in six steps:

1. With 'op in' active, each tag bit is set in the 'tag in' register and tested at the 'tag out' register.
2. With 'op in' and 'status in' active, each tag bit is set in the 'tag in' register and tested at the 'tag out' register.
3. With 'op in' active, the routine ripples the 'bus in' and ensures that the 'bus out' lines respond correctly.
4. With 'op in' and 'select in' active, each tag bit is set in the 'tag in' register and tested at the 'tag out' register.
5. With 'op in' and 'status in' active, each bus bit is set in the 'bus in' register and tested at the 'bus out' register.
6. With 'op in' and 'status in' inactive, each bus bit is set in the 'bus in' register and tested at the 'bus out' register. The bits should not be active.
7. Set 'mark in' and ensure the 'bus out' bit 0 is set.

Routine Start Address: 2010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Setup Procedure for the Channel Wrap Test

See INST 1, "Setup Procedure for the Channel Wrap Test."

Warning: Stop all activity on the host processor channels before you disconnect channel cables, or interface control checks will occur.

---

1. Press stop on the host processor.
2. Disable the channels that are to be tested. (The disable switches are on the control unit operator panel.)
3. Remove all interface cables and terminators from the channel tailgate assembly for the channel to be tested. (See the LOC section for cable locations.)
4. If this is the last control unit on the channel, install the tag terminator on the tag-in cable and the bus terminator on the bus-in cable.
5. If this is not the last control unit on the channel, then connect the bus-in and bus-out cables together and connect the tag-in and tag-out cables together.
6. The user can now continue channel activity from the host processor.
7. See PLAN 1 for "Channel Wrap Blocks."
   a. Install the **wrap terminator (part 6315622)** **1** **5** in the bus-out cable connector position of the I/O connector assembly. This part is in the ship group.
   b. Install the bus **wrap block (part 4299876)** **2** **6** in the bus-in cable connector position of the I/O connector assembly. This part is in the ship group.
   c. Install the **370 channel tag terminator (part 2282676)** **3** **7** in the tag-out cable connector position of the I/O connector assembly.
   d. Install the **tag wrap block (part 4299873)** **4** **8** in the tag-in cable connector position of the I/O connector assembly. This part is in the ship group.
8. Select and run the channel interface wrap test.
9. The following screen is displayed:

```
CHN ADDR
(A)
```

Valid Parameters:

(A) Channel Address (valid parameters are A, B, C, or D)

If channel A is to be tested, press the enter key. If a different channel is to be tested, enter that channel address and press the enter key. The MD will respond with, 'IS THIS CORRECT'. Entry errors may be corrected before proceeding.

The tags issued and expected are:

Tag Sequence	EXP Tag Out
80 Op in	80 Op out
C0 Addr in	81 Sup out
A0 Sel in	A0 Sel out
90 Req in	C0 Addr out
88 Stat in	88 Cmd out
84 Serv in	84 Serv out
82 Data in	82 Data out
81 Disc in	90 Hold out

The tags issued and expected are:

Bus Sequence	EXP Bus Out
80	80
40	40
20	20
10	10
08	08
04	04
02	02
01	01

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

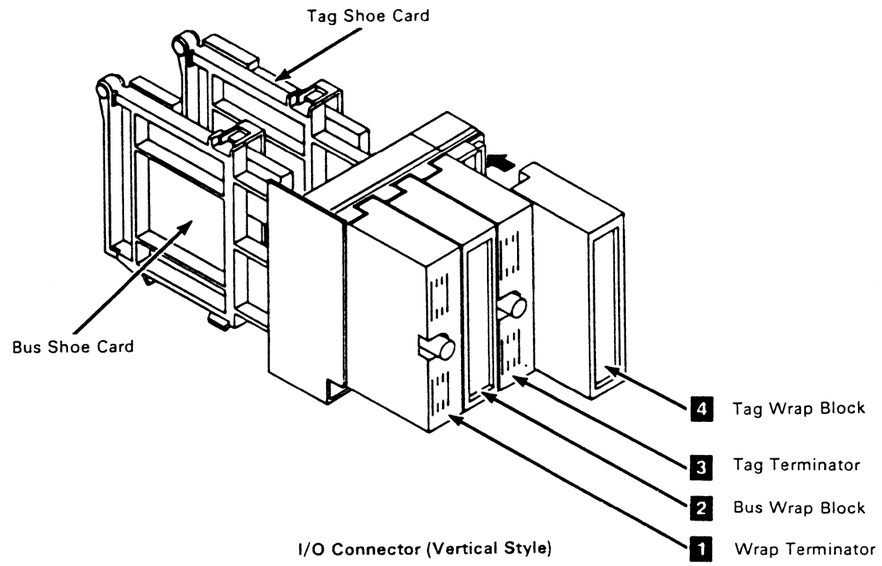
The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

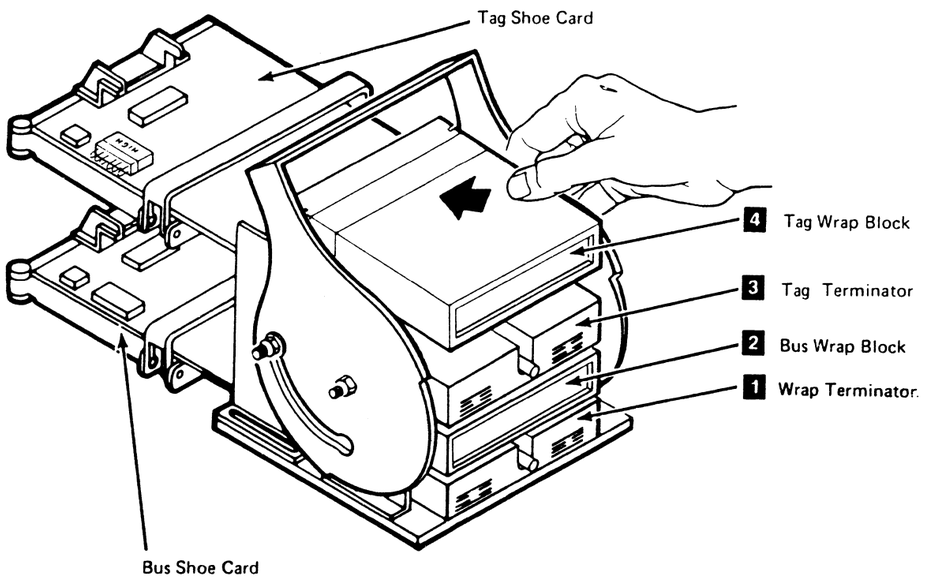
See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

Note: When errors persist after replacing all FRUs, suspect a defective wrap terminator.

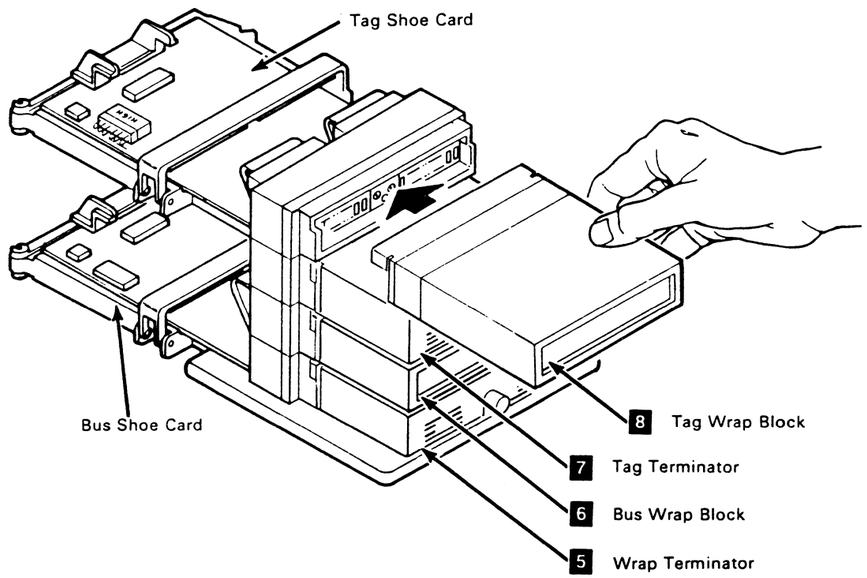


I/O Connector (Vertical Style)

I/O Connector (Movable Rail Style)



I/O Connector (Horizontal Style)



FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C12020	A channel timeout error is detected in the MSB register (bit 0).	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (see DIAG 1). See the FSI section for error code 2060.	FRU154 FRU133 FRU152 FRU195 FRU196 FRU115 FRU121	C12020 ***ERROR CHNL TIMEOUT CARD SEE 'EE62' (REF: DIAG 1) DO YOU WANT TO CONTINUE? NO = Return to menu YES = Start diagnostic EE62
C12021	The service representative (SR) entered an invalid channel adapter address. The address received by the microcode is shown in the ADDR= field. This could be an SR error or an MD communication error.	See the FSI section for error code E04B.	FRU115	C12021 INVALID CA ADDRESS VALID= A B C D ADDR=zz zz Address entered by the service representative
C12022	A channel adapter was selected that is not installed, or the status store to channel adapter communication was incorrect.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (see DIAG 1). See the FSI section for error code 2060.	FRU133 FRU152 FRU195 FRU196 FRU121	C12022 CHNL ADAP=x NOT PLUGGED OR NOT RESPONDING x Channel adapter A,B,C, or D
C12023	The microcode issued a channel adapter order and did not receive an acknowledgement from status store (CRR bit 6). This error applies for all orders after the first hexadecimal F0 order given to the channel adapter. CCC register: Bits 4-7 are offsets to RAM Bit 0 - CA addr A and depend on the setting 1 - CA addr B of the CAE register. 2 - CA addr C Cx - Read CA RAM page x 3 - CA addr D Dx - Write CA RAM page x F4 - Set on line	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (see DIAG 1). See the FSI section for error code 2060.	FRU133 FRU152 FRU195 FRU196 FRU121	C12023 CHNL ADAP DID NOT ACKNWLDGE LAST ORDER CCC=aa CCA=bb aa Contents of the channel card control register bb Contents of the channel card address register
C12024	The microcode issued a channel adapter order and did not receive the complete indication from status store (CRR bit 7). Channel adapter addresses from the channel control card register: 80 = channel adapter A 40 = channel adapter B 20 = channel adapter C 10 = channel adapter D	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 once for each channel. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU121	C12024 CHNL ADAP DID NOT COMPLETE LAST ORDER CCC=aa CCA=bb aa Contents of the channel card control register bb Contents of the channel card address register

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C12025	The microcode issued a channel adapter order and a check 2 occurred.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (see DIAG 1). See the FSI section for error code 55nn.	FRU133 FRU152 FRU195 FRU196 FRU121 FRU137 FRU234 FRU236 FRU238	C12025 A CHECK-2 OCCURRED ON LAST ORDER CAE=cc CER=dd cc Contents of the channel adapter error register dd Contents of the channel error register
C12026	The microcode issued a 'tag in' through the channel adapter diagnostic registers and did not receive the expected bit on 'tag out'. 'Op in' was used as a control tag to gate the bit to the tag line driver to be wrapped back through the tag line receiver. Tags issued and expected: Tag Sequence EXP Tag Out 80 Op in 80 Op out C0 Addr in 81 Sup out A0 Sel in A0 Sel out 90 Req in C0 Addr out 88 Stat in 88 Cmd out 84 Serv in 84 Serv out 82 Data in 82 Data out 81 Disc in 90 Hold out	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (see DIAG 1). If the first expected tag pattern is hexadecimal 80 with a received pattern of hexadecimal 00, the 'Op In' bit may not be active. The cables that could be wrong are: • Power cables to the shoe card • Cabling of the tag-wrap and terminator blocks • Cabling from the electronic gate to the shoe card If the first expected pattern is hexadecimal A0 and the received pattern is hexadecimal 80, check for a priority connector that is incorrect. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU137 FRU163 FRU152 FRU234 FRU239 FRU195 FRU236 FRU240 FRU196 FRU238 FRU241 FRU154	C12026 EXPECTED TAG DOES NOT MATCH RECEIVED EXP=ee ACT=ff ee Tags expected on inbound tag lines ('op in') ff Tags received on inbound tag lines ('op in')
C12027	The microcode issued a 'tag in' through the channel adapter diagnostic registers and did not receive the expected bit on 'tag out'. 'Status in' was used as a control tag to gate the bit to the tag line driver to be wrapped back through the tag line receiver. Tags issued and expected: Tag Sequence EXP Tag Out 88 Op in 88 Op out 48 Addr in 09 Supp out 28 Sel in 28 Sel out 18 Req in 48 Addr out 08 Stat in 08 Cmd out 0C Serv in 0C Serv out 0A Data in 0A Data out 09 Disc in 18 Hold out	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run EE62 again. Run routine EE64 (See DIAG 1). See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU137 FRU163 FRU152 FRU234 FRU239 FRU195 FRU240 FRU236 FRU196 FRU238 FRU241	C12027 EXPECTED TAG DOES NOT MATCH RECEIVED EXP=ee ACT=ff ee Bits expected on inbound bus lines ('status in') ff Bits received on inbound bus lines ('status in')
C12028	The microcode issued a 'tag in' through the channel adapter diagnostic registers and did not receive the expected bit on 'tag out'. 'Op in' and 'status in' are not activated to gate the tags out. Expected bit patterns: Tag Sequence EXP Tag Out 40 00 20 Sel in 20 Sel out 10 Req in 40 Addr out 04 00 02 00 01 00	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU137 FRU163 FRU152 FRU234 FRU239 FRU195 FRU236 FRU240 FRU196 FRU238 FRU241	C12028 EXPECTED TAG DOES NOT MATCH RECEIVED EXP=ee ACT=ff ee Tags expected on inbound tag lines ff Tags received on inbound tag lines

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C12029	The microcode wrote each 'bus in' bit, one at a time in the diagnostic register, and did not receive the expected bit on 'bus out'. 'Op in' was used as a control tag to gate the bit to the bus line driver to be wrapped back through the bus line receiver. Issued and expected bus sequences: Bus Sequence EXP Bus Out 80 80 40 40 20 20 10 10 08 08 04 04 02 02 01 01	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU136 FRU152 FRU233 FRU195 FRU235 FRU196 FRU237	C12029 EXPECTED BUS DOES NOT MATCH RECEIVED EXP=ee ACT=ff ee Tags expected on inbound tag lines ('op in') ff Tags received on inbound tag lines ('op in')
C1202A	The microcode wrote each 'bus in' bit, one at a time in the diagnostic register, and did not receive the expected bit on 'bus out'. 'Status in' was used as a control tag to gate the bit to the bus line driver to be wrapped back through the bus line receiver. Issued and expected bus sequences: Bus Sequence EXP Bus Out 80 80 40 40 20 20 10 10 08 08 04 04 02 02 01 01	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C12027A EXPECTED BUS DOES NOT MATCH RECEIVED EXP=ee ACT=ff ee Tags expected on inbound tag lines ('status in') ff Tags received on inbound tag lines ('status in')
C1202B	The microcode wrote each 'bus in' bit, one at a time in the diagnostic register, and caused RAM parity errors for each bit. This error can be caused by cabling problems: • Power cables to the shoe card • Cabling of the tag-wrap and terminator blocks • Cabling from the electronic gate to the shoe card	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See the FSI section for error code 5CC1.	FRU233 FRU239 FRU195 FRU235 FRU240 FRU196 FRU237 FRU241	C1202B PROBABLE BUS PARITY PROBLEM ALL BITS FAIL
C1202C	The microcode wrote each 'bus in' bit, one at a time in the diagnostic register, and caused RAM parity errors for one or more but not all bits. This error can be caused by a bit that is continuously active. If one bit does not fail but all others fail, check for that bit being continuously active.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See the FSI section for error code 5CC1.	FRU133 FRU136 FRU163 FRU152 FRU233 FRU239 FRU195 FRU235 FRU240 FRU196 FRU237 FRU241	C1202C ONE OR MORE BUS BITS CAUSED PAR ERROR BITS IN ERROR=xx xx The bit that is 'on' is the failing bit

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C1202D	After setting 'mark in' and no hardware errors detected, bus out bit 0 was not set.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C1202D MARK-IN FAILED TO SET BUS-OUT BIT 0 BUS=xx xx Contents of bus out
C1202E	The microcode wrote all 'bus in' bits without a control tag ('op in' or 'status in'). The lack of a control tag should have caused a 'RAM write parity error'.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See the FSI section for error code 5CC1.	FRU133 FRU152 FRU195 FRU196	C1202E BUS-OUT WTHOUT CNTRL BITS FAILED TO SET WRT RAM PAR ERROR
C1202F	A check 2 error is detected in the processor status register after setting a 'mark in'.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See the FSI section for error code D900.	FRU133 FRU152 FRU195 FRU196	C1202F CHK-2 SET ON MARK-IN WRT. MSNG BUS BIT 0 CAE=cc PSR=yy cc Contents of the channel adapter register yy Contents of the processor status register
C12030	The microcode wrote each 'bus in' bit, one at a time in the diagnostic register, and detected a single missing bit.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. Run routine EE64 (See DIAG 1). See the FSI section for error code 5CC1.	FRU133 FRU136 FRU163 FRU152 FRU233 FRU239 FRU195 FRU235 FRU240 FRU196 FRU237 FRU241	C12030 MISSING BUS BIT ON WRAP TEST FAILING BIT=xx xx The bit that is 'on' is the failing bit
C12031	The microcode issued a channel adapter reset but did not receive hexadecimal 4F as an interrupt code.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE62 again. See the FSI section for error code 33EA.	FRU133 FRU152 FRU195 FRU196 FRU121	C12031 INTRPT VALUE NOT 4F FOLLOWING INIT RESET EXP=ee RCVD=ff ee Expected interrupt code ff Received interrupt code

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C12032	The microcode issued a CMR reset and an interrupt was not generated.	Remove the IML diskette, then press the IML switch to cause a power-on reset. Run routine EE62 again. See the FSI section for error code 33EA.	FRU133 FRU152 FRU195 FRU196 FRU121	C12032 INTRPT NOT GENERATED BY CHANNEL ADAPTER RESET
C12033	The bus parity bit is not working correctly.	Remove the IML diskette, then press the IML switch to cause a power-on reset. Run routine EE62 again. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU136 FRU152 FRU233 FRU195 FRU235 FRU196 FRU237	C12033 BUS PARITY IS NEVER ACTIVE
C12034	Before starting the wrap test, the system reset bit would not reset to zero.	Remove the IML diskette, then press the IML switch to cause a power-on reset. Run routine EE62 again. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU121	C12034 SYSTEM RESET BIT IN THE CHANNEL ADAPTER WOULD NOT RESET
C12035	Unable to reset 'request in'.	Remove the IML diskette, then press the IML switch to cause a power-on reset. Run routine EE62 again. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU121	C12035 REQUEST IN, ADDRESS OUT WOULD NOT RESET DURING TAG WRAP TEST
C12036	After testing 'mark in', 'bus out' would not reset to zero.	Remove the IML diskette, then press the IML switch to cause a power-on reset. Run routine EE62 again. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU121	C12036 BUS OUT WOULD NOT RESET TO ZERO AFTER MARK IN TEST

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C12037	At the completion of the wrap test, 'tag in' would not reset to zero.	Remove the IML diskette, then press the IML switch to cause a power-on reset. Run routine EE62 again. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU137 FRU163 FRU152 FRU234 FRU239 FRU195 FRU236 FRU240 FRU196 FRU238 FRU241	C12037 TAG IN WOULD NOT RESET TO ZERO AT END OF CHANNEL WRAP TEST
C12038	At the completion of the wrap test, 'tag out' would not reset to zero.	Remove the IML diskette, then press the IML switch to cause a power-on reset. Run routine EE62 again. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU137 FRU163 FRU152	C12038 TAG OUT WOULD NOT RESET TO ZERO AT END OF CHANNEL WRAP TEST
C12039	Before starting the wrap test 'tag out' had bit 0 active. Suspect that the channels are still connected or the adapter is broken.	Remove the IML diskette, then press the IML switch to cause a power-on reset. Run routine EE62 again. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU137 FRU163 FRU152 FRU234 FRU239 FRU195 FRU236 FRU240 FRU196 FRU238 FRU241	C12039 OP-OUT TAG IS ACTIVE SUSPECT CHANNEL CABLES ARE INSTALLED
C1203A	The channel adapters in this machine are down level and are not supported by this level support disk.	You should install ECA 025 or use the level of the support disk that you received with your machine. EC A29128 is the last level that supports the down level channel adapters.	FRU133 FRU152 FRU195 FRU196 FRU121	C1203A DOWN LEVEL CHAN ADAP IS NOT SUPPORTED INSTALL ECA 025

Channel Adapter Function Test - Routine EE64

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine tests the functional operation of the channel adapter as follows:

- The channel adapter is tested to ensure that it is installed
- Determines control unit addressability
- Verifies level 6 interrupt generation
- Validates the channel adapter RAM
- Validates all valid channel commands
- Forces all channel command retry functions
- Forces and verifies unit checks
- Forces and verifies busy conditions
- Forces and verifies 'selective reset'.

Routine Start Address: 4010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Addressing: Select and run the channel adapter function test. The following screen is used to select a channel address:

```
CHN ADDR
  (A)
```

(A) Channel Address (valid parameters are A, B, C, or D)

If channel adapter A is to be tested press the enter key. If a different channel adapter is to be tested, enter that channel adapter address and press the enter key.

Enter an 'F' if all channels are to be tested. When the first error is detected, the test stops and the error is displayed.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

External Registers Used

BCC	CAE	MDI	WSE
BCPC	CCA	MDO	
BCPL	CCC	MTI	
BCPH	CDR	MTO	
BCSE	CER	PCR	
BCSL	CMR	PCR	
BCSH	CRR	PDR	
BCSS	DLR	PER	
BCR	DSE	PRR	
BDC	IMR	PSR	
BDSE	LSP	RER	
BMR		RSR	

Channel Tags Bit Meaning

Channel Tags In (TGI) (not an external register)

80	Operational In
40	Address In
20	Select In
10	Request In
08	Status In
04	Service In
02	Data In
01	Disconnect In

Channel Tags Out (TGO) (not an external register)

80	Operational Out
40	Address Out
20	Select Out
10	Hold Out
08	Command Out
04	Service Out
02	Data Out
01	Suppress Out

Channel Adapter Interrupt Description

Note: The x equals the device address (0-F)

Channel Tags In (TGI) (not an external register)

0x	Definition
1x	CCW accepted
2x	Interface disconnect
3x	Selective reset
4x	System reset complete
41	PUT/GET - completed
42	PUT/GET - truncated
43	GET - bus out parity error
44-4E	Reserved
4F	Power on reset complete
5x	CCR - No path
6x	CCR - Buffer conditions
7x	CCR Reject
8x	UC - Status store error or channel adapter error
9x	UC - Command sequence error
Ax	UC - Device assigned to other path group
Bx	UC - Command reject
Cx	UC - Command parity error
Dx	UC - Deferred UC
Ex	UC - Device not ready
Fx	UC - Device file protected

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

Error Analysis

```
CCC=ra    CRR=rb
PSR=rc    PER=rd
DSE=re    WSE=rf
RER=rg    RSR=rh
```

```
MTI=rj    MDI=rk
BCSE=abcde XRA=rl
BDSE=fghkj
ERA=rm    ERB=rn
```

```
BOPE= 0xx
BIPE= 0yy
CHAN ERR=ch  CER=cc
STS=ww   ,CODE=zzzz
```

```
ra = Contents of the channel control card
     register
rb = Contents of the request register
rc = Contents of the processor control register
rd = Contents of the processor error register
re = Contents of the drive status error register
rf = Contents of the write status error register
rg = Contents of the read error register
rh = Contents of the read status register
rj = Contents of the maintenance tag-in register
rk = Contents of the maintenance data-in
     register
rl = Contents of the buffer channel status error
     register
rm = Contents of the buffer drive status error
     register
rn = Contents of the external register address
     register
abcde = Contents external register A
     check 1 errors
fghjk = Contents external register B
     check 1 errors
  0xx = On - There is a channel bus-out parity
          error detected in the channel adapter
          hardware
      Off - No error detected
  0yy = On - There is a channel bus-in parity
          error detected in the channel adapter
          hardware
      Off - No error detected
   cc = contents of the channel error register
   ch = Bit 0 - Status store busy
      Bit 1 - Status store data out parity error
      Bit 2 - Status Store Response out parity
              error
      Bit 3 - Bus out error during a buffer
              write command, Service In
      Bit 4 - Bus out error during a buffer
              write command, Data In
      Bit 5 - Processor detected error
      Bit 6 - External register address or
              write error
      Bit 7 - Hardware detected status store
              error
   ww = Ignore all codes except:
      74 - Error free internal channel adapter
           diagnostics
      78 - An error is detected by the internal
           channel adapter hardware diagnostics
 zzzz = Indicates the sequence of testing by the
      internal channel adapter diagnostics.
      They are in ascending sequence from 1zzz
      through Fzzz.
```

Error Analysis

Analyze the errors for Routine EE64 as follows:

1. Record all information on the error screens.

2. If ERA and ERB are not 0, record the contents (if the screen is displayed) of ERA and ERB. See the FSI section for error code E100 and the following FRU list:

   FRU NAME

   117 Microprocessor card
   115 Maintenance adapter card
   114 Buffer control card
   118 Drive-adapter card
   121 Status store basic card
   119 Read clock and format card
   116 Write data card
   120 Buffer adapter card
   122 Status store communication card
   134 Control store card
   135 Control storage array card

3. If PSR bit 0 = 1 , record the contents (if the screen is displayed) of PSR, PER, XRA, MTI, and MDI). See EAD 1 for error code Fnnn and the following FRU list:

   FRU NAME

   118 Drive-adapter card
   117 Microprocessor card
   115 Maintenance adapter card
   114 Buffer control card
   121 Status store basic card
   119 Read clock and format card
   116 Write data card
   120 Buffer adapter card
   122 Status store communication card

4. If BCSE channel error groups 0-3 indicate any errors, record the contents of BCSE. See the FSI section for error code D5nn and the following FRU list:

   FRU NAME

   114 Buffer control card
   120 Buffer adapter card
   112 Buffer storage card (See note b)
   113 Buffer storage card (See note b)
   133 Channel adapter card (channel A)
   136 Bus shoe card (channel A)
   152 Channel adapter card (channel B)
   233 Bus shoe card (channel B)
   195 Channel adapter card (channel C)
   235 Bus shoe card (channel C)
   196 Channel adapter card (channel D)
   237 Bus shoe card (channel D)
   119 Read clock and format card
   118 Drive-adapter card
   116 Write data card
   126 Power/POR card
   134 Control store card
   121 Status store basic card
   122 Status store communication card

5. If BDSE channel error groups 0-3 indicate any errors, record the contents of BDSE. See the FSI section for error code D6nn and the following FRU list:

   FRU NAME

   114 Buffer control card
   120 Buffer adapter card
   112 Buffer storage card (See note b)
   113 Buffer storage card (See note b)
   111 Read ECC/CORR card
   119 Read clock and format card
   118 Drive-adapter card
   116 Write data card
   134 Control store card
   117 Microprocessor card

6. If DSE bits 0, 1, or 2 = 1, record the contents of DCB, DCR, DSE, DIR, and DTR. See the FSI section for error code D4nn and the following FRU list:

   FRU NAME

   118 Drive-adapter card
   116 Write data card
   134 Control store card
   085 Drive control card (See note a)

7. If any RER bits = 1, or if RSR bits 5, 6, 7 = 1, record the contents of RCR, RRC, RER, RSR, and RDC. See the FSI section for error code D8nn and the following FRU list:

   FRU NAME

   064 Write power card
   062 Read preamplifier card (See note a)
   085 Drive control card (See note a)
   132 Read detect card 3
   131 Read detect card 2
   130 Read detect card 1
   123 Read skew buffer card 1
   124 Read skew buffer card 2
   125 Read skew buffer card 3
   119 Read clock and format card
   111 Read ECC/CORR card

8. If WSE bits 4, 5, or 6 = 1, record the contents of WCR and WSE. See the FSI section for error code D7nn and the following FRU list:

   FRU NAME

   116 Write data card
   120 Buffer adapter card
   114 Buffer control card
   117 Microprocessor card
   118 Drive-adapter card
   139 Logic board A1

9. If BOPE is ON, BIPE is ON, CHAN ERR is not 0, or CER bits 0, 1, or 2 = 1, record the contents of CER. See the FSI section for error code 54nn and the following FRU list:

   FRU NAME

   133 Channel adapter card (channel A)
   152 Channel adapter card (channel B)
   195 Channel adapter card (channel C)
   196 Channel adapter card (channel D)
   117 Microprocessor card
   121 Status store basic card
   122 Status store communication card
   197 Channel address switch for channels A, B, C, or D.

Notes:

1. *EC sensitive FRU, see CARR-DR 4.*

2. *EC sensitive FRU, see CARR-CU 7.*

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
CI4021	The service representative (SR) entered an invalid channel adapter address. The address received by the microcode is shown in the ADDRESS RCVD field. This could be an MD communication error.	Ensure that the maintenance device (MD) is working correctly. See REF screen or Error Displays.	The MD FRU169	CI4021 INVALID CA ADDRESS VALID = A B C D F ADDRESS RCVD = xx xx Data received by the microcode
CI4022	A channel adapter was selected that is not installed, or the status store to channel adapter communication data path is bad. The microcode did not receive the correct response from status store for channel adapter reset.	Run routine EE64 once on each channel adapter. Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE64 again. See the FSI section for error code 2060.	FRU133 FRU152 FRU195 FRU196 FRU121 FRU250 FRU251	CI4022 CHANNEL ADAPTER NOT PLUGGED. DOES NOT ACKNOWLEDGE
CI4023	The microcode attempted to force the channel adapter offline but was not successful.	Run routine EE64 once for each channel. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU250 FRU251	CI4023 CANNOT TAKE CHANNEL ADAPTER OFF-LINE
CI4024	The status store did not acknowledge an order from the channel adapter card.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE64 again. See the FSI section for error code 5310.	FRU121	CI4024 CHANNEL ADAPTER DID NOT ACKNOWLEDGE LAST ORDER CHNL CMD=cc CA ADDR=ca CA CMD= co CA DATA=cd ca The failing channel adapter cc The failing channel command cd Channel adapter order co Channel adapter data

Notes

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
CI4025	The microcode detected a check 2 error condition and stopped the test.	FRUs are listed on error analysis on page 320. 1. a. Remove the IML diskette, then press the IML switch to cause a power-on-reset. b. Rerun either routine EE62 or routine EE64.		CI4025 A CHECK-2 ERROR CONDITION WAS DETECTED CER=cc CAE=bb PSR=rr PER=pp DSE=ds WSE=ww RER=re RSR=rs MTI=mm BCSE=abcde BDSE=fg ERA=ra ERB= rb a Buffer channel status and error register bits 0-3 b Channel error group 0 c Channel error group 1 d Channel error group 2 e Channel error group 3 f Buffer device status and error register bits 0-3 g Buffer device error group 0 bb Channel adapter errors for channels A-D cc Contents of the channel error register ds Contents of the device status/error register mm Contents of the maintenance tag in register pp Contents of the processor error register ra External register A check 1 errors rb External register B check 1 errors re Contents of the read error register rr Contents of the processor status register rs Contents of the read status register ww Contents of the write/status error register
CI4026	The microcode attempted to force a diagnostic interrupt ('F8') and was not successful. Channel Adapter Addresses from the channel control card external register: 80 = channel adapter A 40 = channel adapter B 20 = channel adapter C 10 = channel adapter D	Run routine EE64 once for each channel. Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE64 again. See the FSI section for error code 54nn.	FRU133 FRU152 FRU195 FRU196 FRU250 FRU251	CI4026 LEVEL 6 INTERRUPT DID NOT OCCUR CCC=aa CRR=bb aa Contents of the channel card control register bb Contents of the channel request register
CI4027	The microcode detected a read back miss compare after writing channel adapter RAM addresses.	See the FSI section for error code 3302.	FRU133 FRU152 FRU195 FRU196 FRU121 FRU250 FRU251	CI4027 DATA MSCMPR DURING CA RAM READ TESTING EXP=ee RCVD=ff ee Expected channel adapter RAM data ff Received channel adapter RAM data

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C14028	More than one control unit address responded to initial selection.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE64 again. Ensure the control unit address switch is set correctly. See the FSI section for error code 2705.	FRU133 FRU152 FRU195 FRU196 FRU173 FRU153 FRU197	C14028 MULTI CU ADDRESS RESPONDED TO SELECT ADDR1=gg ADDR2=hh gg The first control unit address that responded hh The second control unit address that responded
C14029	The received 'tag in' did not match the expected 'tag in' during a channel command execution.	Compare the actual tags in (TGI) to the TGI EXPECTED tags in, to determine the failing tag. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU114 FRU120 FRU126 FRU250 FRU251 FRU256	C14029 CHANNEL IN TAGS ARE WRONG CA=ca CHNL CMD=cc TGO=jj TGI=kk TG1 EXPECTED=mm ca The failing channel adapter cc The failing channel address jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings. kk Actual 'tag in' data. See "Error Displays" on DIAG 320 for bit meanings. mm Expected 'tag in' data
C1402A	The received address ('bus in') did not match the address ('bus out') from the microcode.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU250 FRU251	C1402A DEV ADDR ON BUS IN DOES NOT MATCH EXPECTED BUS IN CA=ca CHNL CMD=cc TGO=jj BUSO=bo BUSI=bi BUSI EXPECTED=mm ca The failing channel command cc The failing channel command jj Current 'tag out' data See "Error Displays" on DIAG 320 for bit meanings bo 'Bus out' data bi Actual address on 'bus in' mm Expected address on 'bus in'
C1402B	The microcode received no response from any control unit address (0-F) when attempting an initial selection sequence.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE64 again. See the FSI section for error code 2060.	FRU133 FRU152 FRU195 FRU196 FRU173 FRU153 FRU197	C1402B CU DID NOT RESPOND TO ADDRESS 0-F CK CU ADDR SWITCH

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C1402C	The received interrupting channel adapter address does not match the current channel adapter.	Run routine EE64 once for each channel. See the FSI section for error code 5350.	FRU133 FRU152 FRU195 FRU196	C1402C WRONG CA ADDRESS CAUSED INTERRUPT CA=ca CHNL CMD=cc TGO=jj INTRPT=ai EXP INTRPT=ei ca The failing channel adapter cc The failing channel command ai Actual interrupt received. See "Error Displays" on DIAG 320 for interrupt descriptions. ei Expected interrupt jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings.
C1402D	The channel adapter decodes a unique 5-bit code for each channel command.	See the FSI section for error code 52nn.	FRU133 FRU152 FRU195 FRU196	C1402D CHNL CMD DID NOT DECODE TO PROPER 5 BIT DECODE CA=ca CHNL=cc TGO=jj EXP 5 BIT DECODE=ed RCVD 5 BIT DECODE=rd ca The failing channel adapter cc The failing channel command ed Expected 5 bit decode from channel command rd Received 5 bit decode from channel command jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings.
C1402E	The 'bus in' data did not match the expected data on a read forward channel command. A previous Write command could be the fault.	Run routine EE64 once for each channel. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU121 FRU114 FRU120 FRU112[1] FRU113[1] FRU256	C1402E READ DATA MISCOMPARE DATA WAS: EXP=ee RCVD=ff ee Bits expected on inbound bus lines ff Bits received on inbound bus lines
C1402F	The channel adapter failed to reserve the selected device.	Run routine EE64 once for each channel. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C1402F ASSIGNMENT PATH FAILED FOR INITIAL SELECTION

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C14030	The BCSE register did not indicate stop after the microcode raised 'command out' through the channel adapter.	See the FSI section for error code A131.	FRU114 FRU120 FRU112[1] FRU113[1] FRU133 FRU152 FRU195 FRU196 FRU256	C14030 BCSE CHNL STOP NOT DETECTED FOLLOWING A WRITE COMMAND CA=ca CHNL CMD=cc BYTE CNT=by BCSE=abcde a Buffer channel status and error register bits 0-3 b Channel error group 0 c Channel error group 1 d Channel error group 2 e Channel error group 3 by Byte count of the data transferred ca The failing channel adapter cc The failing channel command
C14031	The channel adapter failed to release the selected device.	Run routine EE64 once for each channel. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C14031 DEVICE WAS NOT RELEASED AFTER FALL OF HOLD OUT
C14032	'Service in' or 'data in' was detected after the expected end of read data.	See the FSI section for error code A131.	FRU133 FRU152 FRU195 FRU196	C14032 TOO MANY SERVICE OR DATA IN ON READ COMMAND
C14033	Programming error.	Call your next level of support.		C14033 PROGRAMMING ERROR NO INPUT FOR COMMAND TYPE
C14034	The channel adapter RAM data was incorrect following a GET type channel command. The data in RAM should be in a first-in, last-out sequence.	Run routine EE64 once for each channel. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU121	C14034 RAM DATA MISCOMPARE AFTER GET COMMAND EXP=ee ACT=ff ee Bits expected from channel adapter RAM ff Bits received from channel adapter RAM
C14035	The read data ('bus in') was in error during a PUT type command. The expected data is pre-loaded by the microcode and checked during the data transfer (such as a Sense command).	Run routine EE64 once for each channel. See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU121	C14035 BUS IN DATA MISCOMP ON PUT COMMAND EXP=ee RCVD=ff ee Bits expected on bus lines ff Bits received on bus lines

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C14036	The microcode did not determine that a channel adapter is present. The channel adapter is not tested.	Ensure that the channel adapter card is plugged. If it is plugged, this is an error. If it is not plugged, ignore this message. When running the Basic CU Test or E010, this message is not displayed unless an error occurs. See the FSI section for error code 53A0.	FRU133 FRU152 FRU195 FRU196 FRU121	C14036 THE FOLLOWING ADAPS WERE NOT TESTED 00 Bits 0-3 correspond to channels A-D respectively. If the bit is on, the channel was not tested. Bits 4-7 are not used.
C14037	The microcode sent a channel adapter order and status store did not indicate that it was completed (CRR bit 7).	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE64 again. See the FSI section for error code 5311.	FRU133 FRU152 FRU195 FRU196 FRU121 FRU250 FRU251	C14037 CHANNEL ADAPTER DID NOT COMPLETE LAST ORDER CHNL CMD=cc CA ADDR=ca CA CMD=co CA DATA=cd ca The failing channel adapter cc The failing channel command cd Channel adapter data co Channel adapter order
C14038	The device address was bypassed during a select attempt.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C14038 RECEIVED SELECT-IN DURING INITIAL SELECTION CA=ca CHNL CMD=cc TG0=jj TG1=kk TG1 EXPECTED=mm ca The failing channel adapter cc The failing channel command jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings. kk Actual 'tag in' data. See "Error Displays" on DIAG 320 for bit meanings. mm Expected 'tag in' data
C14039	The channel adapter did not respond with 'service in' to a read type channel command.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196 FRU256	C14039 SERVICE-IN NOT DETECTED DURING DATA TRANSFER CA=ca CHNL CMD=cc TG0=jj TG1=kk TG1 EXPECTED=mm ca The failing channel adapter cc The failing read type channel command jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings. kk Actual 'tag in' data. See "Error Displays" on DIAG 320 for bit meanings. mm Expected 'tag in' data

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C1403A	The channel adapter did not respond with 'service in' to a write type channel command.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C1403A SERVICE-IN NOT DETECTED DURING DATA TRANSFER CA=ca CHNL CMD=cc TGO=jj TG1=kk TG1 EXPECTED=mm ca The failing channel adapter cc The failing write type channel command jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings. kk Actual 'tag in' data. See "Error Displays" on DIAG 320 for bit meanings. mm Expected 'tag in' data
C1403B	The received 'status in' ('bus in') did not match the expected 'status in'.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C1403B CHAN STATUS ON BUS IN DOES NOT MATCH EXPECTED BUS IN CA=ca CHNL CMD=cc TGO=jj BUSO=bo BUSI=bi BUSI EXPECTED =mm bi Actual status on 'bus in' bo 'Bus out' data ca The failing channel adapter cc The failing channel command jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings. mm Expected status on 'bus in'
C1403C	An unexpected channel command retry was requested by the channel adapter microcode.	See the FSI section for error code 38C0.	FRU133 FRU152 FRU195 FRU196	C1403C UNEXP CCR ON LAST CHANNEL COMMAND MARK-IN IS ACTIVE CA=ca CHNL CMD=cc TGO=jj BUSO=bo BUSI=bi BUSI EXPECTED =mm bi Actual status on 'bus in' bo 'Bus out' data ca The failing channel adapter cc The failing channel command jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings. mm Expected status on 'bus in'

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C1403D	The microcode forced a busy condition and the received status did not match the expected status.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C1403D FORCED BUSY STATUS NOT AS EXPECTED CA=ca CHNL CMD=cc TGO=jj BUSO=bo BUSI=bi BUSI EXPECTED =mm bi Actual status on 'bus in' bo 'Bus out' data ca The failing channel adapter cc The failing channel command jj Current 'tag out' data. See "Error Displays" on DIAG 320 for bit meanings. mm Expected status on 'bus in'
C1403E	A channel adapter generated interrupt did not match the expected interrupt.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C1403E INTERRUPT RECEIVED NOT EXPECTED DURING INITIAL SELECTION CA=ca CHNL CMD=cc TGO=jj INTRPT=ai EXP INTRPT=ei ai Actual interrupt received. See "Error Displays" on DIAG 320 for interrupt descriptions. ca The failing channel adapter cc The failing channel command ei Expected interrupt
C1403F	The channel adapter did not respond with an expected interrupt.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C1403F FREE DEV INTERRUPT DID NOT OCCUR CA=ca CHNL CMD=cc TGO=jj INTRPT=ai EXP INTRPT=ei ai Actual interrupt received. See "Error Displays" on DIAG 320 for interrupt descriptions. ca The failing channel adapter cc The failing channel command ei Expected interrupt
C14040	A PUT type channel command did not generate an interrupt at the expected end of data.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C14040 PUT INTERRUPT NOT DETECTED ON LAST DATA BYTE CA=ca CHNL CMD=cc TGO=jj INTRPT=ai EXP INTRPT=ei ai Actual interrupt received. See "Error Displays" on DIAG 320 for interrupt descriptions. ca The failing channel adapter cc The failing channel command ei Expected interrupt

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C14041	The channel adapter responded with an unexpected interrupt.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C14041 INTERRUPT RECEIVED WAS NOT AS EXPECTED CA=ca CHNL CMD=cc TGO=jj INTRPT=ai EXP INTRPT=ei ai Actual interrupt received. See "Error Displays" on DIAG 320 for interrupt descriptions. ca The failing channel adapter cc The failing write type channel command ei Expected interrupt
C14042	A 'unit check' was detected during initial selection.	See EAD 1, "Status Store/Channel Adapter."	FRU133 FRU152 FRU195 FRU196	C14042 UNEXPECTED UNIT CHECK DURING INITIAL SELECTION CA=ca CHNL CMD=cc TGO=jj INTRPT=ai EXP INTRPT=ei ai Actual interrupt received ca The failing channel adapter cc The failing channel command ei Expected interrupt
C14043	The BCSE register did not indicate complete on a Write CRC operation from the channel buffer.	See the FSI section for error code A140.	FRU133 FRU152 FRU195 FRU196 FRU114 FRU120 FRU112[1] FRU113[1] FRU256	C14043 BCSE MP WRITE COMP NOT DETECTED FOLLOWING WRITE CRC CA=ca CHNL CMD=cc BYTE CNT=by BCSE=abcde a Buffer channel status and error register bits 0-3 b Channel error group 0 c Channel error group 1 d Channel error group 2 e Channel error group 3 ca The failing channel adapter cc The failing channel command
C14044	The BCSE register did not indicate channel pointer stop after reading all the data from the data buffer.	See the FSI section for error code A131.	FRU133 FRU152 FRU195 FRU196 FRU114 FRU120 FRU112[1] FRU113[1] FRU256	C14044 BCSE CHNL PNTR STOP NOT DETECTED CA=ca CHNL CMD=cc BYTE CNT=by BCSE=abcde a Buffer channel status and error register bits 0-3 b Channel error group 0 c Channel error group 1 d Channel error group 2 e Channel error group 3 ca The failing channel adapter cc The failing channel command

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C14045	Any buffer error was detected in the BCSE register.	See the FSI section for error code A170.	FRU133 FRU152 FRU195 FRU196 FRU114 FRU120 FRU112[1] FRU113[1] FRU256	C14045 BUFFER ERROR DETECTED FOLLOWING READ OR WRITE CMD. CA=ca CHNL CMD=cc BYTE CNT=by BCSE=abcde a Buffer channel status and error register bits 0-3 b Channel error group 0 c Channel error group 1 d Channel error group 2 e Channel error group 3 ca The failing channel adapter cc The failing channel command by 01 for Write command or 02 for Read command
C14046	Programming error. Command data taken from a control table was not a Read command.	Call your next level of support.		C14046 READ CMD DOES NOT XLATE TO EITHER FORWARD OR BACKWARD
C14047	Programming error. Byte count taken from a control table was greater than 32.	Call your next level of support.		C14047 ILLEGAL BYTE COUNT FOR PUT COMMAND CNT=bc bc Byte count
C14048	The service representative (SR) entered an invalid channel adapter address. The address received by the microcode is shown in the ADDRESS RCVD field. This could be an MD communication error.	Ensure that the Maintenance device (MD) is working correctly. See REF screen or Error Displays.	The MD FRU169	C14048 INVALID CA ADDRESS VALID = A B C D F ADDRESS RCVD = xx xx Data received by the microcode
C14049	The status store did not acknowledge an order from the channel adapter card.	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE64 again. See the FSI section for error code 5310.	FRU121	C14049 CHANNEL ADAPTER DID NOT ACKNOWLEDGE LAST ORDER CA ADDR=ca CA CMD= co CA DATA=cd ca The failing channel adapter cd Channel adapter order co Channel adapter data

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C1404A	The microcode sent a channel adapter order and status store did not indicate that it was completed (CRR bit 7).	Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE64 again. See the FSI section for error code 5311.	FRU133 FRU152 FRU195 FRU196 FRU121 FRU250 FRU251	C1404A CHANNEL ADAPTER DID NOT COMPLETE LAST ORDER CA ADDR=ca CA CMD=co CA DATA=cd ca The failing channel adapter cd Channel adapter data co Channel adapter order
C1404B	Unexpected errors have occurred which are either check 1, check 2, or internal channel adapter errors.	See DIAG 320, "Error Analysis."		C1404B A "CU" OR "CA" ERROR CONDITION WAS DETECTED
C1404C	The microcode detected a read back miss compare after writing channel adapter RAM addresses.	See the FSI section for error code 3302. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196 FRU121 FRU250 FRU251	C1404C READ DATA MISCOMPARE DATA IS: EXP=ee RCVD=ff ee Expected channel adapter RAM data ff Received channel adapter RAM data
C1404D	The received tag-in did not match the expected tag-in during the data transfer of write data to the buffer, or read data from the buffer.	Compare the received tag-in to the expected tag-in to determine the failing tag.	FRU133 FRU152 FRU195 FRU196 FRU114 FRU120 FRU126 FRU250 FRU251 FRU256	C1404D CHANNEL IN TAGS ARE WRONG. CA ADDR=ca TAGS OUT=to TAGS IN=aa EXP TAGS IN=bb ca Failing channel adapter address to Last tag-out, Service Out or Data Out aa Tags-in received. See "Error Displays" on DIAG 320 for bit meanings. bb Tags-in expected. See "Error Displays" on DIAG 320 for bit meanings.
C1404E	The received interrupting channel adapter address does not match the current channel adapter.	Run routine EE64 once for each channel. See the FSI section for error code 5350. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196	C1404E WRONG CA ADDRESS CAUSED INTERRUPT
C1404F	The microcode detected a read back miss compare after writing channel adapter data to the data buffer.	See the FSI section for error code 3302. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196 FRU121 FRU250 FRU251	C1404F READ DATA MISCOMPARE DATA IS: EXP=ee RCVD=ff ee Expected buffer data ff Received buffer data

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C14050	The BCSE register did not indicate stop after the microcode raised 'command out' through the channel adapter.	See the FSI section for error code A131. See DIAG 320, "Error Analysis."	FRU114 FRU120 FRU112[1] FRU113[1] FRU133 FRU152 FRU195 FRU196 FRU256	C14050 BCSE CHNL STOP NOT DETECTED FOLLOWING A WRITE COMMAND
C14051	'Service in' or 'data in' was detected after the expected end of read data.	See the FSI section for error code A131. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196	C14051 TOO MANY SERVICE-IN OR DATA-IN ON READ COMMAND
C14052	Programming error.	Call your next level of support. See DIAG 320, "Error Analysis."		C14052 PROGRAMMING ERROR
C14053	The channel adapter did not acknowledge a channel adapter reset. The channel adapter is not tested.	Ensure that the channel adapter card is plugged. If it is plugged, this is an error. If it is not plugged, ignore this message. When running the Basic CU Test or E010, this message is not displayed unless an error occurs. See CARR-CU 1189 for the correct DLR switch settings. See the FSI section for error code 53A0. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196 FRU121	C14053 THE FOLLOWING ADAPS WERE NOT TESTED: 00 DLR= YY Bits 0-3 correspond to channels A-D respectively. If the bit is on, the channel was not tested. Bits 4-7 are not used. yy = Contents of the DLR external register
C14054	The BCSE register did not indicate complete on a Write CRC operation from the channel buffer.	See the FSI section for error code A140. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196 FRU114 FRU120 FRU112[1] FRU113[1] FRU256	C14054 MP WRITE COMP NOT DETECTED FOLLOWING A WRITE CRC
C14055	The BCSE register did not indicate channel pointer stop after reading all the data from the data buffer.	See the FSI section for error code A131. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196 FRU114 FRU120 FRU112[1] FRU113[1] FRU256	C14055 CHNL PNTR STOP NOT DETECTED FOLLOWING A READ COMMAND

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C14056	Any buffer error was detected in the BCSE register.	See the FSI section for error code A170. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196 FRU114 FRU120 FRU112[1] FRU113[1] FRU256	C14056 BUFFER ERROR DETECTED FOLLOWING READ OR WRITE CMD.
C14057	The microcode detected and unexpected level 6 interrupt. Channel Adapter Addresses from the CCC external register: 80 = channel adapter A 40 = channel adapter B 20 = channel adapter C 10 = channel adapter D	Compare the contents of the CCC register with the CRR register, they should be the same. If not, a channel adapter has failed and either no interrupt is set or multiple interrupts are set. See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196 FRU121 FRU250 FRU251	C14057 HOT LEVEL 6 INTRPT. FOLLOWING A RESET CCC=aa CRR=bb aa Contents of the channel card control register bb Contents of the channel request register
C14058	At this time the processor should be in the correct level indicated by the expected data.	Compare the actual contents of the PSR register to the expected contents, they should be the same. See DIAG 320, "Error Analysis."	FRU117 FRU133 FRU152 FRU195 FRU196	C14058 PSR IS NOT CORRECT INTERRUPT TEST EXP=aa ACT=bb aa Expected contents of the PSR external register bb Actual contents of the PSR external register
C14059	Channel adapter internal diagnostics did not complete. Correct completion is indicated by the ending status being set, along with a level 6 interrupt.	See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196	C14059 LEVEL 6 INTERRUPT DID NOT OCCUR
C1405A	Channel adapter internal diagnostics detected an error during execution.	See DIAG 320, "Error Analysis."		C1405B CHANNEL ADAPTER DIAGNOSTICS FAILED
C1405B	Unexpected errors have occurred, either check 1, check 2, or internal channel adapter errors.	See DIAG 320, "Error Analysis."		C1405B A "CU" or "CA" ERROR CONDITION WAS DETECTED

[1] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
C1405C	The internal channel adapter parameter data should be 'FF'. An error may have been detected before the parameter was set.	See DIAG 320, "Error Analysis."		C1405C CAC1 DATA ERROR FIRST LVL 6 INTRPT. EXP=ee ACT=ff ee Data expected ff Data received
C1405D	The internal channel adapter diagnostic has forced a level 6 interrupt, however, it is not detected by the control unit microcode.	See DIAG 320, "Error Analysis."		C1405D MID TEST CA INTRPT. DID NOT OCCUR.
C1405E	The internal channel adapter diagnostic forced an error, however, when the CER was checked it did not have the correct channel error set.	See DIAG 320, "Error Analysis."	FRU133 FRU152 FRU195 FRU196 FRU250 FRU251	C1405E EXPECTED CER ERROR DID NOT OCCUR. EXP=ee ACT=ff ee Data expected ff Data received
C1405F	The channel adapter address-switch test detected a parity error while reading the channel adapter address switch (the thumbwheel switch).	See DIAG 320, "Error Analysis." The cables associated with this failure are in cable groups 23A, 23B, 23C, and 23D. See FSI 1 for "Cable Group Table."	FRU197 FRU133 FRU152 FRU195 FRU196	C1405F CHANNEL ADAPTER ADDR THUMB WHEEL SWITCH PARITY ERROR.
C14060	The channel adapter address-switch test detected an undefined mode while reading the channel adapter address switch (the thumbwheel switch).	See DIAG 320, "Error Analysis." The cables associated with this failure are in cable groups 23A, 23B, 23C, and 23D. See FSI 1 for "Cable Group Table."	FRU197 FRU133 FRU152 FRU195 FRU196	C14060 CHANNEL ADAPTER ADDR THUMB WHEEL SWITCH INVALID MODE.
C14061	The channel adapters in this machine are down level and are not supported by this level support disk.	You should install ECA 025 or use the level of the support disk that you received with your machine. EC A29128 is the last level that supports the down level channel adapters.	FRU133 FRU152 FRU195 FRU196 FRU121	C14061 DOWN LEVEL CHANNEL ADAPTER IS NOT SUPPORTED. INSTALL ECA 025.

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine consists of five tests.

Routine Start Address: 5010

Test 1

- Tests the external register address extend bits (bits 6 and 7) and the path from the process control register as it is used for external register addressing.
- Tests external address error detection.

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Test 2

- Ensures that an external register error causes a level 0 interrupt
- Tests the path from the processor control register as it is used for external register addressing.

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Test 3

- Tests that writable external registers can be written to and that readable external registers can be read. The data written is ripple data 00 through FF. After each write, the data is read and the read data is compared to the written data.

Error Loop - XR Register Write: Loop on the same XR address writing the same data.

Error Loop - XR Register Read: Loop on the same XR address reading the same data.

Test 3 External Register Test Sequence

START

REG NAME	WRT REG	RD REG
CCC	X	X
MDO	X	
CDR	X	
CMR	X	
ITC	X	
DCB	X	
CER	X	
CRR	X	
DLR	X	
DSH	X	
DSL	X	
DIR	X	
DSE	X	
MDI	X	

REG NAME	WRT REG	RD REG	
RCR	X	X	
RDC	X	X	
BCPL	X	X	
BDPH	X	X	
BDPL	X	X	
BCSH	X	X	
BCSL	X	X	
BDSH	X	X	
BDSL	X	X	
BWRP	X	X	
BCC	X		
BCSE	X	X	*
BCR	X	X	*
BCSS	X	X	*

REG NAME	WRT REG	RD REG	
BDC	X	X	
BDSE	X		
BDR	X	X	
BDSS	X	X	
BDPH	X	X	
BCPC	X		
WSE	X		
RSR	X		
RER	X		
RRC	X		
RPR	X		
BDG0	X	X	*
BDAT	X		*
BMR	X		*

END

NOTE: If the Improved Data Recording Capability or the 4.5 Mb/s feature is installed, the feature registers are tested in place of the registers preceded by an *.

FEATURE REGS

REG NAME	WRT REG	RD REG
CMRS	X	X
CMM	X	X
CIM	X	X
CMDT	X	X
CMS	X	

Test 4

- Tests that external register errors can be set when bad parity data is written to writable registers
- Does not test processor external registers.

Error Loop - XR Register Write: Loop on the same XR address writing 00.

Test 4 External Register Test Sequence

(1) CCC
(2) CCA
(3) CDR
(4) ITC
(5) DCB
(6) DTR
(7) DSC
(8) DSR
(9) MDO
(10) WCR
(11) RCR
(12) RDC
(13) BCPH
(14) BCPL
(15) BDPH
(16) BDPL
(17) BCSH
(18) BCSL
(19) BWRP
(20) BCC
(21) BCSE
(22) BCR
(23) BCSS
(24) BDC
(25) BDSE
(26) BDR
(27) BDSS
(28) BCPC
*(29) BDAT
*(30) BDG0
*(31) BDG1
*(32) BMR

Test 5

- Ensures that external register address errors are set when addresses that are not valid are written to or read from the external register bus.

Error Loop - XR Write: Loop on the same XR address writing 00 and inhibit parity.

Error Loop - XR Read: Loop on the same XR address reading.

Test 5 Address Test Sequence For Addresses That Are Not Valid

- Write and Read Addresses:
  - A04 through A0F
  - A13 through A17
  - B08 through B0F
  - C00 through C0F
  - C14 through C17
  - D13 and D14 (Valid if the 4.5 Mb/s or Improved Data Recording Capability features are installed).
- Write Only Addresses:
  - A07
  - A10 through A12
  - B01
  - B03 through B06
  - B10
  - B13
  - C12
  - C19
  - D19
- Read Only Addresses:
  - A18
  - B18
  - D0D

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

0 0 0 0 0 0 0 0 0 0

External Register Bus Addressing and Data Pattern Test - Routine EE85

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine consists of five tests.

Routine Start Address: 5010

Test 1

- Tests the external register address extend bits (bits 6 and 7) and the path from the process control register as it is used for external register addressing.
- Tests external address error detection.

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Test 2

- Ensures that an external register error causes a level 0 interrupt
- Tests the path from the processor control register as it is used for external register addressing.

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Test 3

- Tests that writable external registers can be written to and that readable external registers can be read. The data written is ripple data 00 through FF. After each write, the data is read and the read data is compared to the written data.

Error Loop - XR Register Write: Loop on the same XR address writing the same data.

Error Loop - XR Register Read: Loop on the same XR address reading the same data.

Test 3 External Register Test Sequence

START

REG NAME	WRT REG	RD REG
CCC	X	X
MDO	X	
CDR	X	
CMR	X	
ITC	X	
DCB	X	
CER	X	
CRR	X	
DLR	X	
DSH	X	
DSL	X	
DIR	X	
DSE	X	
MDI	X	

REG NAME	WRT REG	RD REG
RCR	X	X
RDC	X	X
BCPL	X	X
BDPH	X	X
BDPL	X	X
BCSH	X	X
BCSL	X	X
BDSH	X	X
BDSL	X	X
BWRP	X	X
BCC	X	
BCSE	X	X
BCR	X	X
BCSS	X	X

REG NAME	WRT REG	RD REG
BDC	X	X
BDSE	X	
BDR	X	X
BDSS	X	X
BDPH	X	X
BCPC	X	
WSE	X	
RSR	X	
RER	X	
RRC	X	
* RPR	X	
* BDGO	X	X
* BDAT	X	
* BMR	X	

END

4.5 MB/S REGS

REG NAME	WRT REG	RD REG
CMRS	X	X
CMM	X	X
CHM	X	X
CMDT	X	X
CMS	X	

NOTE: If the 4.5 Mb/s channel feature is installed, the 4.5 Mb/s registers are tested in place of the registers preceded by an *.

Test 4

- Tests that external register errors can be set when bad parity data is written to writable registers
- Does not test processor external registers.

Error Loop - XR Register Write: Loop on the same XR address writing 00.

Test 4 External Register Test Sequence

(1) CCC
(2) CCA
(3) CDR
(4) ITC
(5) DCB
(6) DTR
(7) DSC
(8) DSR
(9) MDO
(10) WCR
(11) RCR
(12) RDC
(13) BCPH
(14) BCPL
(15) BDPH
(16) BDPL
(17) BCSH
(18) BCSL
(19) BWRP
(20) BCC
(21) BCSE
(22) BCR
(23) BCSS
(24) BDC
(25) BDSE
(26) BDR
(27) BDSS
(28) BCPC
(29) BDAT
(30) BDG0
(31) BDG1
(32) BMR

Test 5

- Ensures that external register address errors are set when addresses that are not valid are written to or read from the external register bus.

Error Loop - XR Write: Loop on the same XR address writing 00 and inhibit parity.

Error Loop - XR Read: Loop on the same XR address reading.

Test 5 Address Test Sequence For Addresses That Are Not Valid

- Write and Read Addresses:
  - A04 through A0F
  - A13 through A17
  - B08 through B0F
  - C00 through C0F
  - C14 through C17
  - D13 and D14 (Valid if the 4.5 Mb/s feature is installed).
- Write Only Addresses:
  - A07
  - A10 through A12
  - B01
  - B03 through B06
  - B10
  - B13
  - C12
  - C19
  - D19
- Read Only Addresses:
  - A18
  - B18
  - D0D

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

External Register Table (XRT)

Word 0

Note: The bits in the following table are contained in the first byte of word 0 of the XRT.

Bit	Label	Area	Description/Detail
Bit 0	HIT2A	XR A Bus Flags	Two or more external registers failed while testing the registers on bus A.
Bit 1	HIT1A	XR A Bus Flags	One external register failed while testing the registers on bus A.
Bit 2	WRAF	XR A Bus Flags	A failure was detected while writing a register on bus A.
Bit 3	RDAF	XR A Bus Flags	A failure was detected while reading a register on bus A.
Bit 4	HIT2B	XR B Bus Flags	Two or more external registers failed while testing the registers on bus B.
Bit 5	HIT1B	XR B Bus Flags	One external register failed while testing the registers on bus B.
Bit 6	WRBF	XR B Bus Flags	A failure was detected while writing a register on bus B.
Bit 7	RDBF	XR B Bus Flags	A failure was detected while reading a register on bus B.

Tests 1 and 2 Error Displays

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
XB5021	XR error is on after the hardware, check 1, and user reset at the start of the first test in routine EE85.	To help in problem isolation, also run diagnostics EE10, EE30, EE40, EE50, EE60 EE90, and EEA0. 1. Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE85 again. 2. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. Also see action number 4 of this Additional Actions column. 3. If PSR bit 0 = 1, see EAD 1 for error code Fnnn. 4. If a diagnostic failure occurs and no errors are detected by the hardware, see the FSI section for error code E100 and perform the procedures for the microprocessor and control storage. 5. XR errors (PSR bit 0 = 1) can cause ERA and ERB errors. Use diagnostic EE10 to check the ERA and ERB registers. 6. If ERA and ERB are not 0, record the contents (if the screen is displayed) of ERA and ERB and see the FSI section for error code E100. 7. If PSR bit 0 = 1, record the contents of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn. 8. If BCSE channel error groups 0-3 indicate any errors, record the contents of BCSE. See the FSI section for error code D5nn. 9. If BDSE channel error groups 0-3 indicate any errors, record the contents of BDSE. See the FSI section for error code D6nn. 10. If DSE bits 0, 1, or 2 = 1, record the contents of DCB, DCR, DSE, DIR, and DTR. See the FSI section for error code D4nn. 11. See EAD 1, "Drive Interconnections." If any RER bits = 1, or if RSR bits 5, 6, or 7 = 1, record the contents of RCR, RRC, RER, RSR, and RDC. See the FSI section for error code D8nn. 12. If WSE bits 4, 5, or 6 = 1, record the contents of WCR and WSE. See the FSI section for error code D7nn. 13. If CER bits 0, 1, or 2 = 1, record the contents of CER and AER. See the FSE section for error code 55nn.	FRU121 FRU118 FRU117 FRU115 FRU114 FRU120 FRU119 FRU116 FRU134 FRU135 FRU157 FRU158 FRU159 FRU139	nnnnnn ERA = ra, ERB = rb PSR = rr, PER = pp MTI = mm, MDI = md (This screen is explained on DI HOT BITS XR BUS = aa XRA EXP = ex, ACT=ac MACHINE FAILURES MAY CAUSE CURRENT ERROR DATA TO BE INVALID. SEE DIAG 1 "VERIFY". nnnnnn Failure ID ** No errors were set ra Contents of error register A rb Contents of error register B rr Contents of the processor status register pp Contents of the processor error register mm Contents of the maintenance tag in register. md Contents of the users active register aa Result of ANDing data from registers on the XR bus. ac Actual data in external register address register ex Expected data in external register address register.
XB5022	The XRA did not match the data compare table during the test of all possible combinations of data into the XRA.			
XB5023	An XR error occurred while using procedure registers during the testing of XRA.			
XB5024	An error occurred while using the diagnostic mode to force an error while writing to the JAH register (data equal 00), and using extend bits for addressing external registers A or B. An XR error is expected along with specific data in XRA.			
XB5025	An XR or check 2 error is on unexpectedly during test of XRA following a user test.			
XB5026	1. An XR error is forced causing a level 0 interrupt. These results are expected: XR error, check 2, and user write error. 2. An XR interrupt occurred; however, the XR error or check 2 are not set. 3. An XR error is forced with interrupts disabled, with XR errors and check 2 in the processor error register (PER). 4. Current or preceding interrupt levels are not correct.			
XB5027	1. A level 0 interrupt occurred; however, the current and preceding interrupt levels do not match. Current = 0 and previous = 7. 2. After returning from level 0, the PSR is not correct.			
XB5028	1. Processor problems. 2. A level 0 interrupt occurred and the XRA did not have the correct value in it. 3. The return from a level 0 interrupt did not occur or the level 0 interrupt occurred too soon. 4. The JAH register did not activate 'users active' when an error was forced on the data bus. (Address is correct.) 5. XR error interrupt did not occur. 6. Check reset is activated and check 2 and/or XR error did not reset. 7. The preceding interrupt level changed when the reset is given and XR error is not reset in the PER.			nnnnnn PSR = rr, PER = pp MTI = mm, DSE = ds RER = re, RSR = rs BCSE=bc, BDSE = bd WSE = ww, CER = ce A CAE = aa,B CAE= bb C CAE = cc,D CAE= dd nnnnnn Failure ID ** No errors were set rr Contents of the processor status register pp Contents of the processor error register mm Contents of the maintenance tag in register. ds Contents of the device status/error register. re Contents of the read error register rs Contents of the read status register bc Contents of the buffer channel status and error register bd Contents of the buffer device status and error register ww Contents of the write status/error register ce Contents of the channel error register aa Channel adapter A errors if CER bit 4 = 1 bb Channel adapter B errors if CER bit 5 = 1 cc Channel adapter C errors if CER bit 6 = 1 dd Channel adapter D errors if CER bit 7 = 1
XB5029	Both read and write operations are performed while forcing an addressing error on the XR address. The following failures can occur: • XR error or check 2 did not occur • PER XR errors were not set or reset correctly • IMR responded to an address with bad parity.			
XB502A	While testing to assure that A and B bus does not affect the processor bus, an XR or check 1 error occurred.			
XB502B	An XR address parity error was forced, but the MTI did not contain MTI FRU 1, indicating that the error was not detected.			

Tests 3, 4, and 5 Error Displays

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
XB502C	An error occurred while testing register zzzz.	To help in problem isolation, also run diagnostics EE10, EE30, EE40, EE50, EE60 EE90, and EEA0. 1. Remove the IML diskette, then press the IML switch to cause a power-on-reset. Run routine EE85 again. 2. If the value of ERA or ERB is other than 0, see the FSI section for error code E100. Also see action number 4 of this Additional Actions column. 3. If PSR bit 0 = 1, see EAD 1 for error code Fnnn. 4. If a diagnostic failure occurs and no errors are detected by the hardware, see the FSI section for error code E100 and perform the procedures for the microprocessor and control storage. 5. XR errors (PSR bit 0 = 1) can cause ERA and ERB errors. Use diagnostic EE85 to check the ERA and ERB registers.	FRU121 FRU118 FRU117 FRU115 FRU114 FRU120 FRU119 FRU116 FRU134 FRU135 FRU157 FRU158 FRU159 FRU139	nnnnnn REG = zzzz XRT = ff WR=yy, RD = aa ERA = ra, ERB = rb PSR = xx, EXP = xy PER = pp, EXP = py XRA = za, EXP = zy MTI = ti, EXP = ty MDI = di, EXP = dy MACHINE FAILURES MAY CAUSE CURRENT ERROR DATA TO BE INVALID. SEE DIAG 1 "VERIFY". (This screen is explained on DIAG 6.) nnnnnn Failure ID zzzz Mnemonic of the failing external register ff External register table at first error (program flags) yy Data written to the register aa Data read from the register ra Contents of error register A ** = No errors were set rb Contents of error register B xx Actual contents of the processor status register xy Expected contents of the processor status register pp Actual contents of the processor error register py Expected contents of the processor error register za Actual contents of the external register address register zy Expected contents of the external register address register ti Actual contents of the maintenance tag in register ty Expected contents of the maintenance tag in register di Actual contents of the users active register dy Expected contents of the users active register
XB502D	An error occurred while testing register zzzz.			
XB502E	A failure occurred while using an invalid address. An error is expected; see PSR, PER, and XRA registers. If the actual and expected values are the same for those registers, the error is indicated.			

Status Store Write/Read RAM Storage Test - Routine EE92

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine writes each of the sixteen offset bytes in the sixteen status store pages. The routine tests the status store RAM as follows:

1. It issues a command to write a status store page with a data pattern and increments the offset in the page until all sixteen offset bytes have been written.

2. It issues a command to read the page of storage that was just written. The read data and write data is then compared.

3. When all sixteen pages have been written, the data pattern is changed and steps 1 and 2 are repeated.

   Note: The default data patterns are Hex AA, 55, FF, and 00.

Routine Start Address: 2010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Pattern Entry Display

The data pattern written into status store can be altered by entering the pattern when the following screen displays.

```
DIAG=(EE92)-ENTER:
             PATTERN
              ttii
```

ttii Test data

Press the MD ENTER key to run the default data patterns.

or

Enter a pattern. Two bytes can be entered; the first byte (tt) must be FF to alert the routine that the default patterns are not being used. The second byte (ii) is the data pattern that will be written. Valid patterns are FF00-FFFF.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		
SS2021	A timeout occurred while trying to write in status store. No hardware errors were detected for this error.	See the FSI section for error code 53B2.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	SS2021 SS TIMEOUT OCCURRED DURING THE WRITE FOR PAGE x OFFSET y x = Status store page y = Offset of the storage location
SS2022	A timeout occurred while trying to read a location in status store. No hardware errors were detected for this error.	See the FSI section for error code 53B0.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	SS2022 SS TIMEOUT OCCURRED DURING THE READ FOR PAGE x OFFSET y x = Status store page y = Offset of the storage location
SS2023	The data read from the status store RAM did not match the data written. No hardware errors were detected for this error.	See the FSI section for error code 53B3.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	SS2023 DATA NOT AS EXPECTED PAGE x OFFSET y WRITE = zz READ = ww x = Status store page y = Offset of the storage location zz = Write data ww = Read data
SS2024	The status store write/read was completed successfully; however, a hardware error was detected. The registers that were checked for errors are displayed.	See the FSI section for error code 5900. If ERA and ERB are not 0, record the contents of ERA and ERB and see the FSI section for error code E100. If PSR bit 0 = 1, record the contents of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn. If CER bits 0, 1, 2, or 3 = 1, record the contents of CER. See the FSI section for error code 55nn.	FRU121 FRU122 FRU134	SS2024 ERROR: CER=cc PSR=rr PER=pp ERA=ra ERB=rb XRA=xx MTI=mm MDI=md cc = Contents of channel error register rr = Contents of the processor status register pp = Contents of the processor error register ra = Contents of error register A rb = Contents of error register B xx = Contents of the external register address register mm = Contents of the maintenance 'tag in' register md = Contents of the users active register

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		
SS2025	The data read from status store RAM did not match the data written. A hardware error was detected and the contents of the registers that were checked are displayed.	See the FSI section for error code 53B3. If ERA and ERB are not 0, record the contents of ERA and ERB and see the FSI section for error code E100. If PSR bit 0 = 1, record the contents of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn. If CER bits 0, 1, 2, or 3 = 1, record the contents of CER. See the FSI section for error code 55nn.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	SS2025 DATA NOT AS EXPECTED PAGE x OFFSET y WRITE = zz READ = ww HARDWARE REGISTERS ERROR: CER=cc PSR=rr PER=pp ERA=ra ERB=rb XRA=xx MTI=mm MDI=md x Status store page y Offset of the storage location zz Write data ww Read data cc Contents of the channel error register rr Contents of the processor status register pp Contents of the processor error register ra Contents of error register A rb Contents of error register B xx Contents of the external register address register mm Contents of the maintenance 'tag in' register md Contents of the user's active register
SS2026	A timeout occurred while trying to write in status store. A hardware error was detected and the contents of the registers that were checked are displayed on an additional error screen.	If ERA and ERB are not 0, record the contents of ERA and ERB and see the FSI section for error code E100. If PSR bit 0 = 1, record the contents of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn. If CER bits 0, 1, 2, or 3 = 1, record the contents of CER. See the FSI section for error code 55nn. See the FSI section for error code 53B2.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	SS2026 SS TIMEOUT OCCURRED DURING THE WRITE FOR PAGE x OFFSET y HARDWARE REGISTERS ERROR: CER=cc PSR=rr PER=pp ERA=ra ERB=rb XRA=xx MTI=mm MDI=md x Status store page y Offset of the storage location cc Contents of the channel error register rr Contents of the processor status register pp Contents of the processor error register ra Contents of error register A rb Contents of error register B xx Contents of the external register address register mm Contents of the maintenance 'tag in' register md Contents of the user's active register
SS2027	A timeout occurred while trying to read from status store. A hardware error was detected and the contents of the registers checked are displayed on an additional error screen.	If ERA and ERB are not 0, record the contents of ERA and ERB and see the FSI section for error code E100. If PSR bit 0 = 1, record the contents of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn. If CER bits 0, 1, 2, or 3 = 1, record the contents of CER. See the FSI section for error code 55nn. See the FSI section for error code 53B0.	FRU121 FRU122 FRU133 FRU152 FRU195 FRU196 FRU134	SS2027 SS TIMEOUT OCCURRED DURING THE READ FOR PAGE x OFFSET y HARDWARE REGISTERS ERROR: CER=cc PSR=rr PER=pp ERA=ra ERB=rb XRA=xx MTI=mm MDI=md x Status store page y Offset of the storage location cc Contents of the channel error register rr Contents of the processor status register pp Contents of the processor error register ra Contents of error register A rb Contents of error register B xx Contents of the external register address register mm Contents of the maintenance 'tag in' register md Contents of the user's active register

Status Store Order Test - Routine EE93

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine tests to see if the subsystem is in a dual control unit configuration. If it is, the routine issues a Reset Dual Control Unit Connection before starting the orders test. The orders test consists of the following:

1. The routine issues status store orders that are valid for a single control unit and tests a correct response from status store.

2. The routine tests to see if this is a dual control unit configuration, and if it is, the routine issues status store orders that are valid for a dual control unit and checks the response from status store.

   Note: Dual control unit order '4A' (Set Dual Controller Connect) is not issued by this routine.

Routine Start Address: 3010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			
SS3021	A timeout occurred while trying to determine the type of subsystem being tested; single or dual control unit.	See the FSI section for error code 5360.	FRU121 FRU117	SS3021 SS TIMEOUT OCCURRED WHILE TRYING TO READ FEATURE INFORMATION
SS3022	A timeout occurred while trying to get status store to disconnect from the second control unit before running the status store orders test.	See the FSI section for error code 5360.	FRU121 FRU117	SS3022 SS TIMEOUT OCCURRED WHILE DISCONNECTING THE 2ND CONTROL UNIT
SS3023	A timeout occurred while trying to issue a status store order for a single control unit status store. No hardware errors were detected for this error.	See the FSI section for error code 5310.	FRU121 FRU117	SS3023 A TIMEOUT OCCURRED FOR STATUS STORE ORDER = xx xx Status store order that was issued
SS3024	A timeout occurred while trying to issue a status store order for a dual control unit status store. No hardware errors were detected for this error.	See the FSI section for error code 5310.	FRU121 FRU117	SS3024 A TIMEOUT OCCURRED FOR STATUS STORE ORDER = xx xx Status store order that was issued
SS3025	The channel request register bit 5 was not reset as expected when issuing the Reset Message Buffer order. No hardware errors were detected for this error.	See the FSI section for error code 5311.	FRU121 FRU117	SS3025 THE RECEIVED BIT(5) NOT RESET FOR ORDER RESET READ MSG BUFF
SS3026	The response returned from status store when issuing a Read Message Buffer order indicates that the Reset Message Buffer order was not successful. No hardware errors were detected for this error.	See the FSI section for error code 5341.	FRU121 FRU117	SS3026 RESPONSE TO ACCESS READ MSG BUFF SHOWS RESET READ NOT GOOD
SS3027	The response returned from status store when issuing the acknowledge message indicated that the control units are still connected. No hardware errors were detected for this error.	See the FSI section for error code 5342.	FRU121 FRU117	SS3027 THE ACKNOWLEDGE MSG. RESPONSE INDICATES CU'S ARE CONNECTED

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see the EAD 1 for error code Fnnn.		
SS3028	The status store order completed successfully, but a hardware error was detected.	If ERA and ERB are not 0, record the contents of ERA and ERB and see the FSI section for error code E100. If PSR bit 0 = 1, record the contents of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn. If CER bits 0, 1, 2, or 3 = 1, record the contents of CER. See the FSI section for error code 55nn. See the FSI section for error code 5310.	FRU121 FRU117	SS3028 ERROR: CER=cc PSR=rr PER=pp ERA=ra ERB=rb XRA=xx MTI=mm MDI=md cc Contents of the channel error register rr Contents of the processor status register pp Contents of the processor error register ra Contents of error register A rb Contents of error register B xx Contents of the external register address register mm Contents of the maintenance 'tag in' register md Contents of the user's active register
SS3029	A timeout occurred while trying to issue a status store order for a single control unit status store. A hardware error was detected and the contents of the registers checked are displayed on an additional error screen.	If ERA and ERB are not 0, record the contents of ERA and ERB and see the FSI section for error code E100. If PSR bit 0 = 1, record the contents of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn. If CER bits 0, 1, 2, or 3 = 1, record the contents of CER. See the FSI section for error code 55nn. See the FSI section for error code 5310.	FRU121 FRU117 FRU122 FRU118 FRU115 FRU114 FRU120 FRU119 FRU116 FRU134 FRU135 FRU157 FRU158 FRU159 FRU139	SS3029 A TIMEOUT OCCURRED FOR STATUS STORE ORDER = yy HARDWARE REGISTERS ERROR: CER=cc PSR=rr PER=pp ERA=ra ERB=rb XRA=xx MTI=mm MDI=md yy Status store order issued cc Contents of the channel error register rr Contents of the processor status register pp Contents of the processor error register ra Contents of error register A rb Contents of error register B xx Contents of the external register address register mm Contents of the maintenance 'tag in' register md Contents of the user's active register
SS302A	A timeout occurred while trying to issue a status store order for a dual control unit status store. A hardware error was detected and the contents of the registers checked are displayed on an additional error screen.	If ERA and ERB are not 0, record the contents of ERA and ERB and see the FSI section for error code E100. If PSR bit 0 = 1, record the contents of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn. If CER bits 0, 1, 2, or 3 = 1, record the contents of CER. See the FSI section for error code 55nn. See the FSI section for error code 5310.	FRU121 FRU117	SS302A TIMEOUT OCCURRED FOR DUAL STATUS STORE ORDER = yy HARDWARE REGISTERS ERROR: CER=cc PSR=rr PER=pp ERA=ra ERB=rb XRA=xx MTI=mm MDI=md yy Status store order issued cc Contents of the channel error register rr Contents of the processor status register pp Contents of the processor error register ra Contents of error register A rb Contents of error register B xx Contents of the external register address register mm Contents of the maintenance 'tag in' register md Contents of the user's active register

Basic Tape Motion Test - Routine EEA2

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine contains two tests that exercise a single drive. The serial and parallel drive interconnections are used to verify correct operation of the Test I/O and Read Forward commands. There is no data transfer when the Read Forward command is tested.

Routine Start Address: 2010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Tests

Test 1

This test initializes the routine and checks for active level 3 through level 6 interrupts.

Test 2

This test checks to ensure that the correct drive address has been entered. Once the address has been verified as correct, a Sense command is issued to test correct execution of the command. Finally, Serial Test I/O and Serial Read commands are issued to test drive repositioning and drive interrupt operations.

Test Selection

The following screen displays after routine number EEA2 has been entered to invoke the tape motion diagnostic routine.

```
DIAG=(EEA2)-ENTER:
DRIVE          PATTERN
(xx)            ttii
```

xx Drive address
ttii Test data

To run the tests:

1. Insert a scratch tape that is not file protected.
2. Enter the drive address (valid parameters are 0-F, or 00-0F).
3. Use the ENTER key to move the cursor under PATTERN (ttii).
4. Enter the pattern. Valid parameters are 0200, or 0000. Entering 0200 causes tests 1 and 2 to loop until you press the PF key. Entering 0000 causes tests 1 and 2 to run one time.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

Error Analysis

Analyze errors for routine EEA2 as follows:

1. From the first error information screen record the key number, the drive address, and the serial and parallel commands.
2. Read the error message on the first error information screen and perform any action indicated.
3. Take the actual drive status (tttt) and the expected drive status (ssss) and convert them to binary. Example:

   8621 = 1000 0110 0010 0001

The bits are numbered 0-15, left to right. Compare the actual to expected drive status, and analyze bits that do not match.

Bit 0 This bit indicates that a serial command was issued since the last parallel command. This bit will only be on in the next status received by the control unit. If this is one of the error bits, see the FSI section for error code 9602.

Bit 1 This bit indicates that the drive is repositioning after a previous serial or parallel command. Repositioning can be indicated over either the serial or the parallel interconnections, and should always indicate the real-time operation of the drive, so both indicators should always indicate the same condition. If this is one of the error bits, see the FSI section for error code 8804.

Bit 2 This bit indicates the drive just changed from not ready to ready. This is usually a normal condition. If this is one of the error bits, see the FSI section for error code 33E8.

Bit 3 This bit indicates that the drive has moved a predetermined amount of tape and is notifying the control unit. This is usually a normal condition. This bit is not checked by routine EEA2.

Bit 4 This bit indicates that the drive just completed a disconnected command. If this is one of the error bits, replace FRU085*.

See EAD 1, "Drive Interconnections" for failure isolation.

Bit 5 This bit indicates that the drive just completed a connected command. If this is one of the error bits, replace FRU085*.

See EAD 1, "Drive Interconnections" for failure isolation.

Bit 6 This bit indicates the drive set drive unit check and sense data is present in the drive. Normally, the sense data is valid and is displayed in a later error information screen. Analyze this bit last.

See EAD 1, "Drive Interconnections" for failure isolation.

Bit 7 This bit indicates that the tape installed in the drive has been manually unloaded using the Rewind/Unload switch. If this is one of the error bits, see the FSI section for error code 8202.

Bit 8 This bit indicates that the drive address is one with an address in the range 8–F. If this is one of the error bits, see the FSI section for error code 86C0.

Bit 9 This bit indicates that the drive has completed a tape volume mount and is ready. If the drive is not really ready, you must make it ready. If this is one of the error bits, see the FSI section for error code 33E8.

Bit 10 This bit indicates that the drive has received patches from the control unit. Normally during this diagnostic, this bit is not active; however, if the functional microcode has previously sent patches and the drive has not been powered off or a reset has not been issued, this bit may be on. This bit is not checked.

Bit 11 This bit indicates that the drive is positioned at the beginning of tape. See EAD 1, "Drive Interconnections" for failure isolation.

Bit 12 This bit indicates that the drive tape volume is file protected. If this is one of the error bits, see the FSI section for error code CK07.

Bit 13 This bit indicates that the drive is positioned at or following the logical end of tape. If this is one of the error bits, replace FRU085*.

See EAD 1, "Drive Interconnections" for failure isolation.

Bit 14 This bit indicates that the drive is positioned at the physical end of tape. If this is one of the error bits, replace FRU085*.

See EAD 1, "Drive Interconnections" for failure isolation.

Bit 15 Reserved

* This FRU is EC sensitive. See CARR-DR 4.

Error Analysis (Continued'.

Analyze the errors for routine EEA2 as follows:

1. Record all information on the error screens.

2. If ERA and ERB are not 0, record the contents (if the screen is displayed) of ERA and ERB. See the FSI section for error code E100 and the following FRU list:

FRU	Name
117	Microprocessor card
115	Maintenance adapter card
114	Buffer control card
118	Drive-adapter card
121	Status store basic card
119	Read clock and format card
116	Write data card
120	Buffer adapter card
122	Status store communication card
134	Control store card
135	Control storage array card

3. If PSR bit 0 =1 , record the contents (if the screen is displayed) of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn and the following FRU list:

FRU	Name
118	Drive-adapter card
117	Microprocessor card
115	Maintenance adapter card
114	Buffer control card
121	Status store basic card
119	Read clock and format card
116	Write data card
120	Buffer adapter card
122	Status store communication card

4. If BCSE channel error groups 0-3 indicate any errors, record the contents of BCSE. See the FSI section for error code D5nn and the following FRU list:

FRU	Name
114	Buffer control card
120	Buffer adapter card
112	Buffer storage card (See note 2)
113	Buffer storage card (See note 2)
133	Channel adapter card (channel A)
136	Bus shoe card (channel A)
152	Channel adapter card (channel B)
233	Bus shoe card (channel C)
195	Channel adapter card (channel C)
235	Bus shoe card (channel C)
196	Channel adapter card (channel D)
237	Bus shoe card (channel D)
119	Read clock and format card
118	Drive-adapter card
116	Write data card
126	Power/POR card
134	Control store card
121	Status store basic card
122	Status store communication card

5. If BDSE channel error groups 0-3 indicate any errors, record the contents of BDSE. See the FSI section for error code D6nn and the following FRU list:

FRU	Name
114	Buffer control card
120	Buffer adapter card
112	Buffer storage card (See note 2)
113	Buffer storage card (See note 2)
111	Read ECC/CORR card
119	Read clock and format card
118	Drive-adapter card
116	Write data card
134	Control store card
117	Microprosessor card

6. If DSE bits 0, 1, or 2 = 1, record the contents of DCB, DCR, DSE, DIR, and DTR. See the FSI section for error code D4nn and the following FRU list:

FRU	Name
118	Drive-adapter card
116	Write data card
134	Control store card
085	Drive control card (See note 1)

7. If any RER bits = 1, or if RSR bits 5, 6, 7 = 1, record the contents of RCR, RRC, RER, RSR, and RDC. See the FSI section for error code D8nn and the following FRU list:

FRU	Name
064	Write power card
062	Read preamplifier card (See note 1)
085	Drive control card (See note 1)
132	Read detect card 3
131	Read detect card 2
130	Read detect card 1
123	Read skew buffer card 1
124	Read skew buffer card 2
125	Read skew buffer card 3
119	Read clock and format card
111	Read ECC/CORR card

8. If WSE bits 4, 5, or 6 = 1, record the contents of WCR and WSE. See the FSI section for error code D7nn and the following FRU list:

FRU	Name
116	Write data card
120	Buffer adapter card
114	Buffer control card
117	Microprocessor card
118	Drive-adapter card
139	Logic board A1

9. Record the contents of drive sense. See the last display screen under Error Displays for this routine for an explanation of the drive sense bytes.

Notes:

1. EC sensitive FRU, see CARR-DR 4.

2. EC sensitive FRU, see CARR-CU 7.

ERROR DISPLAYS FOR ROUTINE EEA2

```
nnnnnn
KEY = xxxx,DR = xx
CMD=SER-x,PARALL- yy
***Error messages***
```

* Data is not Valid
nnnnnn Failure ID
xxxx Sequence code for the error.
Sequence codes are:

0000 Initialization and active interrupt test.
0002 Issue an initial sense to assure that drive is in a known state.
0003 Assure that there are no pending drive alerts for the drive being tested.
0005 The drive is at end of tape (EOT). A rewind is issued to the drive.
0006 Issue a serial read forward command.
0008 During Key 0006 the drive is not repositioning, which indicates that the drive is accelerating towards 95 percent velocity in preparation for setting 'gap in'. Repeatedly issue a serial Test I/O command until the drive sets repositioning. Repositioning occurs when the drive reaches the 'gap in' point.
0009 During Key 0006 the drive is not repositioning. Key 0008 is completed with repositioning set. Assure that the drive does not set an alert.
0010 During Key 0006 the drive is not repositioning. Key 0008 is completed with repositioning set. Key 0009 is completed successfully. The drive should set an alert, which indicates that it is back in read forward stoplock.
0011 During Key 0006 the drive is not repositioning, which indicates that the drive is not at read forward stoplock but is moving towards read forward stoplock. The drive should set an alert when it reaches read forward stoplock.
0012 During Key 0006 the drive is not repositioning. Key 0011 either received an alert or timed out. Invoke a serial Test I/O command and check for errors.
0013 During Key 0006 the drive is not repositioning. Key 0011 either received an alert or timed out. Key 12 did not find any errors. Issue a serial Read Forward command, and if repositioning is not on, go to Key 0006.
0014 Key 10 has completed successfully. Perform parallel test I/O and check the drive status.

xx Drive address
x Last serial command issued
yy Last parallel command issued

ERROR MESSAGES:
MAKE THE DRIVE READY = Load the drive with a write enabled tape.
DR STS FILE PROT = The drive should be set to write enable (not file protect).

```
DRSTS=tttt,EXP=ssss
ERA=ra, ERB=rb
PSR=rr,PER=pp,XRA=aa
MTI=mm,MDI=md,
```

* No error is stored
tttt Actual drive status
ssss Expected drive status
ra Contents of error register A
rb Contents of error register B
rr Contents of the processor status register
pp Contents of the processor error register
aa Contents of the external register address register
mm Contents of the maintenance tag in register
md Contents of the user's active register

```
BCSE= abcde
BDSE= fghij,DCB= cb
DCR = dc,  DSE = ds
DIR = di   DTR = dt
```

* No error is set
a Buffer channel status and error register bits 0-3
b BCSE channel error group 0
c BCSE channel error group 1
d BCSE channel error group 2
e BCSE channel error group 3
f Buffer device status and error register bits 0-3
g BDSE device error group 0
h BDSE device error group 1
i BDSE device error group 2
j BDSE device error group 3
cb Contents of the device control bus register
dc Contents of the device control register
ds Contents of the device status/error register
di Contents of the device interrupt register
dt Contents of the device tag register

```
RCR = rc,  RRC = cr
RER = re,  RSR = rs
RDC = rd,
WCR = wc,  WSE = ws
```

* No error is set
rc Contents of the read control register
cr Contents of the read residual count register
re Contents of the read error register
rs Contents of the read status register
rd Contents of the read diagnostic control register
wc Contents of the write control register
ws Contents of the write status/error register

```
DRSNS-  S8=b0,S19=b1
S18= b2, S2021= b4b5
         S2223= b6b7
S30= 21,    EC= 2223
```

The following sense data is described in the SENSE section (see formats 19 and 20).

b0 Contents of the drive error recovery byte (see sense byte 8).
b1 The contents of the drive features byte (see sense byte 19).
b2 Flags modifier to b4b5 (see sense byte 18).
b4b5 The first error the drive detected. B4 contains the drive command associated with this error, an EE to indicate a bus out parity error while loading a command, or an FF to indicate that the error occurred when the drive was not performing a command. B5 contains the drive error code identifying this error (see sense bytes 20 and 21).
b6b7 The last error the drive detected. B6 contains the drive command associated with this error, an EE to indicate a bus out parity error while loading a command, or an FF to indicate that the error occurred when the drive was not performing a command. B7 contains the drive error code identifying this error (see sense bytes 22 and 23).
21 Logical drive address and physical drive address (contents of the thumbwheel switches). See sense byte 30.
2223 The drive EC level (contains the last four digits of the drive ROS module EC level).

Notes

Notes DIAG 503

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 502.
TM2021	LVL 3 INTRPT ACTIVE Level 3 interrupt is active following a reset.	See "Error Analysis" on DIAG 500. See the FSI section for error code 1103.	FRU119 FRU117	
TM2022	LVL 4 INTRPT ACTIVE Level 4 interrupt is active following a reset.	See "Error Analysis" on DIAG 500. See the FSI section for error code 1104.	FRU120 FRU117	
TM2023	LVL 5 INTRPT ACTIVE Level 5 interrupt is active following a reset.	See "Error Analysis" on DIAG 500. See the FSI section for error code 1105.	FRU120 FRU117	
TM2024	During execution of a drive diagnose command, an error occurred.	See "Error Analysis" on DIAG 500.		
TM2025	DR ADDR NOT VALID The drive address is not valid. Valid addresses are 0 through F. Re-enter the drive address from the test selection option screen.	See "Test Selection" on DIAG 500. See EAD 1, "Drive Interconnections."		
TM2026	SNS CMD TIMED OUT Sense time out. A Sense command issued to the drive did not complete.	See "Error Analysis" on DIAG 500. See EAD 1, "Drive Interconnections."		
TM2027	TIO CMD TIMED OUT Test I/O time out. A Test I/O command issued to the drive did not complete.	See "Error Analysis" on DIAG 500. See EAD 1, "Drive Interconnections."		
TM2028	SERIAL TIME OUT 8803 Serial time out. A serial command has been issued but the control unit did not complete the operation.	See "Error Analysis" on DIAG 500. See the FSI section for error code 8803. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118	
TM2029	DR REPO ERROR 8804 While preparing to issue a serial command, repositioning response was active. The error could be caused by the drive being tested, or another drive, or by an invalid response from the control unit.	See "Error Analysis" on DIAG 500. See the FSI section for error code 8804. See EAD 1, "Drive Interconnections."	FRU085[1] FRU118	
TM202A	DR ALERT ON Drive alert error. A Sense command has just completed successfully, which should have reset any alert present. However, a drive alert was detected.	See "Error Analysis" on DIAG 500. 1. Perform a Rewind/Unload operation on the drive. 2. Press POR on the drive. 3. Rerun routine EEA2. See EAD 1, "Drive Interconnections."	FRU085[1]	
TM202B	REW TO - NO ALERT Rewind timed out. Ending alert was not received from the drive.	See "Error Analysis" on DIAG 500. See EAD 1, "Drive Interconnections."	FRU085[1]	

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 502.
TM202C	REW ALERT TOO SOON The following sequence occurred: 1. A serial Read Forward command was issued with the drive at read forward stoplock. 2. Repositioning was checked to ensure it was set, which indicates that the drive was going back to read stoplock. 3. A drive alert was detected too soon.	See "Error Analysis" on DIAG 500. See EAD 1, "Drive Interconnections."	FRU085[1]	
TM202D	INVALID PATTERN RECD An invalid pattern was entered. Valid patterns are 0200 and 0000.	See "Test Selection" on DIAG 500, and enter 0000 to run the test once or 0200 to loop the test continuously.		
TM202E	REW SELECT TIMED OUT Rewind command time out. A Rewind command issued to the drive did not complete.	See "Error Analysis" on DIAG 500. See the FSI section for error codes 89nn and 8Fnn.	FRU085[1] FRU199 FRU248 FRU118 FRU116 FRU134	
TM202F	RDF DR S/B STOPPED Serial Read Forward command is issued. The drive should be at read stoplock and repositioning should be off. Repositioning is still on.	See "Error Analysis" on DIAG 500.	FRU085[1]	
TM2030	SER RD, NO SEL, NOREPO The following sequence occurred: 1. A serial Read Forward command was issued with the drive at read forward stoplock. 2. Repositioning was not set after sufficient time for the drive to have reached 95 percent velocity.	See "Error Analysis" on DIAG 500.	FRU085[1]	
TM2031	REW CMD NOT ACCEPTED The internal status for a Rewind command was not correct, which indicates that the drive did not accept the command.	See "Error Analysis" on DIAG 500.		
TM2032	An external register error occurred during the operation.	See "Error Analysis" on DIAG 500. See steps 1 and 2 at the top of this chart.		
TM2033	A control unit Check 1 error occurred.	See "Error Analysis" on DIAG 500. See steps 1 and 2 at the top of this chart.		
TM2034	Either the BCSE or BDSE register contains an error. Buffer status is not checked for incorrect bits.	See "Error Analysis" on DIAG 500.		
TM2035	Errors are set in the write, read, or drive error registers.	See "Error Analysis" on DIAG 500.		
TM2036	The BCSE or BDSE registers did not contain the correct status.	See "Error Analysis" on DIAG 500.		

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAY
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 502.
TM2037	The WSE register did not contain the correct status.	See "Error Analysis" on DIAG 500. See the FSI section for error code D7nn.	FRU116 FRU118 FRU120 FRU114 FRU139	
TM2038	A drive Check 1 error occurred during the last I/O operation.	See "Error Analysis" on DIAG 500. See the DCB for nn bits and see the FSI section for error code 8Fnn.	FRU085[1] FRU118 FRU116 FRU134 FRU199 FRU248	
TM2039	The drive status is incorrect excluding drive unit check.	See "Error Analysis" on DIAG 500.		
TM203A	The drive sense contains an error that is unrecoverable.	See "Error Analysis" on DIAG 500.		
TM203B	NO ALERT READ A Serial Read command was issued to the drive and no alert occurred after repositioning.	See "Error Analysis" on DIAG 500. See EAD 1, "Drive Interconnections."	FRU085[1]	
TM203C	DIAGNOSE CMD TIMED OUT A diagnose command issued to the drive did not complete.	See "Error Analysis" on DIAG 500. See EAD 1, "Drive Interconnections."		
TM203D	After an error, as part of an error recovery routine, the control unit issued a 'Serial Reset A' command followed by a 'Set Diagnose', which causes a midtape load. During this recovery routine, an error occurred.	See "Error Analysis" on DIAG 500.		
TM203E	After an error, as part of an error recovery routine, the control unit issued a 'Serial Reset A' command followed by a 'Set Diagnose', which causes a midtape load. When the routine had not completed after three minutes, a timeout occurred.	See "Error Analysis" on DIAG 500.		
TM203F	The DLR external register and drive sense do not agree. Model (A11 and B22) or (A22 and B11).	See CARR-CU 1189 for correct DLR external register switch setting.	FRU118	

[1] This FRU is EC sensitive. See CARR-DR 4.

Basic Tape Motion Test-Routine EEA2 (Continued)

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUs	ERROR DISPLAYS
TM2040 TM2041	A timeout error occurred during a TIO command to the drive. A drive status error occurred while sending code to the drive.	1. This program has minimum diagnostic capability during the drive patching procedure. 2. This error occurs when a cartridge loader is installed and a cartridge is present in the drive to be tested. 3. This error can be bypassed by loading the functional code into the control unit and setting the control unit on-line. Press unload switch of the drive to be tested, reload diagnostic EE54 and run it. To avoid channel interference set all the channel enable/disable switches to disable. 4. If this error persists, run "Start Repair" on the product diskette.		See the "Error Displays" on DIAG 502.
TM2042 TM2043 TM2044	The correct level of code patches is not found on the IML diskette. The correct level of code patches is not found on the IML diskette. Unable to read the IML diskette due to an error.	1. Make sure the diskette in the diskette reader is the correct level. 2. This error occurs when a cartridge loader is installed and a cartridge is present in the drive to be tested. 3. This error can be bypassed by loading the functional code into the control unit and setting the control unit on-line. Press unload switch of the drive to be tested, reload diagnostic EE54 and run it. To avoid channel interference set all the channel enable/disable switches to disable. Ensure that the control unit successfully loads code from the diskette. 4. If this error persists, run "Start Repair" on the product diskette.		

Write/Read Exerciser - Routine EEA3

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine verifies that the write, read backward, and read operations of the drive operate correctly. Routine EEA3 tests are performed at the beginning-of-tape (BOT).

This test checks the drive's data flow and buffer with the following sequence of operations:

1. Checks for interrupts that are on all of the time.
2. Ensures that a single drive address is entered.
3. Sends a sense command to reset any unit checks or sense data.
4. Sends a rewind command to start the test at BOT.
5. Writes and reads 16 blocks of varying length data.

Routine Start Address: 3010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Test Selection

The following screen displays after routine number EEA3 has been entered to start the tape motion diagnostic routine.

```
DIAG=(EEA3)-ENTER:
DRIVE
(xx)
```

Valid parameters:

xx Drive address (0-F, or 00-0F).

To run the tests:

1. Insert a write enabled scratch cartridge in the drive and make it ready.
2. Enter the drive address.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

The format of the display's first line is the same for all detected errors. The remaining three lines contain additional information about the failure.

External registers are defined in the DF (Data Fields) section of this maintenance information.

Note: If the diagnostic is not permitted to complete normally, (for example, if the program function or enter key is used to stop the diagnostic) you must wait until the drive motion has stopped before restarting the diagnostic or an error will occur.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

Error Analysis

Analyze the errors for routine EEA3 as follows:

1. From the first error information screen record the key number, the drive address, and the drive status.
2. Read the error message on the first error information screen and perform any action indicated.
3. Take the actual drive status (tttt) and the expected drive status (ssss) and convert them to binary. Example:

   8621 = 1000 0110 0010 0001

   The bits are numbered 0-15, left to right. Compare the actual to expected drive status, and analyze bits that do not match.

   Bit 0 This bit indicates that a Serial command was issued since the last parallel command. This bit will only be on in the next status received by the control unit. If this is one of the error bits, see FSI section for error code 9602.

   Bit 1 This bit indicates that the drive is repositioning after a previous Serial or Parallel command. Repositioning can be indicated over either the serial or the parallel interconnections and should always indicate the real-time operation of the drive, so both indicators should always indicate the same condition. If this is one of the error bits, see FSI section for error code 8804.

   Bit 2 This bit indicates the drive just changed from Not Ready to Ready. This is usually a normal condition. If this is one of the error bits, see FSI section for error code 33E8.

   Bit 3 This bit indicates that the drive has moved a predetermined amount of tape and is notifying the control unit. This is usually a normal condition. This bit is not checked by routine EEA3.

   Bit 4 This bit indicates that the drive just completed a Disconnected command. If this is one of the error bits, replace FRU085*.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 5 This bit indicates that the drive just completed a Connected command. If this is one of the error bits, replace FRU085*.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 6 This bit indicates the drive set drive unit check and sense data is present in the drive. Normally, the sense data is valid and is displayed in a later error information screen. Analyze this bit last.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 7 This bit indicates that the tape loaded in the drive has been manually unloaded using the Rewind/Unload switch. If this is one of the error bits, see FSI section for error code 8202.

   Bit 8 This bit indicates that the drive address is one with an address in the range of 8 F. If this is one of the error bits, see FSI section for error code 86C0.

   Bit 9 This bit indicates that the drive has completed a tape volume mount and is ready. If this is one of the error bits, see FSI section for error code 33E8.

   Bit 10 This bit indicates that the drive has received patches from the control unit. Normally during this diagnostic, this bit is not active; however, if the functional microcode has previously sent patches and the drive has not been powered off or reset has not been issued, this bit may be on. This bit is not checked.

   Bit 11 This bit indicates the drive is positioned at the beginning of tape. See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 12 This bit indicates that the drive tape volume is file protected. If this is one of the error bits, see FSI section for error code CK07.

   Bit 13 This bit indicates that the drive is positioned at or following the logical end of tape. If this is one of the error bits, replace FRU085*.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 14 This bit indicates that the drive is positioned at the physical end of tape. If this is one of the error bits, replace FRU085*.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 15 Reserved

Error Analysis (Continued'.

Analyze the errors for routine EEA3 as follows:

4. Record all information on the error screens.

5. If ERA and ERB are not 0, record the contents (if the screen is displayed) of ERA and ERB. See the FSI section for error code E100 and the following FRU list:

FRU	Name
117	Microprocessor card
115	Maintenance adapter card
114	Buffer control card
118	Drive adapter card
121	Status store basic card
119	Read clock and format card
116	Write data card
120	Buffer adapter card
122	Status store communication card
134	Control store card
135	Control storage array card

6. If PSR bit 0 =1 , record the contents (if the screen is displayed) of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn and the following FRU list:

FRU	Name
118	Drive adapter card
117	Microprocessor card
115	Maintenance adapter card
114	Buffer control card
121	Status store basic card
119	Read clock and format card
116	Write data card
120	Buffer adapter card
122	Status store communication card

7. If BCSE channel error groups 0-3 indicate any errors, record the contents of BCSE. See the FSI section for error code D5nn and the following FRU list:

FRU	Name
114	Buffer control card
120	Buffer adapter card
112	Buffer storage card (See note 2)
113	Buffer storage card (See note 2)
133	Channel adapter card (channel A)
136	Bus shoe card (channel A)
152	Channel adapter card (channel B)
233	Bus shoe card (channel C)
195	Channel adapter card (channel C)
235	Bus shoe card (channel C)
196	Channel adapter card (channel D)
237	Bus shoe card (channel D)
119	Read clock and format card
118	Drive adapter card
116	Write data card
126	Power/POR card
134	Control store card
121	Status store basic card
122	Status store communication card

8. If BDSE channel error groups 0-3 indicate any errors, record the contents of BDSE. See the FSI section for error code D6nn and the following FRU list:

FRU	Name
114	Buffer control card
120	Buffer adapter card
112	Buffer storage card (See note 2)
113	Buffer storage card (See note 2)
111	Read ECC/CORR card
119	Read clock and format card
118	Drive adapter card
116	Write data card
134	Control store card
117	Microprosessor card

9. If DSE bits 0, 1, or 2 = 1, record the contents of DCB, DCR, DSE, DIR, and DTR. See the FSI section for error code D4nn and the following FRU list:

FRU	Name
118	Drive adapter card
116	Write data card
134	Control store card
085	Drive control card (See note 1)

10. If any RER bits = 1, or if RSR bits 5, 6, 7 = 1, record the contents of RCR, RRC, RER, RSR, and RDC. See the FSI section for error code D8nn and the following FRU list:

FRU	Name
064	Write power card
062	Read preamplifier card (See note 1)
085	Drive control card (See note 1)
132	Read detect card 3
131	Read detect card 2
130	Read detect card 1
123	Read skew buffer card 1
124	Read skew buffer card 2
125	Read skew buffer card 3
119	Read clock and format card
111	Read ECC/CORR card

11. If WSE bits 4, 5, or 6 = 1, record the contents of WCR and WSE. See the FSI section for error code D7nn and the following FRU list:

FRU	Name
116	Write data card
120	Buffer adapter card
114	Buffer control card
117	Microprocessor card
118	Drive adapter card
139	Logic board A1

12. Record the contents of drive sense. See the last display screen under Error Displays for this routine for an explanation of the drive sense bytes.

Notes:

1. EC sensitive FRU, see CARR-DR 4.

2. EC sensitive FRU, see CARR-CU 7.

Error Counts

The "BLKS CORR EEA3 EEA4" screen contains a count of the number of blocks written or read forward (fwd) or backward (bkd) upon which ECC correction was performed. It is normal for some error counts to occur. You must use the following information, and any past experience with this machine type, to determine if the error count is normal, or if a problem exists.

Total blocks written are hex '20B'
Total blocks read fwd are hex '200'
Total blocks read bkd are hex '200'

"Correctable errors" are errors that are corrected while processing data between the control unit and the drive. No error recovery actions are required. These errors are sometimes called ECC errors.

A correctable "write" error would be a single track in either or both of the two groups (fwd and bkd). The error is detected in the control unit detection logic as the data from the read head is processed during the writing process. The data itself is not actually corrected because it is not used except for the read-back check.

A correctable "read" error would be a single or double track error in either or both of the two groups (fwd and bkd). The data is corrected as it is processed through the detection and deskewing logic. CRC checking is performed on the corrected data.

Because this diagnostic does not retry errors, it is possible for a worn or bad place on the media to cause write or readback check errors. If this is the cause of an error, do one or more of the following:

- Use another drive (same cartridge)
- Use another cartridge (same drive)
- Run diagnostic routine EEA4 to see if the error occurs at the opposite end of the tape.
- If available, use another control unit.

ERROR DISPLAYS FOR ROUTINE EEA3

```
nnnnnn
KEY = kk   DR = xx
DRSTS=tttt,EXP=ssss
***Error messages***
```

* Data is not valid
nnnnnn Failure ID
kk Key that error occurred in.

Key codes are:

00 Set up write buffer

01 Ensure that a single drive address is entered

02 The microcode performs the following:
1. Generates a sense command to the drive to clear any units checks or sense data.
2. Generates a sense command to the drive to check for any errors.
3. Generates a parallel test I/O command.

03 Send command to drive to set display language.

04 Sends a rewind command to the drive to start the test at beginning-of-tape (BOT).

05 The microcode sets up the control tables.

06 Executes the following block sequence queues (BSQ):

BSQ Number	Description
01	Write a density and a tapemark
02	Write an erase gap
03	Write a tapemark
04	Write an erase gap
05	Write a density mark and a one-byte block
07	In a one drive selection, write an erase gap, tapemark, one-byte block, a 53-byte block, tapemark and a 140-byte block.
0D-1C	Write 16 blocks, varying in length from one-byte to 65536 bytes, then stop and repeat writing the same 16 blocks fifteen more times for a total of 256 blocks. All data blocks are written with ripple data, hex 00-FF. The blocks sizes are:

Block ID	Byte Size	Block ID	Byte Size
0000 0001	1	0000 000A	4906
0000 0002	53	0000 000B	32768
0000 0003	54	0000 000C	5607
0000 0004	140	0000 000D	7009
0000 0005	2102	0000 000E	7710
0000 0006	16384	0000 000F	9813
0000 0007	2803	0000 0010	65536
0000 0008	3504	0000 EEEE	Tapemark
0000 0009	4205	0000 AAAA	Erasegap

During the write operation, the drive buffer, and the write and read data flow are checked to ensure that no errors are detected.

20-4F Write one block, then read backward for two blocks and then read forward two blocks, and repeat for 255 times, using the same block size sequence shown above.

11 Sends rewind command to drive.
tttt Actual drive status.
ssss Expected drive status.

ERROR MESSAGES:
MAKE THE DRIVE READY = Load the drive with a write enabled tape.
DR STS FILE PROT = The drive should be set to write enable.

```
ERA=ra     ERB=rb
PSR=xx,    PER=pp
MTI=mm     MDI=md
XRA=aa
```

This screen is displayed only if a check 1 or an XR error occurs.

* No errors are set
aa Contents of the external register
md Contents of the maintenance data in register
mm Contents of the maintenance tag in register
pp Contents of the processor error register
ra Contents of error register A
rb Contents of error register B
xx Contents of the processor status register

```
SCMD=xxx    PCMD=yyy
 BSQ=qq     DTR=dr
WRITE ID=wwwwwwww
R/RBC ID=rrrrrrrr
```

* Data is not valid
dr Contents of the device tag register
qq For BSQ number, see the Key Code 06 (BSQ descriptions) under the first error display on this page.
rrrrrrrr Block ID of the block currently being read or read back checked.
wwwwwwww Block ID of the block currently being written.
xxx Last serial command
yyy Last parallel command sent

```
BLKS CORR EEA3 EEA4
WRITE   =  bb   ee
READ FWD=  cc   ff
READ BKD=  dd   gg
```

* Data is not valid
bb Write ECC errors counted during the EEA3 test
cc Read forward ECC errors counted during the EEA3 test
dd Read backward ECC errors counted during the EEA3 test
ee Write ECC errors counted during the EEA4 test
ff Read forward ECC errors counted during the EEA4 test
gg Read backward ECC errors counted during the EEA4 test

```
BCSE= abcde  DSE= ds
BDSE= fghij  RCR= rc
WCR = wc     RSR= rs
WSE = ws     RER= re
```

* No errors are set
a Buffer channel status and error register bits 0-3
b BCSE channel error group 0
c BCSE channel error group 1
d BCSE channel error group 2
e BCSE channel error group 3
f Buffer device status and error register bits 0-3
g BDSE device error group 0
h BDSE device error group 1
i BDSE device error group 2
j BDSE device error group 3
ds Contents of the device status error register
rc Contents of the read control register
re Contents of the read error register
rs Contents of the read status register
wc Contents of the write control register
ws Contents of the write status error register

```
DRSNS-  S8=b0,S19=b1
S18= b2, S2021= b4b5
         S2223= b6b7
S30= 21,    EC= 2223
```

The following sense data is described in the SENSE section (see formats 19 and 20).

b0 Contents of the drive error recovery byte (see sense byte 8).
b1 The contents of the drive features byte (see sense byte 19).
b2 Flags modifier to b4b5 (see sense byte 18).
b4b5 The first error the drive detected. B4 contains the drive command associated with this error; an EE indicates a bus out parity error occurred while loading a command, or an FF indicates that the error occurred when the drive was not performing a command. B5 contains the drive error code identifying this error (see sense bytes 20 and 21).
b6b7 The last error the drive detected. B6 contains the drive command associated with this error; an EE indicates a bus out parity error occurred while loading a command, or an FF indicates that the error occurred when the drive was not performing a command. B7 contains the drive error code identifying this error (see sense bytes 22 and 23).
21 Logical drive address and physical drive address (contents of the thumbwheel switches). See sense byte 30.
2223 The drive EC level (contains the last four digits of the drive ROS module EC level).

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM3021	LVL 0 INTRPT ACTIVE Level 0 interrupt was active following a reset.	See "Error Analysis" on DIAG 510. See the FSI section for error code 1100.	FRU119 FRU117	
TM3022	LVL 3 INTRPT ACTIVE Level 3 interrupt was active following a reset.	See "Error Analysis" on DIAG 510. See the FSI section for error code 1103.	FRU120 FRU117	
TM3023	LVL 4 INTRPT ACTIVE Level 4 interrupt was active following a reset.	See "Error Analysis" on DIAG 510. See the FSI section for error code 1104.	FRU120 FRU117	
TM3024	LVL 5 INTRPT ACTIVE Level 5 interrupt was active following a reset.	See "Error Analysis" on DIAG 510. See the FSI section for error code 1105.	FRU120 FRU117	
TM3025	DR ADDR NOT VALID The drive address is not valid. Valid addresses are 0 through F.	Enter the drive address from the test selection option screen, again. See "Test Selection" on DIAG 510.		
TM3026	UNIT CK ON SNS CMD Unit Check (UC) was on in the initial status from the Sense command. A UC is acceptable only in the first Sense command, but was still on in the second Sense command.	See "Error Analysis" on DIAG 510.	FRU120 FRU117	
TM3027	SNS CMD TIMED OUT A Sense command timed out. A Sense command issued to the drive did not complete.	See "Error Analysis" on DIAG 510.		
TM3028	TIO CMD TIMED OUT A Test I/O command timed out. A Test I/O command issued to the drive did not complete, and timed out after approximately 33 milliseconds on the device data bus.	See "Error Analysis" on DIAG 510.		
TM3029	SERIAL TIME OUT 8803 A Serial command timed out. A serial command has been issued but the control unit did not complete the operation on the device data bus.	See "Error Analysis" on DIAG 510. See the FSI section for error code 8803.	FRU085[1] FRU118	
TM302A	DR REPO ERROR 8804 While preparing to issue a serial command, repositioning response was active. This error could be caused by the drive being tested, by another drive, or by an invalid response from the control unit on the device data bus.	See "Error Analysis" on DIAG 510. See the FSI section for error code 8804.	FRU085[1] FRU118	
TM302B	REW TO - NO ALERT A Rewind command timed out. Ending alert was not received from the drive.	See "Error Analysis" on DIAG 510.	FRU085[1]	

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM302C	REW SELECT TIMED OUT A Rewind command timed out. A Rewind command issued to the drive did not complete.	See "Error Analysis" on DIAG 510. See the FSI section for error codes 89nn and 8Fnn.	FRU085[1] FRU118 FRU116 FRU134 FRU199 FRU248	
TM302D	REW CMD NOT ACCEPTED The initial status for a Rewind command issued to the drive was not correct, which indicates that the drive did not accept the command.	See "Error Analysis" on DIAG 510.		
TM302E	An external register error occurred during the operation.	See "Error Analysis" on DIAG 510. See steps 1 and 2 at the top of this chart.		
TM302F	A control unit check 1 error occurred.	See "Error Analysis" on DIAG 510. See steps 1 and 2 at the top of this chart.		
TM3030	Either the BCSE or BDSE register contains an error. Buffer status is not checked for incorrect bits.	See "Error Analysis" on DIAG 510.		
TM3031	Errors are set in the write, read, or drive error registers.	See "Error Analysis" on DIAG 510.		
TM3032	The BCSE or BDSE registers did not contain the correct status.	See "Error Analysis" on DIAG 510.		
TM3033	The WSE register did not contain the correct status.	See "Error Analysis" on DIAG 510. See the FSI section for error code D7nn.	FRU116 FRU118 FRU120 FRU114 FRU139	
TM3034	A drive Check 1 error occurred during the last I/O operation.	See "Error Analysis" on DIAG 510. See the DCB for nn bits and see the FSI section for error code 8Fnn.	FRU085[1] FRU118 FRU116 FRU134 FRU199 FRU248	
TM3035	The drive status is incorrect.	See "Error Analysis" on DIAG 510.		
TM3036	The drive sense contains an error that is unrecoverable.	See "Error Analysis" on DIAG 510.		
TM3037	NO ALERT A serial command was issued to the drive, and no alert occurred after repositioning.	See "Error Analysis" on DIAG 510.	FRU085[1]	
TM3038	This is a microcode program error.	Call your next level of support.		
TM3039	This is a microcode program error.	Call your next level of support.		

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 512.
TM303A	This is a microcode program error.	Call your next level of support.		
TM303B	This is a microcode program error.	Call your next level of support.		
TM303C	An error occurred while writing the buffer to initialized the channel buffer storage.	See "Error Analysis" on DIAG 510. See the FSI section for error code A141.	FRU120 FRU114	
TM303D	A buffer error occurred while writing the write operation data into the buffer. The BCSE register value should be X'20'.	See "Error Analysis" on DIAG 510.		
TM303E	A buffer error was detected while writing this record.	See "Error Analysis" on DIAG 510. See the FSI section for error code 70E4.	FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU116	
TM303F	'Device xfer complete' (BDSE register) did not set.	See "Error Analysis" on DIAG 510. See the FSI section for error code 70E6.	FRU085[1] FRU062[1] FRU064 FRU116 FRU118 FRU114 FRU120	
TM3040	A write data flow error was detected while writing this record. Error bits were on in the WSE register, or 'end write' did not set in the maximum allowable time.	See "Error Analysis" on DIAG 510. See the FSI section for error code 70E5.		
TM3041	A write sequence error occurred. This is a microcode program error.	Call your next level of support.		
TM3042	A write sequence error occurred. This is a microcode program error.	Call your next level of support.		
TM3043	A time out occurred waiting for the 'status in' response to 'gap out' on the device data bus.	See "Error Analysis" on DIAG 510. See the FSI section for error code 70E3.	FRU085[1] FRU118	
TM3044	A drive check 1 occurred.	See "Error Analysis" on DIAG 510. See the FSI section for error code 89nn.	FRU085[1] FRU199 FRU248 FRU118 FRU116 FRU134	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM3045	A time out occurred waiting for the device data bus 'status in' line to come active.	See "Error Analysis" on DIAG 510. See the FSI section for error code 8C03.	FRU085[1] FRU118 FRU116 FRU134	
TM3046	The hardware detected a device adapter error.	See "Error Analysis" on DIAG 510. See the FSI section for error code 8Bnn.	FRU085[1] FRU118 FRU116 FRU134	
TM3047	Drive sense data contains an error, and while ending the tag sequence to the drive, device data bus 'status in' did not drop.	See "Error Analysis" on DIAG 510. See the FSI section for error code 8C07.	FRU085[1] FRU118 FRU116 FRU134	
TM3048	A pattern sequence table error occurred during the read back check. The read data flow detected an IBG that was not expected.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7061.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3049	This is a microcode program error.	Call your next level of support.		
TM304A	IBG was not detected after 'gap in' on the device data bus.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7093.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 512.
TM304B	A device buffer overrun occurred once while writing the same record.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7181.	FRU114 FRU120 FRU117	
TM304C	256 ERGs were read without detecting a Block or TM.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7702.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM304D	A read error occurred on the last record.	See "Error Analysis" on DIAG 510. See the FSI section for error code 76nn.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU120 FRU114 FRU111	
TM304E	A timeout occurred waiting for the device data bus 'status in' response to device data bus 'gap out'.	See "Error Analysis" on DIAG 510.	FRU085[1] FRU118	
TM304F	During a read back check, a level 3 interrupt occurred that was caused by 'end sync'.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7503.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM3050	A read back check error occurred on the last record.	See "Error Analysis" on DIAG 510. See the FSI section for error code 74nn.	FRU064 FRU062[1] FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU111 FRU114 FRU120 FRU264 FRU265	
TM3051	The value of bits 0 and 1 of the RRC register do not match the value of bits 6 and 7 (word 1) of the LDT table.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7501.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	
TM3052	A timeout occurred while waiting for device data bus 'status in' in response to device data bus 'gap out'.	See "Error Analysis" on DIAG 510. See the FSI section, error code 7502.	FRU085[1] FRU118	
TM3053	Device data bus 'gap out' did not occur for the last block of data read.	See "Error Analysis" on DIAG 510. See the FSI section, error code 7502.	FRU085[1] FRU118	
TM3054	After a Read ID operation, an error was indicated in the BDSE register.	See "Error Analysis" on DIAG 510. See the FSI section, error code 70C1.	FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU116	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM3055	A block ID format error occurred. Bits 0 and 8-11 of the four-byte block ID are always zero. The block just read from the tape contains a block ID with at least one of these bits on.	See "Error Analysis" on DIAG 510. See the FSI section for error code 70C4.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3056	A block ID error occurred on a Read Forward operation. The block just read from the tape does not have the expected block ID sequence number.	See "Error Analysis" on DIAG 510. See the FSI section for error code 70C2.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3057	A block ID error occurred on a Read Backward operation. The block just read from the tape does not have the expected block ID sequence number.	See "Error Analysis" on DIAG 510. See the FSI section for error code 70C3.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3058	The expected buffer CRC data did not compare to the actual data read from the buffer. This could be the wrong block read. No hardware errors were detected.	See "Error Analysis" on DIAG 510.		
TM3059	The expected buffer CRC data did not compare to the actual data read from the buffer. This could be the wrong block read. No hardware errors were detected.	See "Error Analysis" on DIAG 510.		

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 512.
TM305A	A level 0 interrupt occurred that was caused by an external register error.	See "Error Analysis" on DIAG 510. See steps 1 and 2 at the top of this chart. See the FSI section for error code 7061.		
TM305B	A level 0 interrupt occurred that was not caused by an external register error or 'collision detect'.	See "Error Analysis" on DIAG 510. See the FSI section for error code 1100.	FRU119 FRU117	
TM305C	A level 0 interrupt occurred that was caused by 'collision detect'.	See "Error Analysis" on DIAG 510. FRUs are to be changed in both control units. See the FSI section for error code 1100.	FRU117 FRU121 FRU122 FRU134	
TM305D	A time out occurred waiting for 'beg sync' during a read back check operation.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7071.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM305E	A write data flow error was detected while writing this record. FRU bits were on in WSE register, or 'end write' did not set in the maximum allowable time (50 microseconds).	See "Error Analysis" on DIAG 510. See the FSI section for error code 7076.	FRU085[1] FRU062[1] FRU064 FRU116 FRU118 FRU114 FRU120	
TM305F	The BDSE register detected an buffer error while writing this record.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7077.	FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU116	
TM3060	'Device xfer complete' (BDSE register) was not on, at the end of a Buffer to WDF Transfer operation.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7078.	FRU120 FRU114	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM3061	A pattern sequence table error occurred during a read back check operation.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7074.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3062	'Gap in' and 'generate gap out' (RSR register) were on, causing a level 3 interrupt to occur.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7081.	FRU118 FRU119 FRU176 FRU116	
TM3063	A device buffer overrun condition occurred once while writing the same record.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7081.	FRU114 FRU120 FRU117	
TM3064	A device buffer overrun condition occurred while reading a record operation.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7173.	FRU114 FRU120	
TM3065	'Density separator' was not detected before 45 sets of samples were taken.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7161.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3066	A pattern sequence table error occurred during a read back check operation. The read data flow detected a tapemark (TM) that was not expected.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7041.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM3067	A tapemark (TM) was read during read back check that did not meet the minimum length specifications.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7042.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3068	The write control register (WCR) did not set at the correct time.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7192.	FRU064 FRU116 FRU063[1] FRU118	
TM3069	This is a microcode program error.	Call your next level of support.		
TM306A	The read back check started incorrectly. It came up when reading the IBG, and did not find the block before the first IBG.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7051. See the FSI section for error code D0nn. See the FSI section for error code D8nn.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM306B	The read back check started incorrectly and timed out waiting for the IBG preceding the first block written.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7052.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM306C	The IBG read during the read back check was too short.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7151.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM306D	The IBG read during the read back check was too long.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7152.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM306E	A read back check occurred waiting for the IBG.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7159.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM306F	VOID was detected during a read operation. A valid block, TM, or ERG was not detected within 67 milliseconds after 'gap in'.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7153.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	
TM3070	A data transfer timeout was detected during a read operation. No valid IBG was read within 67 milliseconds after 'beg sync'.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7154.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3071	A data transfer timeout was detected during a RBC operation. No valid IBG was read within 67 milliseconds after 'beg sync'.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7155.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 512.
TM3072	A read back check of a tapemark determined that the tapemark's length was too long.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7156.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3073	No beginning of block or tapemark was detected in the maximum allowed time during a read operation.	See "Error Analysis" on DIAG 510. See the FSI section error code 7154.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3074	A Write Erase Gap operation was not ended by a buffer interrupt.	See "Error Analysis" on DIAG 510. See the FSI section for error code 715A.	FRU114 FRU120	
TM3075	A write data flow error occurred.	See "Error Analysis" on DIAG 510.		
TM3076	A valid density pattern was not read after five retries.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7141.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2] FRU264 FRU265	
TM3077	A timeout occurred waiting for 'write end' when writing a write density separator.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7144.	FRU116	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 512.
TM3078	A timeout occurred waiting for the density separator.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7142.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM3079	A timeout occurred while waiting for the IBG after the density separator.	See "Error Analysis" on DIAG 510. See the FSI section for error code 7143.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM307A	This is a microcode program error.	See "Error Analysis" on DIAG 510. See the FSI section for error code 9600.		
TM307B	A timeout occurred waiting for 'gap in' from the drive.	See "Error Analysis" on DIAG 510. See the FSI section for error code 9601.	FRU085[1] FRU118 FRU117 FRU134 FRU115	
TM307C	A time out occurred while waiting for the drive to be selected on a read or write command.	See "Error Analysis" on DIAG 510. See the FSI section for error code 8005. See the FSI section for error code 8007. See the FSI section for error code 8009.	FRU085[1] FRU199 FRU248 FRU118 FRU059 FRU049 FRU108 FRU107 FRU105	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 512.
TM307D	This is a microcode program error.	Call your next level of support.		
TM307E	This is a microcode program error.	Call your next level of support.		
TM307F	This is a microcode program error.	Call your next level of support.		
TM3080	Set Diagnose command was sent to the drive and did not complete correctly.	See "Error Analysis" on DIAG 510.	FRU0851 FRU199	
TM3081	A Set Diagnose command, sent to the drive, did not complete.	See "Error Analysis" on DIAG 510. See the FSI section for error code 8005. See the FSI section for error code 8007. See the FSI section for error code 8009.	FRU0851 FRU199 FRU248 FRU118 FRU059 FRU049 FRU108 FRU107 FRU105	
TM3082	Test EEA3 has completed, and there are one or more errors in the counters. The counters are displayed on the screen with the following first line: BLKS CORR EEA3 EEA4. (See ERROR DISPLAYS on DIAG 512.)	1. See "Error Counts" on DIAG 510. 2. a. Test another drive using the same cartridge. b. Test the the same 2 drives using another cartridge. c. Test both drives using both cartridges. d. Run the test using the other CU (if present). 3. Clean the read/write head. See CARR-DR 1-1, for FRU013. 4. Use the product diskette and run the "unit test" option, looking for a high number of temporary errors.	DR FRU0621 FRU064 FRU0631 FRU0851 FRU216 FRU059 FRU013 CU FRU132 FRU131 FRU130 FRU125 FRU124 FRU123 FRU119 FRU111 FRU199 FRU248 FRU264 FRU265	
TM3083	The DLR external register and drive sense do not agree. Model (A11 and B22) or (A22 and B11).	See CARR-CU 1189 for correct DLR external register switch setting.	FRU118	

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUs	ERROR DISPLAYS
TM3084 TM3085	A timeout error occurred during a TIO command to the drive. A drive status error occurred while sending code to the drive.	1. This program has minimum diagnostic capability during the drive patching procedure. 2. This error occurs when a cartridge loader is installed and a cartridge is present in the drive to be tested. 3. This error can be bypassed by loading the functional code into the control unit and setting the control unit on-line. Press unload switch of the drive to be tested, reload diagnostic EE54 and run it. To avoid channel interference set all the channel enable/disable switches to disable. 4. If this error persists, run "Start Repair" on the product diskette.		See the "Error Displays" on DIAG 512.
TM3086 TM3087 TM3088	The correct level of code patches is not found on the IML diskette. The correct level of code patches is not found on the IML diskette. Unable to read the IML diskette due to an error.	1. Make sure the diskette in the diskette reader is the correct level. 2. This error occurs when a cartridge loader is installed and a cartridge is present in the drive to be tested. 3. This error can be bypassed by loading the functional code into the control unit and setting the control unit on-line. Press unload switch of the drive to be tested, reload diagnostic EE54 and run it. To avoid channel interference set all the channel enable/disable switches to disable. Ensure that the control unit successfully loads code from the diskette. 4. If this error persists, run "Start Repair" on the product diskette.		

Write/Read Exerciser - Routine EEA4

Prerequisite diagnostics must run without failure before this diagnostic is run. See DIAG 3, "PREREQUISITE DIAGNOSTICS."

This routine verifies that the write, read backward, and read operations of the drive operate correctly. Routine EEA4 tests are performed at the end of tape (EOT).

This test checks the drive's data flow and buffer with the following sequence of operations:

1. Checks for interrupts that are on all of the time.
2. Ensures that a single drive address is entered.
3. Sends a sense command to reset any units checks or sense data.
4. Sends DSE and Locate commands to start the test at EOT.
5. Writes and reads 16 blocks of data varying in length from 1 byte to 65 536 bytes. This is repeated fifteen times for a total of 256 blocks. All data blocks are written using a ripple data pattern of X'00 ' to X'FF'.

Routine Start Address: 6010

Error Loop: If no error occurs, the routine loops as if "LOOP ROUTINE" is set. When an error is detected, the routine saves the error information and displays the error on the MD. After the error is displayed, the routine continues to loop on that error. However, if a different error occurs, that new error is displayed on the MD, and the routine will loop on the new error.

Test Selection

The following screen displays after routine number EEA4 has been entered to start the tape motion diagnostic routine.

```
DIAG=(EEA4)-ENTER:
DRIVE
(xx)
```

Valid parameters:

xx Drive address (0-F, or 00-0F).

To run the tests:

1. Insert a write enabled scratch cartridge in the drive and make it ready.
2. Enter the drive address.

Error Displays

When an error is detected by the diagnostic program, the maintenance device displays error information on its keyboard/display. The first screen displays automatically. You can see the second and following screens by pressing the ENTER key on the keyboard/display.

External registers are defined in the DF (Data Fields) section of this maintenance information.

Note: If the diagnostic is not permitted to complete normally, you must wait until drive motion has stopped before restarting the diagnostic, or an error will occur.

FRUS

See CARR-CU or CARR-DR, pages 1-1, 1-2, 1-3, and 1-4 for the names and locations of the FRUs.

Error Analysis

Analyze the errors for routine EEA4 as follows:

1. From the first error information screen record the key number, the drive address, and drive status.
2. Read the error message on the first error information screen and perform any action indicated.
3. Take the actual drive status (tttt) and the expected drive status (ssss) and convert them to binary. Example:

   8621 = 1000 0110 0010 0001

   The bits are numbered 0-15, left to right. Compare the actual to expected drive status, and analyze bits that do not match.

   Bit 0 This bit indicates that a Serial command was issued since the last parallel command. This bit will only be on in the next status received by the control unit. If this is one of the error bits, see the FSI section for error code 9602.

   Bit 1 This bit indicates that the drive is repositioning after a previous Serial or Parallel command. Repositioning can be indicated over either the serial or the parallel interconnections, and should always indicate the real-time operation of the drive, so both indicators should always indicate the same condition. If this is one of the error bits, see the FSI section for error code 8804.

   Bit 2 This bit indicates the drive just changed from Not Ready to Ready. This is usually a normal condition. If this is one of the error bits, see the FSI section for error code 33E8.

   Bit 3 This bit indicates that the drive has moved a predetermined amount of tape and is notifying the control unit. This is usually a normal condition. This bit is not checked by routine EEA4.

   Bit 4 This bit indicates that the drive just completed a Disconnected command. If this is one of the error bits, replace FRU085*.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 5 This bit indicates that the drive just completed a Connected command. If this is one of the error bits, replace FRU085*.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 6 This bit indicates the drive set drive unit check and sense data is present in the drive. Normally, the sense data is valid and is displayed in a later error information screen. Analyze this bit last. See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 7 This bit indicates that the tape loaded in the drive has been manually unloaded using the Rewind/Unload switch. If this is one of the error bits, see the FSI section for error code 8202.

   Bit 8 This bit indicates that the drive address is one with an address in the range of 8-F. If this is one of the error bits, see the FSI section for error code 86C0.

   Bit 9 This bit indicates that the drive has completed a tape volume mount and is ready. If this is one of the error bits, see the FSI section for error code 33E8.

   Bit 10 This bit indicates that the drive has received patches from the control unit. Normally during this diagnostic, this bit is not active; however, if the functional microcode has previously sent patches and the drive has not been powered off or reset has not been issued, this bit may be on. This bit is not checked.

   Bit 11 This bit indicates the drive is positioned at the beginning of tape. See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 12 This bit indicates that the drive tape volume is file protected. If this is one of the error bits, see the FSI section for error code CK07.

   Bit 13 This bit indicates that the drive is positioned at or following the logical end of tape. If this is one of the error bits, replace FRU085*.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 14 This bit indicates that the drive is positioned at the physical end of tape. If this is one of the error bits, replace FRU085*.

   See EAD 1, "Drive Interconnections" for failure isolation.

   Bit 15 Reserved

Note:

IBM Enhanced Capacity Cartridge System tapes should not be mounted in a 3480 subsystem. Only the 3490E has the design updates needed to support the use of the enhanced capacity cartridge. Tape that exceeds the length of the IBM Cartridge System Tape could cause damage to either the tape or the drive.

Analyze the errors for routine EEA4 as follows:

4. Record all information on the error screens.

5. If ERA and ERB are not 0, record the contents (if the screen is displayed) of ERA and ERB. See the FSI section for error code E100 and the following FRU list:

FRU	Name
117	Microprocessor card
115	Maintenance adapter card
114	Buffer control card
118	Drive adapter card
121	Status store basic card
119	Read clock and format card
116	Write data card
120	Buffer adapter card
122	Status store communication card
134	Control store card
135	Control storage array card

6. If PSR bit 0 =1 , record the contents (if the screen is displayed) of PSR, PER, XRA, MTI, and MDI. See EAD 1 for error code Fnnn and the following FRU list:

FRU	Name
118	Drive adapter card
117	Microprocessor card
115	Maintenance adapter card
114	Buffer control card
121	Status store basic card
119	Read clock and format card
116	Write data card
120	Buffer adapter card
122	Status store communication card

7. If BCSE channel error groups 0-3 indicate any errors, record the contents of BCSE. See the FSI section for error code D5nn and the following FRU list:

FRU	Name
114	Buffer control card
120	Buffer adapter card
112	Buffer storage card (See note 2)
113	Buffer storage card (See note 2)
133	Channel adapter card (channel A)
136	Bus shoe card (channel A)
152	Channel adapter card (channel B)
233	Bus shoe card (channel C)
195	Channel adapter card (channel C)
235	Bus shoe card (channel C)
196	Channel adapter card (channel D)
237	Bus shoe card (channel D)
119	Read clock and format card
118	Drive adapter card
116	Write data card
126	Power/POR card
134	Control store card
121	Status store basic card
122	Status store communication card

8. If BDSE channel error groups 0-3 indicate any errors, record the contents of BDSE. See the FSI section for error code D6nn and the following FRU list:

FRU	Name
114	Buffer control card
120	Buffer adapter card
112	Buffer storage card (See note 2)
113	Buffer storage card (See note 2)
111	Read ECC/CORR card
119	Read clock and format card
118	Drive adapter card
116	Write data card
134	Control store card
117	Microprosessor card

9. If DSE bits 0, 1, or 2 = 1, record the contents of DCB, DCR, DSE, DIR, and DTR. See the FSI section for error code D4nn and the following FRU list:

FRU	Name
118	Drive adapter card
116	Write data card
134	Control store card
085	Drive control card (See note 1)

10. If any RER bits = 1, or if RSR bits 5, 6, 7 = 1, record the contents of RCR, RRC, RER, RSR, and RDC. See the FSI section for error code D8nn and the following FRU list:

FRU	Name
064	Write power card
062	Read preamplifier card (See note 1)
085	Drive control card (See note 1)
132	Read detect card 3
131	Read detect card 2
130	Read detect card 1
123	Read skew buffer card 1
124	Read skew buffer card 2
125	Read skew buffer card 3
119	Read clock and format card
111	Read ECC/CORR card

11. If WSE bits 4, 5, or 6 = 1, record the contents of WCR and WSE. See the FSI section for error code D7nn and the following FRU list:

FRU	Name
116	Write data card
120	Buffer adapter card
114	Buffer control card
117	Microprocessor card
118	Drive adapter card
139	Logic board A1

12. Record the contents of drive sense. See the last display screen under Error Displays for this routine for an explanation of the drive sense bytes.

Notes:

1. EC sensitive FRU, see CARR-DR 4.

2. EC sensitive FRU, see CARR-CU 7.

Error Counts

The "BLKS CORR EEA3 EEA4" screen contains a count of the number of blocks written or read forward (fwd) or backward (bkd) upon which ECC correction was performed. It is normal for some error counts to occur. You must use the following information, and any past experience with this machine type, to determine if the error count is normal, or if a problem exists.

Total blocks written are hex '20B'
Total blocks read fwd are hex '200'
Total blocks read bkd are hex '200'

"Correctable errors" are errors that are corrected while processing data between the control unit and the drive. No error recovery actions are required. These errors are sometimes called ECC errors.

A correctable "write" error would be a single track in either or both of the two groups (fwd and bkd). The error is detected in the control unit detection logic as the data from the read head is processed during the writing process. The data itself is not actually corrected because it is not used except for the read-back check.

A correctable "read" error would be a single or double track error in either or both of the two groups (fwd and bkd). The data is corrected as it is processed through the detection and deskewing logic. CRC checking is performed on the corrected data.

Because this diagnostic does not retry errors, it is possible for a worn or bad place on the media to cause write or readback check errors. If this is the cause of an error, do one or more of the following:

- Use another drive (same cartridge)
- Use another cartridge (same drive)
- Run diagnostic routine EEA4 to see if the error occurs at the opposite end of the tape.
- If available, use another control unit.

ERROR DISPLAYS FOR ROUTINE EEA4

```
nnnnnn
KEY = kk   DR = xx
DRSTS=tttt,EXP=ssss
***Error messages***
```

* Data is not valid
nnnnnn Failure ID
kk Key that error occurred in.
Key codes are:
00 Set up write buffer
01 Ensure that a single drive address is entered
02 The microcode performs the following:
1. Generates a sense command to the drive to clear any units checks or sense data.
2. Generates a sense command to the drive to check for any errors.
3. Generates a parallel test I/O command.
03 Send command to drive to set display language.
04 Sends a rewind command to the drive to start the test at beginning-of-tape (BOT).
05 The microcode sets up the control tables.
06 Executes the following block sequence queues (BSQ):

BSQ Number	Description
01	Write a density and a tapemark
02	Write an erase gap
03	Write a tapemark
04	Write an erase gap
05	Write a density mark and a one-byte block
07	In a one drive selection, write an erase gap, tapemark, one-byte block, a 53-byte block, tapemark and a 140-byte block.
0D-1C	Write 16 blocks, varying in length from one-byte to 65536 bytes, then stop and repeat writing the same 16 blocks fifteen more times for a total of 256 blocks. All data blocks are written with ripple data, hex 00-FF. The blocks sizes are:

Block ID	Byte Size	Block ID	Byte Size
0000 0001	1	0000 000A	4906
0000 0002	53	0000 000B	32768
0000 0003	54	0000 000C	5607
0000 0004	140	0000 000D	7009
0000 0005	2102	0000 000E	7710
0000 0006	16384	0000 000F	9813
0000 0007	2803	0000 0010	65536
0000 0008	3504	0000 EEEE	Tapemark
0000 0009	4205	0000 AAAA	Erasegap

During the write operation, the drive buffer, and the write and read data flow are checked to ensure that no errors are detected.
20-4F Write one block, then read backward for two blocks and then read forward two blocks, and repeat for 255 times, using the same block size sequence shown above.
11 Sends rewind command to drive.
tttt Actual drive status.
ssss Expected drive status.

ERROR MESSAGES:
MAKE THE DRIVE READY = Load the drive with a write enabled tape.
DR STS FILE PROT = The drive should be set to write enable.

```
ERA=ra     ERB=rb
PSR=xx,    PER=pp
MTI=mm     MDI=md
XRA=aa
```

This screen is displayed only if a check 1 or an XR error occurs.

* No errors are set
aa Contents of the external register
md Contents of the maintenance data in register
mm Contents of the maintenance tag in register
pp Contents of the processor error register
ra Contents of error register A
rb Contents of error register B
xx Contents of the processor status register

```
SCMD=xxx   PCMD=yyy
 BSQ=qq    DTR=dr
WRITE ID=wwwwwwww
R/RBC ID=rrrrrrrr
```

* Data is not valid
dr Contents of the device tag register
qq For BSQ number, see the Key Code 06 (BSQ descriptions) under the first error display on this page.
rrrrrrrr Block ID of the block currently being read or read back checked.
wwwwwwww Block ID of the block currently being written.
xxx Last serial command
yyy Last parallel command sent

```
BLKS CORR EEA3 EEA4
WRITE   =  bb   ee
READ FWD=  cc   ff
READ BKD=  dd   gg
```

* Data is not valid
bb Write ECC errors counted during the EEA3 test
cc Read forward ECC errors counted during the EEA3 test
dd Read backward ECC errors counted during the EEA3 test
ee Write ECC errors counted during the EEA4 test
ff Read forward ECC errors counted during the EEA4 test
gg Read backward ECC errors counted during the EEA4 test

```
BCSE= abcde  DSE= ds
BDSE= fghij  RCR= rc
WCR = wc     RSR= rs
WSE = ws     RER= re
```

* No errors are set
a Buffer channel status and error register bits 0-3
b BCSE channel error group 0
c BCSE channel error group 1
d BCSE channel error group 2
e BCSE channel error group 3
f Buffer device status and error register bits 0-3
g BDSE device error group 0
h BDSE device error group 1
i BDSE device error group 2
j BDSE device error group 3
ds Contents of the device status error register
rc Contents of the read control register
re Contents of the read error register
rs Contents of the read status register
wc Contents of the write control register
ws Contents of the write status error register

```
DRSNS-  S8=b0,S19=b1
S18= b2, S2021= b4b5
         S2223= b6b7
S30= 21,    EC= 2223
```

The following sense data is described in the SENSE section (see formats 19 and 20).
b0 Contents of the drive error recovery byte (see sense byte 8).
b1 The contents of the drive features byte (see sense byte 19).
b2 Flags modifier to b4b5 (see sense byte 18).
b4b5 The first error the drive detected. B4 contains the drive command associated with this error; an EE indicates a bus out parity error occurred while loading a command, or an FF indicates that the error occurred when the drive was not performing a command. B5 contains the drive error code identifying this error (see sense bytes 20 and 21).
b6b7 The last error the drive detected. B6 contains the drive command associated with this error; an EE indicates a bus out parity error occurred while loading a command, or an FF indicates that the error occurred when the drive was not performing a command. B7 contains the drive error code identifying this error (see sense bytes 22 and 23).
21 Logical drive address and physical drive address (contents of the thumbwheel switches). See sense byte 30.
2223 The drive EC level (contains the last four digits of the drive ROS module EC level).

Failure ID	Description	Additional Actions	FRUS
TM6021	**LVL 0 INTRPT ACTIVE** Level 0 interrupt was active following a reset.	See "Error Analysis" on DIAG 550 See the FSI section for error code 1100.	FRU119 FRU117
TM6022	**LVL 3 INTRPT ACTIVE** Level 3 interrupt was active following a reset.	See "Error Analysis" on DIAG 550 See the FSI section for error code 1103.	FRU120 FRU117
TM6023	**LVL 4 INTRPT ACTIVE** Level 4 interrupt was active following a reset.	See "Error Analysis" on DIAG 550 See the FSI section for error code 1104.	FRU120 FRU117
TM6024	**LVL 5 INTRPT ACTIVE** Level 5 interrupt was active following a reset.	See "Error Analysis" on DIAG 550 See the FSI section for error code 1105.	FRU120 FRU117
TM6025	**DR ADDR NOT VALID** The Drive Address is not valid. Valid addresses are 0 through F.	Enter the drive address from the test selection option screen, again. See "Test Selection" on DIAG 550	
TM6026	**UNIT CK ON SNS CMD** Unit check (UC) was on in the initial status from the Sense command. A UC is acceptable only in the first Sens command, but was still on in the second Sense command.	See "Error Analysis" on DIAG 550	FRU120 FRU117
TM6027	**SNS CMD TIMED OUT** A Sense command timed out. A Sense command issued to the drive did not complete.	See "Error Analysis" on DIAG 550 **Note:** This error can be caused by Enhanced Capacity Cartridges. IBM Enhanced Capacity Cartridge System tapes should not be mounted in a 3480 subsystem.	
TM6028	**TIO CMD TIMED OUT** A Test I/O command timed out. A Test I/O command issued to the drive on the device data bus did not complete, and timed out after approximately 33 milliseconds.	See "Error Analysis" on DIAG 550	
TM6029	**SERIAL TIME OUT 8803** A Serial command timed out. A Serial command has been issued but the control unit did not complete the operation on the device data bus.	See "Error Analysis" on DIAG 550 See the FSI section for error code 8803.	FRU085* FRU118
TM602A	**DR REPO ERROR 8804** While preparing to issue a Serial command, repositioning response was active. This error could be caused by the drive being tested, another drive, or by an invalid response from the control unit on the device data bus.	See "Error Analysis" on DIAG 550 See the FSI section for error code 8804.	FRU085* FRU118
TM602B	**DSE SELECT TIMED OUT** A DSE command timed out. A DSE command issued to the drive did not complete.	See "Error Analysis" on DIAG 550 See the FSI section for error code 8005. See the FSI section for error code 8007. See the FSI section for error code 8009.	FRU085* FRU199 FRU248 FRU118 FRU059 FRU049 FRU108 FRU107 FRU105

* This FRU is EC Sensitive. See CARR-DR4.

Follow steps 1 and 2 before taking any other actions

1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100.
2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.

Error Displays:

See the "Error Displays" on DIAG 552.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM602C	DSE COMMAND NOT ACCEPTED The initial status for a DSE command issued to the drive was not correct, which indicates that the drive did not accept the command.	See "Error Analysis" on DIAG 550. See the FSI section for error code 89nn. See the FSI section for error code 8Fnn.	FRU085[1] FRU118 FRU116 FRU134 FRU199 FRU248	
TM602D	DSE TO - NO ALERT A DSE command timed out. Ending alert was not received from the drive.	See "Error Analysis" on DIAG 550. See the FSI section for error code 89nn. See the FSI section for error code 8Fnn.	FRU085[1] FRU118 FRU116 FRU134 FRU199 FRU248	
TM602E	LOCATE SELECT TIMED OUT A Locate command timed out. A Locate command issued to the drive did not complete.	See "Error Analysis" on DIAG 550. See the FSI section for error code 89nn. See the FSI section for error code 8Fnn.	FRU085[1] FRU199 FRU248 FRU118 FRU116 FRU134	
TM602F	LOC COMMAND NOT ACCEPTED The initial status for a LOC command issued to the drive was not correct, which indicates that the drive did not accept the command.	See "Error Analysis" on DIAG 550.		
TM6030	LOC TO - NO ALERT A LOC command timed out. Ending alert was not received from the drive.	See "Error Analysis" on DIAG 550. See the FSI section for error code 89nn. See the FSI section for error code 8Fnn.	FRU085[1] FRU118 FRU116 FRU134 FRU199 FRU248	
TM6031	An external register error occurred during the operation.	See "Error Analysis" on DIAG 550. See steps 1 and 2 at the top of this chart.		
TM6032	A control unit check 1 error occurred.	See "Error Analysis" on DIAG 550. See steps 1 and 2 at the top of this chart.		
TM6033	Either the BCSE or BDSE register contains an error. Buffer status is not checked for incorrect bits.	See "Error Analysis" on DIAG 550.		
TM6034	Errors are set in the write, read, or drive error registers.	See "Error Analysis" on DIAG 550.		

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM6035	The BCSE or BDSE registers did not contain the correct status.	See "Error Analysis" on DIAG 550.		
TM6036	The WSE register did not contain the correct status.	See "Error Analysis" on DIAG 550. See the FSI section for error code D7nn.	FRU116 FRU118 FRU120 FRU114 FRU139	
TM6037	A drive Check 1 error occurred during the last I/O operation.	See "Error Analysis" on DIAG 550. See the DCB for nn bits and see the FSI section for error code 8Fnn.	FRU085[1] FRU118 FRU116 FRU134 FRU199 FRU248	
TM6038	The drive status is incorrect.	See "Error Analysis" on DIAG 550.		
TM6039	The drive sense contains an error that is unrecoverable.	See "Error Analysis" on DIAG 550.		
TM603A	NO ALERT A serial command was issued to the drive, and no alert occurred after repositioning.	See "Error Analysis" on DIAG 550.	FRU085[1]	
TM603B	This is a microcode program error.	Call your next level of support.		
TM603C	This is a microcode program error.	Call your next level of support.		
TM603D	This is a microcode program error.	Call your next level of support.		
TM603E	This is a microcode program error.	Call your next level of support.		
TM603F	An error occurred while writing to the buffer to initialize the channel buffer storage.	See "Error Analysis" on DIAG 550. See the FSI section for error code A141.	FRU120 FRU114	
TM6040	A buffer error occurred while writing the write operation data into the buffer. The BCSE register value should be X'20'.	See "Error Analysis" on DIAG 550.		
TM6041	A buffer error was detected while writing this record.	See "Error Analysis" on DIAG 550. See the FSI section for error code 70E4.	FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU116	
TM6042	'Device xfer complete' (BDSE register) did not set.	See "Error Analysis" on DIAG 550. See the FSI section for error code 70E6.	FRU085[1] FRU062[1] FRU064 FRU116 FRU118 FRU114 FRU120	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 552.
TM6043	A write data flow error was detected while writing this record. Error bits were on in the WSE register, or 'end write' did not set in the maximum allowable time.	See "Error Analysis" on DIAG 550. See the FSI section for error code 70E5.		
TM6044	A write sequence error occurred. This is a microcode program error.	Call your next level of support.		
TM6045	A write sequence error occurred. This is a microcode program error.	Call your next level of support.		
TM6046	A time out occurred waiting for the 'status in' response to 'gap out'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 70E3.	FRU085[1] FRU118	
TM6047	A drive check 1 occurred.	See "Error Analysis" on DIAG 550. See the FSI section for error code 89nn.	FRU085[1] FRU199 FRU248 FRU118 FRU116 FRU134	
TM6048	A time out occurred waiting for the device data bus 'status in' line to become active.	See "Error Analysis" on DIAG 550. See the FSI section for error code 8C03.	FRU085[1] FRU118 FRU116 FRU134	
TM6049	The hardware detected a device adapter error.	See "Error Analysis" on DIAG 550. See the FSI section for error code 8Bnn.	FRU085[1] FRU118 FRU116 FRU134	
TM604A	Drive sense data contains an error, and while ending the tag sequence to the drive, device data bus 'status in' did not drop.	See "Error Analysis" on DIAG 550. See the FSI section for error code 8C07.	FRU085[1] FRU118 FRU116 FRU134	

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM604B	A pattern sequence table error occurred during the read back check. The read data flow detected an IBG that was not expected.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7061.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM604C	This is a microcode program error.	Call your next level of support.		
TM604D	IBG was not detected after device data bus 'gap in'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7093.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	
TM604E	A device buffer overrun occurred once while writing the same record.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7181.	FRU114 FRU120 FRU117	
TM604F	256 ERGs were read without detecting a Block or TM.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7702.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM6050	A read error occurred on the last record.	See "Error Analysis" on DIAG 550. See the FSI section for error code 76nn.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU120 FRU114 FRU111	
TM6051	A timeout occurred waiting for the device data bus 'status in' response to 'gap out'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7701.	FRU085[1] FRU118	
TM6052	During a read back check, a level 3 interrupt occurred that was caused by 'end sync'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7503.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	
TM6053	A read back check error occurred on the last record.	See "Error Analysis" on DIAG 550. See the FSI section for error code 74nn.	FRU064 FRU062[1] FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU111 FRU114 FRU120 FRU264 FRU265	

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM6054	The value of bits 0 and 1 of the RRC register do not match the value of bits 6 and 7 (word 1) of the LDT table.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7501.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	
TM6055	A timeout occurred while waiting for the device data bus 'status in' response to 'gap out'.	See "Error Analysis" on DIAG 550. See the FSI section, error code 7502.	FRU085[1] FRU118	
TM6056	Device data bus 'gap out' did not occur for the last block of data read.	See "Error Analysis" on DIAG 550. See the FSI section, error code 7502.	FRU085[1] FRU118	
TM6057	After a Read ID operation, an error was indicated in the BDSE register.	See "Error Analysis" on DIAG 550. See the FSI section, error code 70C1.	FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU116	
TM6058	A block ID format error occurred. Bits 0 and 8-11 of the four-byte block ID are always zero. The block just read from the tape contains a block ID with at least one of these bits on.	See "Error Analysis" on DIAG 550. See the FSI section for error code 70C4.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM6059	A block ID error occurred on a Read Forward operation. The block just read from the tape does not have the expected block ID sequence number.	See "Error Analysis" on DIAG 550. See the FSI section for error code 70C2.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM605A	A block ID error occurred on a Read Backward operation. The block just read from the tape does not have the expected block ID sequence number.	See "Error Analysis" on DIAG 550. See the FSI section for error code 70C3.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM605B	The expected buffer CRC data did not compare to the actual data read from the buffer. This could be the wrong block read. No hardware errors were detected.	See "Error Analysis" on DIAG 550.		
TM605C	The expected buffer CRC data did not compare to the actual data read from the buffer. This could be the wrong block read. No hardware errors were detected.	See "Error Analysis" on DIAG 550.		
TM605D	A level 0 interrupt occurred that was caused by an external register error.	See "Error Analysis" on DIAG 550. See steps 1 and 2 at the top of this chart. See the FSI section for error code 7061.		
TM605E	A level 0 interrupt occurred that was not caused by an external register error or 'collision detect'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 1100.	FRU119 FRU117	
TM605F	A level 0 interrupt occurred that was caused by 'collision detect'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 1100.	FRU119 FRU117	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM6060	A time out occurred waiting for 'beg sync' during a read back check operation.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7071.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM6061	A write data flow error was detected while writing this record. FRU bits were on in WSE register, or 'end write' did not set in the maximum allowable time (50 microseconds).	See "Error Analysis" on DIAG 550. See the FSI section for error code 7076.	FRU085[1] FRU062[1] FRU064 FRU116 FRU118 FRU114 FRU120	
TM6062	The BDSE register detected an buffer error while writing this record.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7077.	FRU114 FRU120 FRU112[2] FRU113[2] FRU111 FRU116	
TM6063	'Device xfer complete' (BDSE register) was not on, at the end of a Buffer to WDF Transfer operation.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7078.	FRU120 FRU114	
TM6064	A pattern sequence table error occurred during a read back check operation.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7074.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM6065	'Gap in' and 'generate gap out' (RSR register) were on, causing a level 3 interrupt to occur.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7081.	FRU118 FRU119 FRU176 FRU116	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM6066	A device buffer overrun condition occurred once while writing the same record.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7081.	FRU114 FRU120 FRU117	
TM6067	A device buffer overrun condition occurred while reading a record operation.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7173.	FRU114 FRU120	
TM6068	'Density separator' was not detected before 45 sets of samples were taken.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7161.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM6069	A pattern sequence table error occurred during a read back check operation. The read data flow detected a tapemark (TM) that was not expected.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7041.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM606A	A tapemark (TM) was read during read back check that did not meet the minimum length specifications.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7042.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM606B	The write control register (WCR) did not set at the correct time.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7192.	FRU064 FRU116 FRU063[1] FRU118	
TM606C	This is a microcode program error.	Call your next level of support.		
TM606D	The read back check started incorrectly. It came up when reading the IBG, and did not find the block before the first IBG.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7051. See the FSI section for error code D0nn. See the FSI section for error code D8nn.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM606E	The read back check started incorrectly and timed out waiting for the IBG preceding the first block written.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7052.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM606F	The IBG read during the read back check was too short.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7151.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM6070	The IBG read during the read back check was too long.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7152.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM6071	A read back check occurred waiting for the IBG.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7159.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	
TM6072	VOID was detected during a read operation. A valid block, TM, or ERG was not detected within 67 milliseconds after 'gap in'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7153.	FRU064 FRU062[1] FRU085[1] FRU130 FRU116 FRU216 FRU059 FRU117 FRU131 FRU132 FRU118 FRU119 FRU063[1] FRU058 FRU013	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM6073	A data transfer timeout was detected during a read operation. No valid IBG was read within 67 milliseconds after 'beg sync'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7154.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM6074	A data transfer timeout was detected during a RBC operation. No valid IBG was read within 67 milliseconds after 'beg sync'.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7155.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	
TM6075	A read back check of a tapemark determined that the tapemark's length was too long.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7156.	FRU062[1] FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU112[2] FRU113[2]	

[1] This FRU is EC sensitive. See CARR-DR 4.

[2] This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 552.
TM6076	No beginning of block or tapemark was detected in the maximum allowed time during a read operation.	See "Error Analysis" on DIAG 550. See the FSI section error code 7154.	FRU0621 FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU1122 FRU1132	
TM6077	A Write Erase Gap operation was not ended by a buffer interrupt.	See "Error Analysis" on DIAG 550. See the FSI section for error code 715A.	FRU114 FRU120	
TM6078	A write data flow error occurred.	See "Error Analysis" on DIAG 550.		
TM6079	A valid density pattern was not read after five retries.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7141.	FRU0621 FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU1122 FRU1132 FRU264 FRU265	
TM607A	A timeout occurred waiting for 'write end' when writing a write density separator.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7144.	FRU116	
TM607B	A timeout occurred waiting for the density separator.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7142.	FRU0621 FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU1122 FRU1132	

1 This FRU is EC sensitive. See CARR-DR 4.

2 This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS: 1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.			See the "Error Displays" on DIAG 552.
TM607C	A timeout occurred while waiting for the IBG after the density separator.	See "Error Analysis" on DIAG 550. See the FSI section for error code 7143.	FRU0621 FRU064 FRU116 FRU118 FRU130 FRU131 FRU132 FRU123 FRU124 FRU125 FRU119 FRU1122 FRU1132	
TM607D	This is a microcode program error.	Call your next level of support.		
TM607E	A timeout occurred waiting for 'gap in' from the drive.	See "Error Analysis" on DIAG 550. See the FSI section for error code 9601.	FRU0851 FRU118 FRU117 FRU134 FRU115	
TM607F	A time out occurred waiting for the drive to be selected on a read or write command.	See "Error Analysis" on DIAG 550. See the FSI section for error code 8005. See the FSI section for error code 8007. See the FSI section for error code 8009.	FRU0851 FRU199 FRU248 FRU118 FRU059 FRU049 FRU108 FRU107 FRU105	
TM6080	This is a microcode program error.	Call your next level of support.		
TM6081	This is a microcode program error.	Call your next level of support.		
TM6082	This is a microcode program error.	Call your next level of support.		
TM6083	A Set Diagnose command was sent to the drive and it did not complete correctly.	See "Error Analysis" on DIAG 550.	FRU0851 FRU199	
TM6084	A Set Diagnose command, sent to the drive, did not complete.	See "Error Analysis" on DIAG 550. See the FSI section for error code 8005. See the FSI section for error code 8007. See the FSI section for error code 8009.	FRU0851 FRU199 FRU248 FRU118 FRU059 FRU049 FRU108 FRU107 FRU105	

1 This FRU is EC sensitive. See CARR-DR 4.

2 This FRU is EC sensitive. FRU112 may not be present. See CARR-CU 7.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUS	ERROR DISPLAYS
	FOLLOW STEPS 1 AND 2 BEFORE TAKING ANY OTHER ACTIONS:	1. If the value of ERA or ERB is other than 00, see the FSI section for error code E100. 2. If PSR bit 0 = 1, see EAD 1 for error code Fnnn.		See the "Error Displays" on DIAG 552.
TM6085	Test EEA4 has completed, and there are one or more errors in the counters. The counters are displayed on the screen with the following first line: BLKS CORR EEA3 EEA4. (See ERROR DISPLAYS on DIAG 552.)	1. See "Error Counts" on DIAG 550. 2. a. Test another drive using the same cartridge. b. Test the the same 2 drives using another cartridge. c. Test both drives using both cartridges. d. Run the test using the other CU (if present). 3. Clean the read/write head. See CARR-DR 1-1, for FRU013. 4. Use the product diskette and run the "unit test" option, looking for a high number of temporary errors.	DR FRU062[1] FRU064 FRU063[1] FRU085[1] FRU216 FRU059 FRU013 CU FRU132 FRU131 FRU130 FRU125 FRU124 FRU123 FRU119 FRU111 FRU199 FRU248 FRU264 FRU265	
TM6086	The DLR external register and drive sense do not agree. Model (A11 and B22) or (A22 and B11).	See CARR-CU 1189 for correct DLR external register switch setting.	FRU118	

[1] This FRU is EC sensitive. See CARR-DR 4.

FAILURE ID	DESCRIPTION	ADDITIONAL ACTIONS	FRUs	ERROR DISPLAYS
TM4087 TM4088	A timeout error occurred during a TIO command to the drive. A drive status error occurred while sending code to the drive.	1. This program has minimum diagnostic capability during the drive patching procedure. 2. This error occurs when a cartridge loader is installed and a cartridge is present in the drive to be tested. 3. This error can be bypassed by loading the functional code into the control unit and setting the control unit on-line. Press unload switch of the drive to be tested, reload diagnostic EE54 and run it. To avoid channel interference set all the channel enable/disable switches to disable. 4. If this error persists, run "Start Repair" on the product diskette.		See the "Error Displays" on DIAG 552.
TM4089 TM408A TM408B	The correct level of code patches is not found on the IML diskette. The correct level of code patches is not found on the IML diskette. Unable to read the IML diskette due to an error.	1. Make sure the diskette in the diskette reader is the correct level. 2. This error occurs when a cartridge loader is installed and a cartridge is present in the drive to be tested. 3. This error can be bypassed by loading the functional code into the control unit and setting the control unit on-line. Press unload switch of the drive to be tested, reload diagnostic EE54 and run it. To avoid channel interference set all the channel enable/disable switches to disable. Ensure that the control unit successfully loads code from the diskette. 4. If this error persists, run "Start Repair" on the product diskette.		

This routine permits the service representative (SR) to select and loop a register in any of the eight control or adapter cards. Addresses, data, clock lines, and so on, can also be scoped in the external register area of the control unit using this scoping utility.

Use the "XR Bus and Control Clocks" timing chart (see EAD 1) as a guide when using this scope procedure.

Error Loop: All errors are ignored when this routine is running.

Test Selection

The following screen displays after routine EEF0 has been selected.

```
DIAG=(EEF0)-ENTER:
           PATTERN
           TTII
```

TT Address for register selection
II Data field (enter 00)

Four characters must be entered for the data pattern to be valid. Valid TT patterns are listed under ENTRY ADDRESS in the table below. If an odd-numbered address is selected, the parity bit is inhibited and the data field will be the default listed in the Address and Register Selection chart in Figure 1.

Parity errors can be forced by selecting the odd number address for the register being tested.

ENTRY ADDRESS	REGISTER TESTED	PARITY INHIBIT	DEFAULT DATA	FUNCTIONAL AREA	CARD LOCATION
21	CCC	Yes	00	Status Store	01A-A1G2
22	CCC	No	FF	Status Store	01A-A1G2
23	WCR	Yes	00	Write Control	01A-A1P2
24	WCR	No	FF	Write Control	01A-A1P2
25	RCR	Yes	00	Read Data	01A-A1S2
26	RCR	No	FF	Read Data	01A-A1S2
27	DCB	Yes	00	Drive-Adapter	01A-A1Q2
28	DCB	No	FF	Drive-Adapter	01A-A1Q2
29	MDO	Yes	00	Maintenance Adapter	01A-A1E2
2A	MDO	No	FF	Maintenance Adapter	01A-A1E2
2B	BMR	Yes	00	Buffer Adapter	01A-A1K2
2C	BMR	No	FF	Buffer Adapter	01A-A1K2
2D	LSP	Yes	00	Microprocessor	01A-A1D2
2E	LSP	No	FF	Microprocessor	01A-A1D2
2F	BCSL	Yes	00	Buffer Control	01A-A1L2
30	BCSL	No	FF	Buffer Control	01A-A1L2

Figure 1. Address and Register Selection Chart

This chart shows which diagnostic is used to test the external registers.

DIAGNOSTIC	REGISTER	LOCATION	FUNCTIONAL AREA
EE12 EE13 EE14	ERA LSP ERB PCR IMR PER ITA PDR ITB PSR JAH XRA JAL PRR*	01A-A1D2	Processor
EE85	MDI MTI MDO MTO PRR*	01A-A1E2	Maintenance
	CCA CER CCC CMR CDR CRR PRR*	01A-A1G2	Status Store
	BCC BDC BCR BDR BCPC BDPH BCPH BDPL BCPL BDSE BCSE BDSH BCSH BDSL BCSL BDSS BCSS BWRP PRR*	01A-A1L2	Buffer
	BD60 BD61 BDAT BMR CIM** CMDT** CMM** CMS**	01A-A1K2	Buffer-Adapter
	DCB DSC DCR DSH DLR DSL DIR DSR DTR ITC DSE PRR*	01A-A1Q2	Drive-Adapter
	RCR RPR RDC RRC RER RSR PRR*	01A-A1S2	Read Data
	WCR WSE PRR*	01A-A1P2	Write Data

* This register is used to send a check reset to any or all functional areas. When the register is written the 'check reset' line is activated, and if bit 3 is inactive, all functional areas whose assigned bit is active perform a check reset.
** These Buffer Adapter registers will be tested in place of the unmarked Buffer Adapter registers if the control unit has the 4.5 Mb/s channel adapter or the Extended Data Recording Format feature.

Figure 2. Diagnostic and External Register Chart

Scope Loop Sync Address

The scope loop routine consists of the following sync address.

SYNC ADDRESS	DESCRIPTION
003A	Set the PCR extend bits on
003C	Write the specified external register
003D	Read the specified external register
003E	Read, 'OR' the data and write it back
0040	Set the extend bits off
0042	Set user reset into the PRR register

Figure 3. Scope Loop Sync Addresses

0 0 0 0 0 0 0 0 0 0

Scope Loop Utility - Routine EEF0

This routine permits the service representative (SR) to select and loop a register in any of the eight control or adapter cards. Addresses, data, clock lines, and so on, can also be scoped in the external register area of the control unit using this scoping utility.

Use the "XR Bus and Control Clocks" timing chart (see EAD 1) as a guide when using this scope procedure.

Error Loop: All errors are ignored when this routine is running.

Test Selection

The following screen displays after routine EEF0 has been selected.

```
DIAG=(EEF0)-ENTER:
           PATTERN
           TTII
```

TT Address for register selection
II Data field (enter 00)

Four characters must be entered for the data pattern to be valid. Valid TT patterns are listed under ENTRY ADDRESS in the table below. If an odd-numbered address is selected, the parity bit is inhibited and the data field will be the default listed in the Address and Register Selection chart in Figure 1.

Parity errors can be forced by selecting the odd number address for the register being tested.

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21	CCC	Yes	00	Status Store	01A-A1G2
22	CCC	No	FF	Status Store	01A-A1G2
23	WCR	Yes	00	Write Control	01A-A1P2
24	WCR	No	FF	Write Control	01A-A1P2
25	RCR	Yes	00	Read Data	01A-A1S2
26	RCR	No	FF	Read Data	01A-A1S2
27	DCB	Yes	00	Drive-Adapter	01A-A1Q2
28	DCB	No	FF	Drive-Adapter	01A-A1Q2
29	MDO	Yes	00	Maintenance Adapter	01A-A1E2
2A	MDO	No	FF	Maintenance Adapter	01A-A1E2
2B	BMR	Yes	00	Buffer Adapter	01A-A1K2
2C	BMR	No	FF	Buffer Adapter	01A-A1K2
2D	LSP	Yes	00	Microprocessor	01A-A1D2
2E	LSP	No	FF	Microprocessor	01A-A1D2
2F	BCSL	Yes	00	Buffer Control	01A-A1L2
30	BCSL	No	FF	Buffer Control	01A-A1L2

Figure 1. Address and Register Selection Chart

This chart shows which diagnostic is used to test the external registers.

DIAGNOSTIC	REGISTER	LOCATION	FUNCTIONAL AREA
EE12 EE13 EE14	ERA LSP ERB PCR IMR PER ITA PDR ITB PSR JAH XRA JAL PRR*	01A-A1D2	Processor
EE85	MDI MTI MDO MTO PRR*	01A-A1E2	Maintenance
	CCA CER CCC CMR CDR CRR PRR*	01A-A1G2	Status Store
	BCC BDC BCR BDR BCPC BDPH BCPH BDPL BCPL BDSE BCSE BDSH BCSH BDSL BCSL BDSS BCSS BWRP PRR*	01A-A1L2	Buffer
	BDGO BMR BDG1 BDAT	01A-A1K2	
	DCB DSC DCR DSH DLR DSL DIR DSR DIR ITC DSE PRR*	01A-A1Q2	Drive-Adapter
	RCR RPR RDC RRC RER RSR PRR*	01A-A1S2	Read Data
	WCR WSE PRR*	01A-A1P2	Write Data

* This register is used to send a check reset to any or all functional areas. When the register is written the 'check reset' line is activated, and if bit 3 is inactive, all functional areas whose assigned bit is active perform a check reset.

Figure 2. Diagnostic and External Register Chart

Scope Loop Sync Address

The scope loop routine consists of the following sync address.

SYNC ADDRESS	DESCRIPTION
003A	Set the PCR extend bits on
003C	Write the specified external register
003D	Read the specified external register
003E	Read, 'OR' the data and write it back
0040	Set the extend bits off
0042	Set user reset into the PRR register

Figure 3. Scope Loop Sync Addresses

Scope Loop Sync Address (Continued)

The scope loop sync address provides a positive going sync pulse, when the microprocessor fetches an instruction from the selected address. The negative going part of this pulse should be used to sync the oscilloscope when scoping the XR timings for a specific part of the EEF0 routine. The first Subsystem Clock S0 time (after the negative transition of the sync pulse) starts that part of the XR timing sequence (see DIAG 610).

This scope loop routine contains the following sync addresses. See DIAG 610 for the following reference key locations.

SYNC ADDRESS	DESCRIPTION
0038 **1**	Turns on both XR page selection XR address extend bits. Sets PCR bits 6 and 7 to one (equals XR page D). They may already be on.
003A **2**	Turns off both XR page selection XR address extend bits. Sets PCR bits 6 and 7 to zero (equals XR page A).
003C **3**	Sets the XR page to the page selected by the service representative. PCR bits 6 and 7, and XR XR extend bits 0 and 1, respectively, are set to the XR page of the selected XR. See Figure 2 on this page.
0040 **4**	Writes the XR that was selected in the "Test Selection". During address selection, the XR address bus contains the address of the selected XR. During write time the XR data bus contains the data specified in the "Data Used" in "Test Selection". See Figure 1 on DIAG 600.
0042 **5**	Reads the XR selected in "Test Selection". During address selection the XR address bus contains the address of the selected XR. During read time, the XR data bus contains the data specified in the "Data Used" (see Figure 1 on DIAG 600) in "Test Selection" that was written into the selected XR during sync address 0040.
0044 **6**	Reads, then writes the XR selected during "Test Selection". During address selection, the XR address bus contains the address of the selected XR. During read time, the XR data bus contains the data specified in the "Data Used" (see Figure 1 on DIAG 600) "Test Selection" that was written into the selected XR during sync address 0040. During write time, the XR data bus contains the data that was read during the read part of this sync address.

Figure 1. Scope Loop Sync Address Descriptions

Set the sync address by performing the following:

1. Start routine EEF0 running (see "Test Selection" on DIAG 600).
2. Press the PF key on the MD.
3. Enter a 2 (alter parameters).
4. The screen displays, WANT TO ALTER TEST PARM? Press Yes.
5. Enter sync address (xxxx). See Figure 1 on this page.
6. On next display enter a 7 (run).
7. IS THIS CORRECT? Press Yes.
8. Attach the scope lead (on this control unit) to 01A-A1E2Z12.

If the following screen is displayed after setting up the scope loop and sync address, you can ignore it because the loop routine is still running.

```
SUPPORT DIAG CNTRL
SECTION:  EExx   #zz
ROUTIN:   EEyy
STS=           /RTN=
```

The following chart indicates which bits are active for any one of the eight registers that can be selected with routine EEF0.

	EXTEND BITS	XR ADDRESS BUS BITS		
	0 1	0 1 2 3 4 P		
XR REGISTER	0 1	2 3 4 5 6 7	FUNCTIONAL AREA	CARD LOCATION
CCC	0 0	0 0 0 0 0 0	Status Store	01A-A1G2
WCR	0 1	0 0 0 0 0 0	Write Data Flow	01A-A1P2
RCR	0 1	0 0 0 1 0 1	Read Clock/Format	01A-A1S2
DCB	0 1	1 1 0 0 0 0	Drive-Adapter	01A-A1Q2
MDO	1 0	1 0 0 1 1 1	Maint. Adapter	01A-A1E2
BMR	1 1	1 0 1 1 1 0	Buffer Adapter	01A-A1K2
LSP	1 1	1 1 1 1 1 1	Microprocessor	01A-A1D2
BCSL	1 1	0 0 1 0 1 0	Buffer Adapter	01A-A1L2

Figure 2. Extend Bit and XR Register Chart

The notes on this page refer to to the diagram on DIAG 615.

Notes:

1. *The logic card that contains the XR that is selected turns on its line to the MA card. Each line name identifies the card that it came from. For example, selecting the CCC register's XR turns on '-SS addressed' line to the MA card. The MA card checks the lines from all cards to ensure that only one XR is selected at a time. It also checks that one line is on during all XR operations.*

   The logic pages used are: BA001, DF001, DI001, MP003, RC001, SS001, MA001, and MA002.

2. *To read the XR selected by the XR address and XR extended bits 0 and 1 at S18-S21 time. However, the XR data read from the selected XR is actually latched.*

   The logic pages used are: BA001, DI001, MA001, RC001, SS001. in the microprocessor card at S18-S19 time.

3. *To all microprocessors cards with XR registers. If active during 'XR addressed clock' time, a check 2 and 'XR error latched' are set.*

4. *The microprocessor card samples 'XR error ungated' during S9-S10 time for XR write, and S20-S21 time for XR read.*

5. *When the MP instruction decodes as an XR write, data is put on the XR data bus and write gate is turned on.*

   0038 - PCR bits 6,7 = 1,1
   003A - PCR bits 6,7 0,0
   003C - PCR bits 6,7 = XR page of selected XR (see Figure 2 on this page)
   0040 - From EEF0's, data used in the write data test selection parameter
   0042 - SR selected XR read data that was written in address sync word 0040 cycle

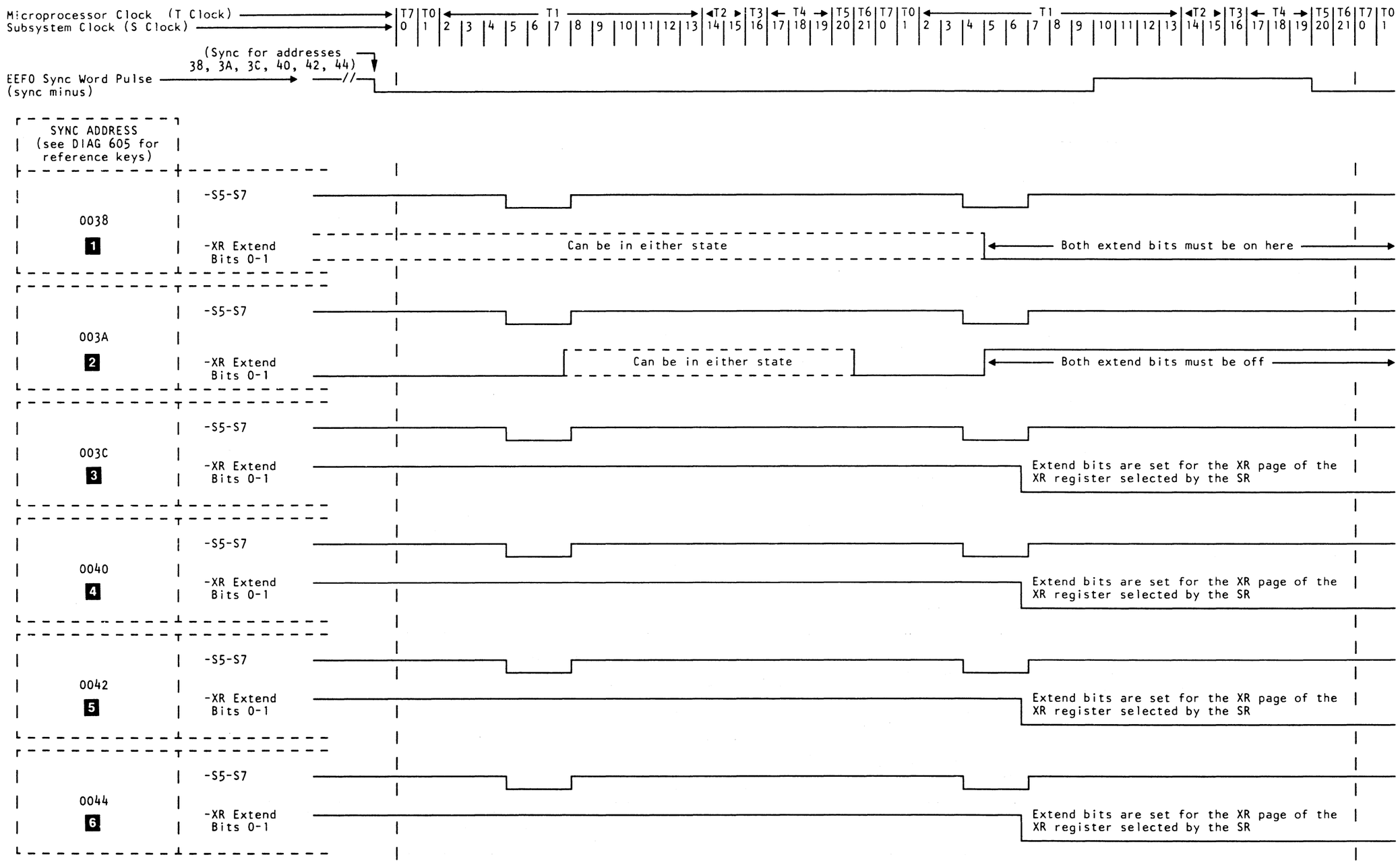
   The bidirectional XR data bus can have write data on it from S0-S14 time, but the selected XR writes at S5-S7 'XR load' time. The XR data bus can have read data on it at S18-S21 time, however, it is set into the microprocessor card's read data register (RDR) at S18-S19 time.

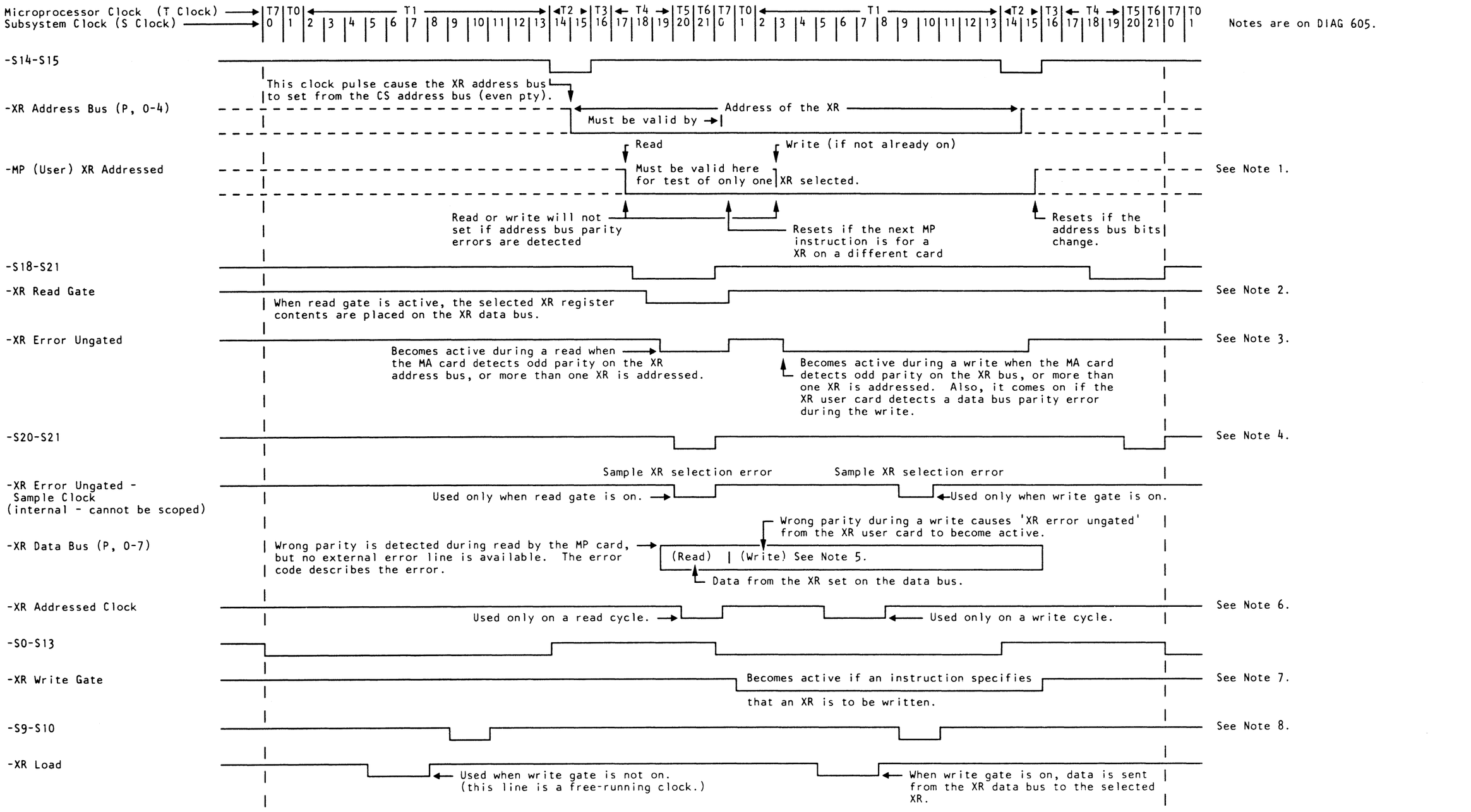
6. *Used by the MA to validate its 'one and only one' check.*

7. *To write the XR selected by the XR address and XR extend bits 0 and 1 at S0-S13 time. The XR write data is set on the XR data bus at S0-S13 time, but the selected XR sets at S5-S7 'XR load' time.*

   The logic pages used are: BA001, DF001, DI001, MA001, RC001, SS001.

8. *To all XR cards on logics pages BA001, DF001, DI001, MA001, RC001, SS001 and to BA003 from BA002 as '-XR load clock'.*





Drive Patch Load Utility - Routine EEF1

This routine is used to automatically read microcode from the IML diskette and then send it to the drive.

Error Loop does not apply to this routine.

Test Selection

This routine cannot be selected directly from the maintenance device (MD).

When any routine is loaded that requires drive microcode patches from the IML diskette, this routine is automatically loaded.

Drive Command Exerciser

The drive command exerciser is a group of programs, on the support diskette, which permits you to test a suspect drive for failures. The support diskette is loaded on a maintenance device (MD), which is connected to a control unit. The drive command exerciser issues commands to the suspect drive in a concurrent maintenance mode. The exerciser can be used to isolate drive motion problems or failures caused by a specific command sequence.

You must select one channel adapter and one drive to run the commands on. The maintenance device (MD) will display the channel adapters you are allowed to select from. Only those channel adapters that the control unit microcode is able to communicate with, will be displayed. If you select a channel adapter that is not on the MD display, an error is caused.

You can run a predefined group of commands to the drive by selecting routine 1 or 2, or you can run a group of commands of your own selection, up to a maximum of eight commands.

> **Note:** Routine 2 cannot be looped because the last command of that routine is a Rewind Unload. Any group of commands that contains a Rewind Unload (RUN) command should not be looped, because it can cause errors.
>
> Any motion command issued to a drive after a Rewind Unload (RUN) command will cause an error.

A command is entered by keying in the command acronym and pressing the ENTER key. When all the commands in the chain are entered, a null entry (the ENTER key is pressed again) signals the program that all the command entries have been made. A run mode option selection screen is then displayed.

Once a command chain is entered and the run mode is selected, the MD sends the commands to the control unit. Each command is executed in turn. Status from the control unit is sent to the MD and is analyzed by the exerciser microprogram. Depending on the status returned from the control unit, one of the following actions are taken:

- If the command sent receives a good beginning and ending status from the device, the next command is issued.
- If the status returned is a channel command retry, the same command is reissued.
- If the status returned is a unit check, the program gets sense data from the control unit and displays an error message followed by the sense data.

Commands

Commands are entered as acronyms by way of the maintenance device keyboard/display. If additional data such as record number, data length, and number of blocks is required, the exerciser microprogram will request the information.

The following commands are supported by the drive command exerciser:

- BSB - Backspace block
- BSF - Backspace file
- DSE - Data security erase
- ERG - Erase gap
- FSB - Forward space block
- FSF - Forward space file
- LDD - Load display
- LOC - Locate block
- MDS - Mode set
- NOP - No operation
- RBI - Read block ID
- RBK - Read backward
- RBL - Read buffered log
- RDF - Read forward
- REW - Rewind
- RUN - Rewind unload
- SID - Sense path/group ID
- SIO - Sense I/O
- SNS - Sense
- TIO - Test I/O
- WRT - Write to tape with synchronize buffer command
- WTM - Write tapemark
- RES - Reserve device
- REL - Release device

For write data commands that execute in tape write immediate mode (SYN - Synchronize buffer), block size (1K increments to 32K) and block count (1 to 256) must be defined.

Run Mode Options

Execution run mode options are:

- **Once:** The command or command chain executes once.
- **Continuous Loop:** The loop continues until an MD function key is pressed, or an error is detected. If an error is detected, the loop ends and an error message is displayed on the MD keyboard/display. The error message is followed by 32 bytes of sense information.

  > **Note:** The loop option should not be selected if you are using the Rewind Unload (RUN) command. If loop is used with a group of commands containing Rewind Unload, an error will occur.

- **Loop 255 Times:** The command or command chain loops 255 times, or until an error is detected. If an error is detected, the loop ends and an error message is displayed on the MD keyboard/display. The error message is followed by 32 bytes of sense information.

Status and error data sent to the MD keyboard/display contains the same information as would normally be sent to the host system.

Error Display

If an error is detected while the drive command exerciser is executing, the following error screen is displayed.

The first and second lines are used to display an error message that describes the error. The last line is used to indicate the command that was executing when the error occurred.

```
     (Error
     Message)
ON THE COMMAND:
(Command)
```

Error Messages

The following error messages are displayed on lines 1 and 2 of the MD keyboard/display when an error is detected while the drive command exerciser is executing.

LOOK AT SENSE FOR PROBLEM

INCORRECT NUMBER OF DATA BYTES SNT

DEVICE IS IN USE

INVALID DATA WITH COMMAND

CANNOT RELEASE, NOT RESERVED

NEED RES TO EXECUTE COMMAND

INVALID DIAGNOSTIC OP-CODE

INVALID CHANNEL OP-CODE

CANNOT SCHEDULE OPERATION

SENSE HAS ERROR DATA

TIMEOUT ALLOC BUFF SW

ERR DUR. WRTCARR WCA ORDER

ERR DUR. WRTCACC WCA ORDER

ERR DUR. DIAGINT WCA ORDER

TIMEOUT DURING PMA RESP.

FOUND DEVICE XFER ACTIVE

THE TAPE IS FILE PROTECTED

DEVICE IS NOT READY

CHANNEL COMMAND RETRY

NO BUFFER RECORDS PRESENT

BUFFER IS IN USE

NO ROOM IN BRT TO CREATE REC

DEVICE IS NOT ONLINE

BUFFER DATA NOT CORRECT

XR ERROR

DEFERRED UNIT CHECK

CHANNEL TRANSFER ACTIVE

SNS ERROR MATCH CODE MATC

ERROR PROCESSING RBSSSS ORDER

ERR DUR. DIAG MODEWCA ORDER

UNIT CK END STAT FROM DV

ERR DURING SWB SSS ORDER

ERR DURING RBE SSS ORDER

ERR DUR. RDCADC RCA ORDER

ERR DUR. WTCADS WCA ORDER

DIDNT SEE IBG DUR LWR CMND

BCSE NOT COMP OR FRU ACTIVE

BDSE FRUS ACTIVE

ATTEMPTING TO RD INVAL CS

RD BUFF POINTERS FOR TM

SET OF DIAG MODE FAILED

ERR DUR DEV SEL SEQUENCE

ERR DUR DEV CMND SEQUENCE

RESET OF DIAG MODE FAILED

DO RBP CMND B4 DEL REC

TIMEOUT ENDING LWR OP

The drive command exerciser is a group of programs, on the support diskette, which permits you to test a suspect drive for failures. The support diskette is loaded on a maintenance device (MD), which is connected to a control unit. The drive command exerciser issues commands to the suspect drive in a concurrent maintenance mode. The exerciser can be used to isolate drive motion problems or failures caused by a specific command sequence.

You must select one channel adapter and one drive to run the commands on. The maintenance device (MD) will display the channel adapters you are allowed to select from. Only those channel adapters that the control unit microcode is able to communicate with, will be displayed. If you select a channel adapter that is not on the MD display, an error is caused.

You can run a predefined group of commands to the drive by selecting routine 1 or 2, or you can run a group of commands of your own selection, up to a maximum of eight commands.

Note: Routine 2 cannot be looped because the last command of that routine is a Rewind Unload. Any group of commands that contains a Rewind Unload (RUN) command should not be looped, because it can cause errors.

Any motion command issued to a drive after a Rewind Unload (RUN) command will cause an error.

A command is entered by keying in the command acronym and pressing the ENTER key. When all the commands in the chain are entered, a null entry (the ENTER key is pressed again) signals the program that all the command entries have been made. A run mode option selection screen is then displayed.

Once a command chain is entered and the run mode is selected, the MD sends the commands to the control unit. Each command is executed in turn. Status from the control unit is sent to the MD and is analyzed by the exerciser microprogram. Depending on the status returned from the control unit, one of the following actions are taken:

- If the command sent receives a good beginning and ending status from the device, the next command is issued.
- If the status returned is a channel command retry, the same command is reissued.
- If the status returned is a unit check, the program gets sense data from the control unit and displays an error message followed by the sense data.

Note: The control unit error light can blink on and off under certain normal operating conditions. Real errors will be reported on the error display.

Commands

Commands are entered as acronyms by way of the maintenance device keyboard/display. If additional data such as record number, data length, and number of blocks is required, the exerciser microprogram will request the information.

The following commands are supported by the drive command exerciser:

- BSB - Backspace block
- BSF - Backspace file
- DSE - Data security erase
- ERG - Erase gap
- FSB - Forward space block
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- LDD - Load display
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- RDF - Read forward
- REW - Rewind
- RUN - Rewind unload
- SID - Sense path/group ID
- SIO - Sense I/O
- SNS - Sense
- TIO - Test I/O
- WRT - Write to tape with synchronize buffer command
- WTM - Write tapemark
- RES - Reserve device
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For write data commands that execute in tape write immediate mode (SYN - Synchronize buffer), block size (1K increments to 32K) and block count (1 to 256) must be defined.

Run Mode Options

Execution run mode options are:

- **Once:** The command or command chain executes once.
- **Continuous Loop:** The loop continues until an MD function key is pressed, or an error is detected. If an error is detected, the loop ends and an error message is displayed on the MD keyboard/display. The error message is followed by 32 bytes of sense information.

  Note: The loop option should not be selected if you are using the Rewind Unload (RUN) command. If loop is used with a group of commands containing Rewind Unload, an error will occur.
- **Loop 255 Times:** The command or command chain loops 255 times, or until an error is detected. If an error is detected, the loop ends and an error message is displayed on the MD keyboard/display. The error message is followed by 32 bytes of sense information.

Status and error data sent to the MD keyboard/display contains the same information as would normally be sent to the host system.

Error Display

If an error is detected while the drive command exerciser is executing, the following error screen is displayed.

The first and second lines are used to display an error message that describes the error. The last line is used to indicate the command that was executing when the error occurred.

```
(Error
 Message)
ON THE COMMAND:
(Command)
```

Error Messages

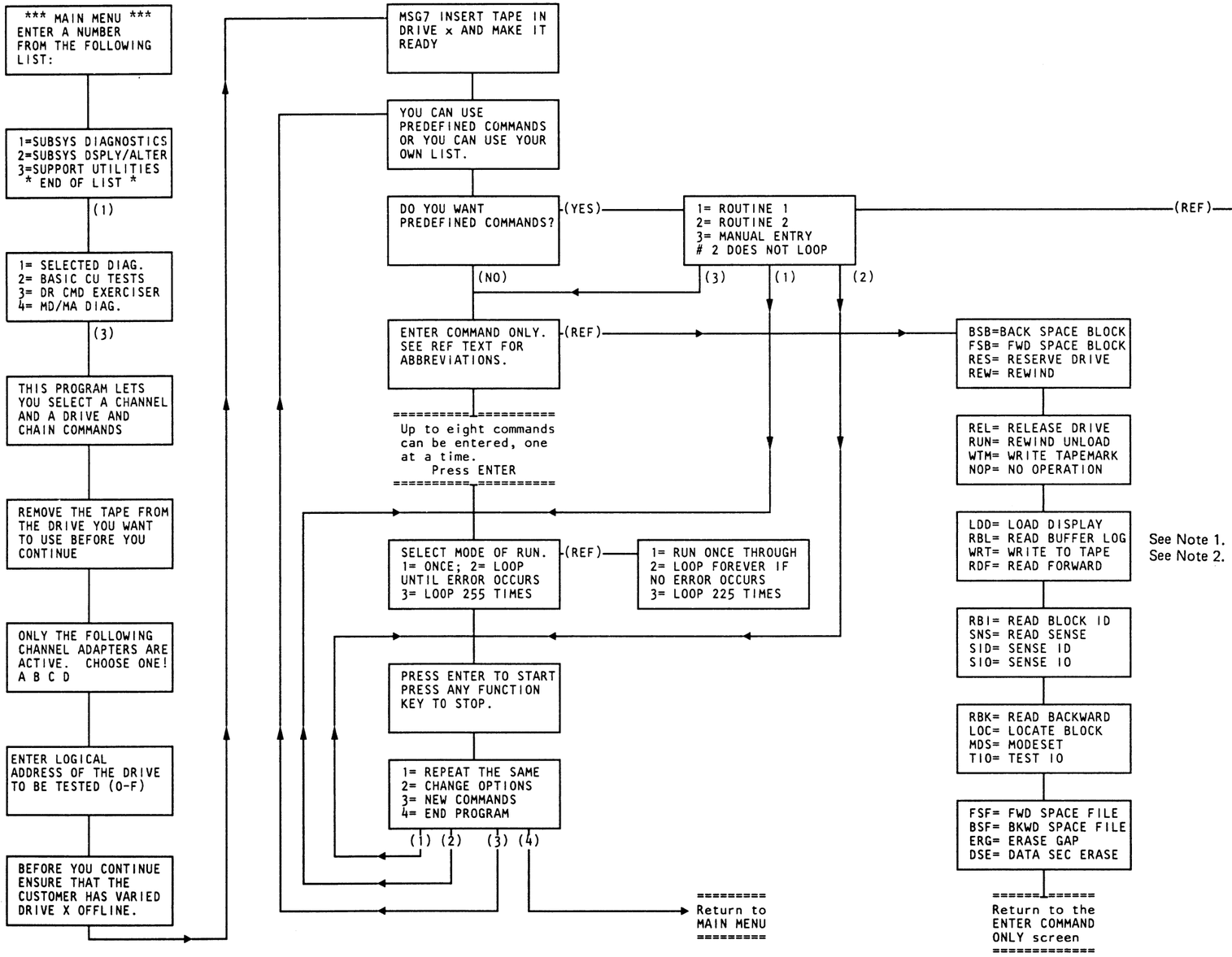
The following error messages are displayed on lines 1 and 2 of the MD keyboard/display when an error is detected while the drive command exerciser is executing.

LOOK AT SENSE FOR PROBLEM
INCORRECT NUMBER OF DATA BYTES SNT
DEVICE IS IN USE
INVALID DATA WITH COMMAND
CANNOT RELEASE, NOT RESERVED
NEED RES TO EXECUTE COMMAND
INVALID DIAGNOSTIC OP-CODE
INVALID CHANNEL OP-CODE
CANNOT SCHEDULE OPERATION
SENSE HAS ERROR DATA
TIMEOUT ALLOC BUFF SW
ERR DUR. WRTCARR WCA ORDER
ERR DUR. WRTCACC WCA ORDER
ERR DUR. DIAGINT WCA ORDER
TIMEOUT DURING PMA RESP.
FOUND DEVICE XFER ACTIVE
THE TAPE IS FILE PROTECTED
DEVICE IS NOT READY
CHANNEL COMMAND RETRY
NO BUFFER RECORDS PRESENT
BUFFER IS IN USE
NO ROOM IN BRT TO CREATE REC
DEVICE IS NOT ONLINE
BUFFER DATA NOT CORRECT
XR ERROR
DEFERRED UNIT CHECK
CHANNEL TRANSFER ACTIVE
SNS ERROR MATCH CODE MATC
ERROR PROCESSING RBSSSS ORDER
ERR DUR. DIAG MODEWCA ORDER
UNIT CK END STAT FROM DV
ERR DURING SWB SSS ORDER
ERR DURING RBE SSS ORDER
ERR DUR. RDCADC RCA ORDER
ERR DUR. WTCADS WCA ORDER
DIDNT SEE IBG DUR LWR CMND
BCSE NOT COMP OR FRU ACTIVE
BDSE FRUS ACTIVE
ATTEMPTING TO RD INVAL CS
RD BUFF POINTERS FOR TM
SET OF DIAG MODE FAILED
ERR DUR DEV SEL SEQUENCE
ERR DUR DEV CMND SEQUENCE
RESET OF DIAG MODE FAILED
DO RBP CMND B4 DEL REC
TIMEOUT ENDING LWR OP

0 0 0 0 0 0 0 0 0 0

Drive Command Exerciser (Continued) DIAG 721

Drive Command Exerciser Diagram



Note 1: The actual number of blocks written to tape using the write command is twice as many as entered on the MD keyboard.

Note 2. Read commands will read multiple blocks from the drive. The next read command will purge the buffer and read the following block from the drive.

Drive Command Exerciser Details

The Drive Command Exerciser programs are written on the support diskette. Once the support diskette has been placed in the maintenance device and the control program has been loaded, the MD display screen indicates the control unit serial number and the EC level and part number of the support diskette.

Press ENTER: The following screen displays.

```
 *** MAIN MENU ***
ENTER A NUMBER
FROM THE FOLLOWING
LIST.
```

Press ENTER: The following screen displays.

```
1=SUBSYS DIAGNOSTICS
2=SUBSYS DSPLY/ALTER
3=SUPPORT UTILITIES
 * END OF LIST *
```

Enter a 1: The following screen displays.

```
1= SELECTED DIAG.
2= BASIC CU TESTS
3= DR CMD EXERCISER
4= MD/MA DIAG.
```

Enter a 3: The following information screen displays.

```
THIS PROGRAM LETS
YOU SELECT A CHANNEL
AND A DRIVE AND
CHAIN COMMANDS.
```

Press ENTER: The following screen displays.

```
REMOVE THE TAPE FROM
THE DRIVE YOU WANT
TO USE BEFORE YOU
CONTINUE
```

- Remove the cartridge completely from the drive.

Press ENTER: The following screen displays.

```
ONLY THE FOLLOWING
CHANNEL ADAPTERS ARE
ACTIVE.  CHOOSE ONE!
A B C D
```

- The channel adapter that is to be tested is selected from this display.
- Any adapter not shown is either not working correctly or not present.

Enter an A, B, C, or D: The following screen displays.

```
ENTER UNIT ADDRESS
OF THE DRIVE TO BE
TESTED. (0-F)
```

- This entry identifies the tape drive that will be tested.

Note: In a dual control unit configuration the MD can be attached to either control unit; therefore, any drive can be tested.

Enter the drive address: The following screen displays.

```
BEFORE YOU CONTINUE
ENSURE THAT THE
CUSTOMER HAS VARIED
DRIVE X OFFLINE.
```

- X = Current drive being tested.

Press ENTER: The following screen displays.

```
MSG7 INSERT TAPE IN
DRIVE X AND MAKE IT
READY
```

- This entry prepares the drive you want to use so the MD can exercise it.

  After the drive is ready, **press ENTER**. The following screen displays.

```
DO YOU WANT
PREDEFINED COMMANDS?
```

- A YES response to "Do you want predefined commands?" causes the following screen to display:

```
1 = ROUTINE1
2 = ROUTINE2
3 = MANUAL ENTRY
# 2 DOES NOT LOOP
```

If you press the ref key while the above display is active, you will be shown the contents of routine 1:

- REW, WRT(16x), WTM, BSF, LOC, RDF(10x), RBK(10x) and FSF commands.

And the contents of routine 2:

- REW, WTM, DSE, REW, FSF, WRT(511x), WTM BSF, LOC, LOC, BSF, LDD, and RUN commands.

If one of the routines is selected, each command executes in the sequence noted above.

- A NO response to "Do you want predefined commands?" causes the following screen to display:

```
ENTER COMMAND ONLY.
SEE REF TEXT FOR
ABBREVIATIONS.
```

- Commands can be entered from this screen only.
- Up to eight commands can be entered, one at a time.
- If the command abbreviations are not known, pressing the REF key will cause prompting screens to display. See the Drive Command Exerciser Diagram for the content of the screens (DIAG 721).
  - Pressing REF causes the next prompting screen to display.
  - Pressing RET causes the 'ENTER COMMAND ONLY' screen to return.
- Press ENTER after each command abbreviation is keyed in.

  Note: If the LDD, WRT, LOC, or MDS commands are entered, additional prompting screens will display. See Prompting Screens on DIAG 725 for the content of the screens.

Press ENTER: The following screen displays.

```
SELECT MODE OF RUN
1= ONCE; 2= LOOP
UNTIL ERROR OCCURS
3= LOOP 255 TIMES
```

- Pressing the REF key causes a prompting screen to display that defines the selections.
  - ONCE - The commands run one time.
  - CONTINUOUS LOOP - The loop continues until an MD function key is pressed, or an error occurs. If an error is detected, the loop ends and an error message is displayed on the MD keyboard/display. The error message is followed by 32 bytes of sense information.
  - LOOP 255 TIMES - The command or command chain loops 255 times. If an error is detected, the loop ends and an error message is displayed. The error screen is followed by another screen that contains 32 bytes of sense information.

Note: The loop option should not be selected if you are using the Rewind Unload (RUN) command. If loop is used with a group of commands containing Rewind Unload, an error will occur. **Select the run mode and press ENTER:** The following screen displays.

```
PRESS ENTER TO START
PRESS ANY FUNCTION
KEY TO STOP.
```

Press ENTER: The following screen displays.

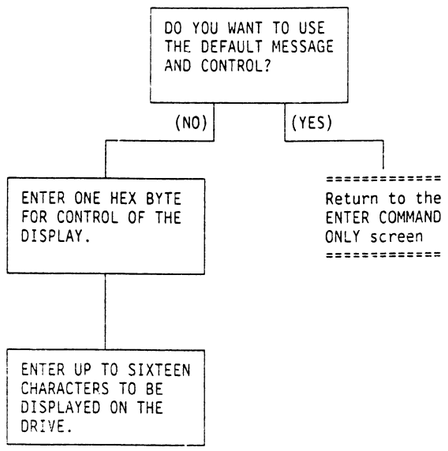
```
1= REPEAT THE SAME
2= CHANGE OPTIONS
3= NEW COMMANDS
4= END PROGRAM
```

- See the Drive Command Exerciser Diagram (DIAG 721) for the paths taken for each selection.
- If routine 2 is being used, you cannot change options. If you select option 2 it will default to option 1.

Drive Command Exerciser Details DIAG 722

Prompting Screens

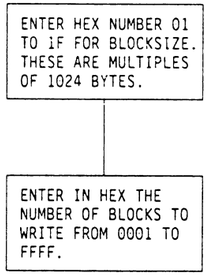
Load Display (LDD)



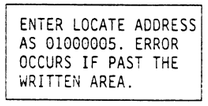
The bits used to control the load display option are defined as follows:

- Bits 0, 1, and 2
  - 000 - Permit drive message to overlay message
  - 001 - No overlay unless tape is removed
  - 010 - No overlay until drive is ready
  - 111 - Display both messages until cartridge is removed, then display 9 - 16 until the drive is ready.
- Bit 3
  - 0 - Display message specified by bit 5
  - 1 - Display both messages
- Bit 4
  - 1 - Flash message specified by bit 5
- Bit 5
  - 0 - Display bytes 1 through 8
  - 1 - Display bytes 9 through 16
- Bits 6 and 7.
  - Reserved

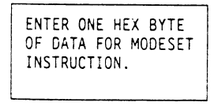
Write To Tape (WRT)



Locate Block (LOC)



Modeset (MDS)



The bits used to enter one byte of data for a modeset instruction are defined as follows:

- Bits 0 and 1 - Tape Format
  - 00 - Write 18 track format
  - 01 - Reserved
  - 10 - Reserved
  - 11 - Reserved
- Bit 2 - Write Mode
  - 0 - Buffered write
  - 1 - Tape write mode
- Bit 3 - Inhibit Supervisor Commands
  - 0 - Execute supervisor commands
  - 1 - Inhibit supervisor commands
- Bits 4, 5, and 6 - Reserved
- Bit 7 - Inhibit Control Unit Error Recovery.
  - 0 - Automatic error recovery takes place
  - 1 - Temporary read and write errors reported as permanent errors.

Note: Registers marked with a * may or may not be present depending upon the EC level and installed features.

0 0 0 0 0 0 0 0 0 0

Contents

* These registers are EC sensitive and may or may not be present.

Functional Areas

The microprocessor communicates data that can be used for problem analysis via external registers. These one byte wide registers are distributed throughout the control unit and are attached to the processor by the External Register Interface. The registers may be read only, write only, or read/write.

Functional areas serviced by the registers are the following:

- Buffer area and control
- Drive adapter interface
- Maintenance adapter
- Microprocessor
- Read data flow
- Status store
- Write data flow

Note: The location of bit definitions for individual registers can be found in the table of contents. Storage fields that are loaded by the microcode with subsystem error and status information are also defined.

External Register Address Cross-Reference Tables

The external register cross-reference tables contain the following information:

- **REGISTER NAME:**

  Formal name of the register.

- **REGISTER MNEM/TYPE:**

  MNEM - Mnemonic name of the register.

  TYPE - Type of register.

  - R = Read
  - W = Write
  - R/W = Read and Write

- **XR PAGE:**

  XR page select address.

  The XR page defines groups of external registers that have the same address. That is, two external registers may have the address hexadecimal 02, but they are defined as different locations by the XR page. The pages are controlled by the XR address extend bits 0 and 1, shown on logic page MP001, as follows:

XR Address Extend	
Bits 0 1	Page
0 0	A
0 1	B
1 0	C
1 1	D

- **ADDRESS:**

  The actual register address in the buffer page. Both hexadecimal and decimal values are provided.

- **XRA VALUE:**

  The external register address value as it appears on the Maintenance Device (MD) display.

External Register Addressing

Addresses for the XR registers are generated from the XR address bus and the XR address extend bits 0 and 1. The extend bits become bits 0 and 1 of the XRA register. Bits 0, 1, 2, 3, 4, and P of the XR address bus become XRA register address bits 2, 3, 4, 5, 6, and 7.

XR register address bits 2, 3, 4, 5, 6, and 7 are used to address multiple XR registers and the extend bits control which register (page) will be selected. The XR address extend bits do not have any parity bits associated with them. The parity of the XR address bus is even.

XR Address Extend Bits	XR Address Bus Bits
0 1	0 1 2 3 4 P

XRA Register	
Extend Bits	Address Bits
0 1	2 3 4 5 6 7

Examples of Address Bus/XRA Translation

- XR Page/Address Bus to XRA

EXAMPLE 1

```
XR Page=D

XR Address Bus = Hex 00

  XR          XR
  Address     Address
  Extend      Bus
  Bits        Bits

   D   0      0
  ---- ---- ----
  0 1  0 1 2 3 4 P
  1 1  0 0 0 0 0
                  0 <- Add 0 to maintain even
                       parity for address bus
                       bits 0-4

  1 1  0 0 0 0 0 0
  ---- ---- ----
    C    0     =  XRA value
```

EXAMPLE 2

```
XR Page=B

XR Address Bus = Hex 13

  XR          XR
  Address     Address
  Extend      Bus
  Bits        Bits

   D   0      0
  ---- ---- ----
  0 1  0 1 2 3 4 P
  0 1  1 0 0 1 1
                  1 <- Add 0 to maintain even
                       parity for address bus
                       bits 0-4

  0 1  1 0 0 1 1 1
  ---- ---- ----
    6    7     =  XRA value
```

- XR to XR Page/Address Bus Examples

EXAMPLE 1

```
XRA value = E2
        XRA
        Value
        Bits

       E    2
  ---------- ----------
  0 1 2 3 4 5 6 7
  1 1 1 0 0 0 1 0
  ---------- ----------
  XR         XR
  Extend     Address
  Address    Bus
  Bits       Bits

  0 1        0 1 2 3 4 P
  1 1                     = XR page D
             1 0 0 0 1 0  = XR address bus
             1 0 0 0 1 X
             ---- ----
               1    1     = XR address
                            Hex 11 (17 decimal)
```

EXAMPLE 2

```
XRA value = A1
        XRA
        Value
        Bits

       A    1
  ---------- ----------
  0 1 2 3 4 5 6 7
  1 0 1 0 0 0 0 1
  ---------- ----------
  XR         XR
  Extend     Address
  Address    Bus
  Bits       Bits

  0 1        0 1 2 3 4 P
  1 0                     = XR page C
             1 0 0 0 0 1  = XR address bus
             1 0 0 0 0 X
             ---- ----
               1    0     = XR address
                            Hex 10 (16 decimal)
```

Cross Reference Tables

Note: Not all the registers are defined in this section. Only those registers that are useful for troubleshooting are defined.

Buffer Control Card (01A-A1L2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
BCPH	R/W	Buffer Channel Pointer High	D	00	0	C0
BCPL	R/W	Buffer Channel Pointer Low	D	01	1	C3
BDPH	R/W	Buffer Device Pointer High	D	02	02	C5
BDPL	R/W	Buffer Device Pointer Low	D	03	3	C6
BCSH	R/W	Buffer Channel Stop High	D	04	4	C9
BCSL	R/W	Buffer Channel Stop Low	D	05	5	CA
BDSH	R/W	Buffer Device Stop High	D	06	6	CC
BDSL	R/W	Buffer Device Stop Low	D	07	7	CF
BWRP	R/W	Buffer Wrap	D	08	8	D1
BCC	R/W	Buffer Channel Command	D	09	9	D2
BCSE	R/W	Buffer Channel Status/Error	D	0A	10	D4
BCR	R/W	Buffer Channel Remainder	D	0B	11	D7
BCSS	R/W	Buffer Channel SARS	D	0C	12	D8
BCPC	W	Buffer Channel Pad Counter	D	0D	13	DB
BDC	R/W	Buffer Device Command	D	OE	14	DD
BDSE	R/W	Buffer Device Status/Error	D	0F	15	DE
BDR	R/W	Buffer Device Remainder	D	10	16	E1
BDSS	R/W	Buffer Device SARS	D	11	17	E2

Buffer Adapter Card (01A-A1K2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
BDAT	R/W	Buffer Data (Pseudo Name)	D	12	18	E4
BDG0	R/W	Buffer Diagnostic 0	D	15	21	EB
BDG1	R/W	Buffer Diagnostic 1	D	16	22	ED
BMR	R/W	Buffer Mode Register	D	17	23	EE

Buffer Adapter Card (01A-A1K2) with 4.5 Mb/s Channel or Improved Data Recording Capability

Replaces the above table when installed.

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
CMDT	R/W	Diagnostic Data	D	12	18	E4
CMRS	R/W	Register Select	D	13	19	E7
CMRP	R/W	Register Page	D	14	20	E8
CMS	R	Status	D	15	21	EB

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
CMM	R/W	Mode	D	16	22	ED
CHM	R/W	Channel Mode	D	17	23	EE

Drive Adapter Card (01A-A1Q2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
DLR	R	Device Level Register	A	10	16	21
DSH	R	Control Unit Serial High	A	11	17	22
DSL	R	Control Unit Serial Low	A	12	18	24
DIR	R	Device Interrupt Register	B	10	16	61
ITC	R/W	Interval Timer C	B	11	17	62
DCR	R/W	Device Control Register	B	12	18	64
DSE	R	Device Status/Error	B	13	19	67
DCB	R/W	Device Control Bus	B	14	20	68
DTR	R/W	Device Tag Register	B	15	21	6B
DSC	R/W	Device Secondary Clock	B	16	22	6D
DSR	R/W	Device Secondary Register	B	17	23	6E

Maintenance Adapter Card (01A-A1E2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
MTI	R/W	Maintenance Tag In	C	10	16	A1
MTO	R/W	Maintenance Tag Out	C	11	17	A2
MDI	R	Maintenance Data In	C	12	18	A4
MDO	R/W	Maintenance Data Out	C	13	19	A7
MSB	R	Maintenance Status Byte	*	*	*	*

Note: * These registers are not directly addressable, but can be displayed by using the Support Diskette.

0 0 0 0 0 0 0 0 0 0

Cross Reference Tables

Note: Not all the registers are defined in this section. Only those registers that are useful for troubleshooting are defined.

Buffer Control Card (01A-A1L2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
BCPH	R/W	Buffer Channel Pointer High	D	00	0	C0
BCPL	R/W	Buffer Channel Pointer Low	D	01	1	C3
BDPH	R/W	Buffer Device Pointer High	D	02	02	C5
BDPL	R/W	Buffer Device Pointer Low	D	03	3	C6
BCSH	R/W	Buffer Channel Stop High	D	04	4	C9
BCSL	R/W	Buffer Channel Stop Low	D	05	5	CA
BDSH	R/W	Buffer Device Stop High	D	06	6	CC
BDSL	R/W	Buffer Device Stop Low	D	07	7	CF
BWRP	R/W	Buffer Wrap	D	08	8	D1
BCC	R/W	Buffer Channel Command	D	09	9	D2
BCSE	R/W	Buffer Channel Status/Error	D	0A	10	D4
BCR	R/W	Buffer Channel Remainder	D	0B	11	D7
BCSS	R/W	Buffer Channel SARS	D	0C	12	D8
BCPC	W	Buffer Channel Pad Counter	D	0D	13	DB
BDC	R/W	Buffer Device Command	D	OE	14	DD
BDSE	R/W	Buffer Device Status/Error	D	0F	15	DE
BDR	R/W	Buffer Device Remainder	D	10	16	E1
BDSS	R/W	Buffer Device SARS	D	11	17	E2

Buffer Adapter Card (01A-A1K2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
BDAT	R/W	Buffer Data (Pseudo Name)	D	12	18	E4
BDG0	R/W	Buffer Diagnostic 0	D	15	21	EB
BDG1	R/W	Buffer Diagnostic 1	D	16	22	ED
BMR	R/W	Buffer Mode Register	D	17	23	EE

4.5 Mb/s Buffer Adapter Card (01A-A1K2)

Replaces the above table when installed.

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
CMDT	R/W	Diagnostic Data	D	12	18	E4
CMRS	R/W	Register Select	D	13	19	E7
CMRP	R/W	Register Page	D	14	20	E8
CMS	R	Status	D	15	21	EB
CMM	R/W	Mode	D	16	22	ED
CHM	R/W	Channel Mode	D	17	23	EE

Drive Adapter Card (01A-A1Q2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
DLR	R	Device Level Register	A	10	16	21
DSH	R	Control Unit Serial High	A	11	17	22
DSL	R	Control Unit Serial Low	A	12	18	24
DIR	R	Device Interrupt Register	B	10	16	61
ITC	R/W	Interval Timer C	B	11	17	62
DCR	R/W	Device Control Register	B	12	18	64
DSE	R	Device Status/Error	B	13	19	67
DCB	R/W	Device Control Bus	B	14	20	68
DTR	R/W	Device Tag Register	B	15	21	6B
DSC	R/W	Device Secondary Clock	B	16	22	6D
DSR	R/W	Device Secondary Register	B	17	23	6E

Maintenance Adapter Card (01A-A1E2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	Addr Dec	XRA Value
MTI	R/W	Maintenance Tag In	C	10	16	A1
MTO	R/W	Maintenance Tag Out	C	11	17	A2
MDI	R	Maintenance Data In	C	12	18	A4
MDO	R/W	Maintenance Data Out	C	13	19	A7
MSB	R	Maintenance Status Byte	*	*	*	*

Note: * These registers are not directly addressable, but can be displayed by using the Support Diskette.

Cross-Reference Tables (Continued)

Microprocessor Card (01A-A1D2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	ess Dec	XRA Value
ITB	W	Interval Timer B	A/B	18	4	30/70
ERA	R	Error Register A	C	18	4	B0
ERB	R	Error Register B	D	18	4	F0
ITA	R/W	Interval Timer A	A/B	19	5	33/73
XRA	R	External Register Address	C/D	19	5	B3/F3
PER	R	Processor Error Register	A/B/C/D	1A	6	35/75/ B5/F5
JAL	W	Jump Address Low	A/B/C/D	1A	6	35/75/ B5/F5
PSR	R	Processor Status Register	A/B/C/D	1B	7	36/76/ B6/F6
JAH	W	Jump Address High	A/B/C/D	1B	7	36/76/ B6/F6
PDR	R/W	Processor Diagnostic Register	A/B/C/D	1C	8	39/79/ B9/F9
PCR	R/W	Processor Control Register	A/B/C/D	1D	9	3A/7A/ BA/FA
IMR	R/W	Interrupt Mask Register	A/B/C/D	1E	0	3C/7C/ BC/FC
LSP	R/W	Local Storage Page	A/B/C/D	1F	1	3F/7F/ BF/FF

Read Data Flow and Read Control Card (01A-A1S2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	ess Dec	XRA Value
RCR	R/W	Read Control Register	B	02	2	45
RSR	R	Read Status Register	B	03	3	46
RER	R	Read Error Register	B	04	4	49
RRC	R	Read Residual Count	B	05	5	4A
RPR	R	Read Pattern Register	B	06	6	4C
RDC	R/W	Read Diagnostic Control	B	07	7	4F

Status Store Card (01A-A1G2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	ess Dec	XRA Value
CCC	R/W	Channel Card Control	A	00	0	00
CCA	R/W	Channel Card Address	A	01	1	03
CDR	R/W	Channel Data Register	A	02	2	05
CER	R	Channel Error Register	A	03	3	06
CMR	W	Channel Modifier Register	A	03	3	06
CRR	R	Channel Request Register	A	07	7	0F
CAE	R	Channel Adapter Error				
CAS	R	Channel Adapter Status	These registers are not directly addressable, but can be displayed by using the Support Diskette.			

Write Data Flow Card (01A-A1P2)

MNEM	Register Type	Register Name	XR Page	Addr Hex	ess Dec	XRA Value
WCR	R/W	Write Control Register	B	00	0	40
WSE	R	Write Status/Error	B	01	1	43

Cross-Reference Tables (Continued)

XRA Value to Register Name Cross-Reference Table

XRA Value	Register Name
00	Channel Card Control
03	Channel Card Address
05	Channel Data Register
06 (R)	Channel Error Register
06 (W)	Channel Modifier Register
0F	Channel Request Register
21	Device Level Register
22	Control Unit Serial High
24	Control Unit Serial Low
30	Interval Timer B
33	Interval Timer A
35	Processor Error Log
35	Jump Address Low
36 (R)	Processor Status Register
36 (W)	Jump Address High
39	Processor Diagnostic Register
3A	Processor Control Register
3C	Interrupt Mask Register
3F	Local Storage Page
40	Write Control Register
43	Write Status/Error
45	Read Control Register
46	Read Status Register
49	Read Error Register
4A	Read Residual Count
4C	Read Pattern Register
4F	Read Diagnostic Control
61	Device Interrupt Register
62	Interval Timer C
64	Device Control Register
67	Device Status/Error
68	Device Control Bus
6B	Device Tag Register
6D	Device Secondary Clock
6E	Device Secondary Register
70	Interval Timer B
73	Interval Timer A
75	Processor Error Register
75	Jump Address Low
76 (R)	Processor Status Register
76 (W)	Jump Address High
79	Processor Diagnostic Register
7A	Processor Control Register
7C	Interrupt Mask Register
7F	Local Storage Page
A1	Maintenance Tag In
A2	Maintenance Tag Out
A4	Maintenance Data In
A7	Maintenance Data Out
B0	Error Register A
B3	External Register Address
B5 (R)	Processor Error Register
B5 (W)	Jump Address Low
B6 (R)	Processor Status Register
B6 (W)	Jump Address High
BA	Processor Control Register
BC	Interrupt Mask Register
BF	Local Storage Page
C0	Buffer Channel Pointer High
C3	Buffer Channel Pointer Low
C5	Buffer Device Pointer High
C6	Buffer Device Pointer Low
C9	Buffer Channel Stop High
CA	Buffer Channel Stop Low
CC	Buffer Device Stop High
CF	Buffer Device Stop Low
D1	Buffer Wrap
D2	Buffer Channel Command
D4	Buffer Channel Status/Error
D7	Buffer Channel Remainder
D8	Buffer Channel SARS
DB	Buffer Channel Pad Counter
DD	Buffer Device Command
DE	Buffer Device Status/Error
E1	Buffer Device Remainder
E2	Buffer Device SARS
F0	Error Register B
F3	External Register Address
F5 (R)	Processor Error Register
F5 (W)	Jump Address Low
F6 (R)	Processor Status Register
F6 (W)	Jump Address High
FA	Processor Control Register
FC	Interrupt Mask Register
FF	Local Storage Page

Buffer Adapter Registers

XRA Value	Register Name
E4	Buffer Data Not Real
EB	Buffer Diagnostic 0
ED	Buffer Diagnostic 1
EE	Buffer Mode Register

Buffer Adapter Registers with the 4.5 Mb/s Channel or Improved Data Recording Capability

XRA Value	Register Name
E4	Diagnostic Data
E7	Register Select
E8	Register Page
EB	Status
ED	Mode
EE	Channel Mode

Note: These registers replace the buffer adapter registers when the Improved Data Recording Capability 4.5 Mb/s buffer adapter card is installed.

External Registers (Continued)

Cross-Reference Tables (Continued)

XRA Value to Register Name Cross-Reference Table

XRA Value	Register Name
00	Channel Card Control
03	Channel Card Address
05	Channel Data Register
06 (R)	Channel Error Register
06 (W)	Channel Modifier Register
0F	Channel Request Register
21	Device Level Register
22	Control Unit Serial High
24	Control Unit Serial Low
30	Interval Timer B
33	Interval Timer A
35	Processor Error Log
35	Jump Address Low
36 (R)	Processor Status Register
36 (W)	Jump Address High
39	Processor Diagnostic Register
3A	Processor Control Register
3C	Interrupt Mask Register
3F	Local Storage Page
40	Write Control Register
43	Write Status/Error
45	Read Control Register
46	Read Status Register
49	Read Error Register
4A	Read Residual Count
4C	Read Pattern Register
4F	Read Diagnostic Control
61	Device Interrupt Register
62	Interval Timer C
64	Device Control Register
67	Device Status/Error
68	Device Control Bus
6B	Device Tag Register
6D	Device Secondary Clock
6E	Device Secondary Register
70	Interval Timer B
73	Interval Timer A
75	Processor Error Register
75	Jump Address Low
76 (R)	Processor Status Register
76 (W)	Jump Address High
79	Processor Diagnostic Register
7A	Processor Control Register
7C	Interrupt Mask Register
7F	Local Storage Page
A1	Maintenance Tag In
A2	Maintenance Tag Out
A4	Maintenance Data In
A7	Maintenance Data Out
B0	Error Register A
B3	External Register Address
B5 (R)	Processor Error Register
B5 (W)	Jump Address Low
B6 (R)	Processor Status Register
B6 (W)	Jump Address High
BA	Processor Control Register
BC	Interrupt Mask Register
BF	Local Storage Page
C0	Buffer Channel Pointer High
C3	Buffer Channel Pointer Low
C5	Buffer Device Pointer High
C6	Buffer Device Pointer Low
C9	Buffer Channel Stop High
CA	Buffer Channel Stop Low
CC	Buffer Device Stop High
CF	Buffer Device Stop Low
D1	Buffer Wrap
D2	Buffer Channel Command
D4	Buffer Channel Status/Error
D7	Buffer Channel Remainder
D8	Buffer Channel SARS
DB	Buffer Channel Pad Counter
DD	Buffer Device Command
DE	Buffer Device Status/Error
E1	Buffer Device Remainder
E2	Buffer Device SARS
F0	Error Register B
F3	External Register Address
F5 (R)	Processor Error Register
F5 (W)	Jump Address Low
F6 (R)	Processor Status Register
F6 (W)	Jump Address High
FA	Processor Control Register
FC	Interrupt Mask Register
FF	Local Storage Page

Buffer Adapter Registers

XRA Value	Register Name
E4	Buffer Data Not Real
EB	Buffer Diagnostic 0
ED	Buffer Diagnostic 1
EE	Buffer Mode Register

4.5 Mb/s Buffer Adapter Registers

XRA Value	Register Name
E4	Diagnostic Data
E7	Register Select
E8	Register Page
EB	Status
ED	Mode
EE	Channel Mode

Note: These registers replace the buffer adapter registers when the 4.5 Mb/s buffer adapter card is installed.

BCPH Register

- Type = Read/Write
- Card = 01A-A1L2
- XRA Value = C0

The Buffer Channel Pointer High (BCPH) register provides the high order half of the address used for channel storage cycles. It is incremented at the end of each channel storage cycle, except the last channel storage cycle, at the completion of Store CRC and Loop Write to Read operations. It is initialized before starting a Buffer Channel Side operation. The BCPH register is reset by Power-On-Reset (POR).

BCPL Register

- Type = Read/Write
- Card = 01A-A1L2
- XRA Value = C3

The Buffer Channel Pointer Low (BCPL) register provides the low order half of the address used for channel storage cycles. It is incremented at the end of each channel storage cycle, except the last channel storage cycle, at the completion of Store CRC and Loop Write to Read operation. It is initialized before starting a Buffer Channel Side operation. The BCPL register is reset by POR.

BCSE Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = D4

The Buffer Channel Status and Error (BCSE) register is used to indicate channel status and error conditions.

Note: All cards referenced by this table are on the 01A gate. To display the BCSE register, see "Register Display/Alter" on SDISK 1.

Bits 0-3 have the same meaning for all four channel groups.
Bits 4-7 (BCSE0) = Channel Error Group 0
Bits 4-7 (BCSE1) = Channel Error Group 1
Bits 4-7 (BCSE2) = Channel Error Group 2
Bits 4-7 (BCSE3) = Channel Error Group 3

Bit	Label	Description/Detail
0	Channel Pointer Equals Stop	A status condition set during a channel store cycle when buffer control detects that the last byte in the buffer has transferred for this channel data transfer operation.
1	Channel Stop	A status condition set after a Channel Stop condition is received from the buffer adapter card during channel read or write operations. Set after a Device Read End condition is received from the read data flow during a Loop to Read operation.
2	Microprocessor Write Complete	A status condition set after the data in the channel RAM containing the two CRC bytes has been stored.
3	Sample Channel Errors (This is a status condition.)	When set, enables the Channel Error Group pointer so that following each read of the BCSE register, the contents of the BCSE register are updated to the next error group. The first read of the BCSE register shows the errors for Error Group 0, the second read for Error Group 1, the third read for Error Group 2, and the fourth read for Error Group 3. The operation then is repeated.
4-7	Channel Errors	Bits 4 through 7 represent errors in each of the four error groups and change meaning for each group. Bits 4-7 of the BCSE register comes from Bits 0-3 of the CEGO, CEG1, CEG2, and CEG3 register respectively. Error groups are identified by the Channel Error Group Pointer. Channel Error Group 0 (CEG0): Bit 4 = Any channel error Bit 5 = Channel overrun Bit 6 = Channel Adapter to Buffer Adapter Parity Error Bit 7 = Buffer Control to Channel Adapter Parity Error Channel Error Group 1 (CEG1): Bit 4 = Buffer Control - FRU114 (A1L2), FRU120 (A1K2) Bit 5 = Buffer Adapter - FRU120 (A1K2), FRU114 (A1L2) Bit 6 = Buffer Memory - FRU112 (A1M2); FRU113 (A1N2) Bit 7 = Host/Channel Adapter Channel Error Group 2 (CEG2): Bit 4 = Channel Buffer Memory Address Parity Error Bit 5 = Buffer Memory Address Pointer Parity Error Bit 6 = Channel Buffer Memory Data Correctable Error Bit 7 = Channel Buffer Memory Data Uncorrectable Error Channel Error Group 3 (CEG3): Bit 4 = Buffer Adapter to Buffer Control Channel Data Bus Parity Error Bit 5 = Buffer Control Channel RAM Data Parity Error Bit 6 = Channel CRC Error Bit 7 = Not used

BCSS Register

- Type = Read/Write
- Card = 01A-A1L2
- XRA Value = D8

The Buffer Channel SARS (BCSS) register provides the addressing for the intermediate channel storage, for any data transfers between the channel storage and the buffer channel side interfaces (host processor). It is incremented each time a byte of data is read from, or written into the channel storage via one of the buffer channel side interfaces. The BCSS register is reset with a hardware or channel control reset.

BDSE Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = DE

The Buffer Device Status and Error (BDSE) register shows drive status and error conditions.

Note: All cards referenced by this table are on the 01A gate. To display the BDSE register, see "Register Display/Alter" on SDISK 1.

Bits 0-3 have the same meaning for all four device groups.
Bits 4-7 (BDSE0) = Device Error Group 0
Bits 4-7 (BDSE1) = Device Error Group 1
Bits 4-7 (BDSE2) = Device Error Group 2
Bits 4-7 (BDSE3) = Device Error Group 3

Bit	Label	Description/Detail
0	Device Pointer Equals Stop	A status condition set during a device store cycle when buffer control detects that the last data byte has been transferred for this device data transfer.
1	Device Read End	A status condition set after a Device Read End is received from the Read Data Flow.
2	Device Data Transfer Complete	A status condition set after the CRC bytes have been processed through the Device CRC Checker during a write operation. Is also set after the data in the device RAM, containing the two CRC bytes, has been stored during a Read and Store CRC operation.
3	Sample Device Errors (This is a status condition.)	When set, enables the Device Error Group pointer, so that following each read of the BDSE register, the contents of the BDSE register are updated to the next error group. The first read of the BDSE register shows the errors for Error Group 0, the second read for Error Group 1, the third read for Error Group 2, and the third read for Error Group 3. The operation then is repeated.
4-7	Device Errors	Bits 4 through 7 represent errors in each of the four error groups and change meaning for each group. Bits 4-7 of the BDSE register comes from Bits 0-3 of the CEG0, CEG1, CEG2, and CEG3 register respectively. Error groups are identified by the Device Error Group Pointer. Device Error Group 0 (DEG0): Bit 4 = Any device error Bit 5 = Device Data Overrun Bit 6 = Read Data Flow to Buffer Adapter Parity Error Bit 7 = Buffer Control to Buffer Adapter Device Data Bus Parity Error Device Error Group 1 (DEG1): Bit 4 = Buffer Control - FRU114 (A1L2) Bit 5 = Buffer Adapter - FRU120 (A1K2) Bit 6 = Buffer Memory - FRU112 (A1M2) Bit 7 = Read Data Flow Device Error Group 2 (DEG2): Bit 4 = Device Buffer Memory Address Parity Error Bit 5 = Device Buffer Memory Address Pointer Parity Error Bit 6 = Device Buffer Memory Data Correctable Error Bit 7 = Device Buffer Memory Data Uncorrectable Error Device Error Group 3 (DEG3): Bit 4 = Buffer Adapter to Buffer Control Data Bus Parity Error Bit 5 = Buffer Control Device RAM Data Parity Error Bit 6 = Device CRC Error Bit 7 = Not used

BDG0 Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = EB

Buffer Diagnostic 0 (BDG0) register is used for diagnostic purposes.

Bit	Label	Description/Detail
0	Shift Gate Select 0	Used to select one of eight scan paths on the BC card when the Shift Gate Enable bit equals a one, or one of two paths on the BA card when the Shift Gate Enable bit equal zero.
1	Shift Gate Select 1	See Bit 0.
2	Shift Gate Select 2	See Bit 0.
3	Shift Gate Enable	Used to start a scan operation on the BC card when the bit is set to a one.
4	Enable Correctable Error Status	When set to a one, enables the correctable error status to be put into the BCSE register.
5	Read End	When set to a one, issues a Read End Tag in diagnostic mode.
6	Device Side Diagnostic	When set to a one, causes a drive operation in diagnostic mode.
7	Channel Side Diagnostic	When set to a one, causes a channel operation in diagnostic mode.

BDG1 Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = ED

The Buffer Diagnostic 1 (BDG1) register is used with diagnostic mode.

Bit	Label	Description/Detail
0	Scan Out Data (Read Only)	Used to sample the Scan Out Data from the BC card.
0	Scan In Data (Write Only)	Used for diagnostic scans of the BC card.
1	Service In (Read Only)	Samples the Service In tag. A value of one indicates that the Service In tag is active.
1	Scan Clock A (Write Only)	When set to a one, permits 'LSSD scan A clock' line to scan data for the BC card.
2	Data In (Read Only)	When set to a one, indicates that the Data In tag is active.
2	Scan Clock B (Write Only)	When set to a zero, permits 'LSSD scan B clock' line to scan data for the BC card.
3	Write End (Read Only)	When set to a one, indicates that the Write Data Flow End tag is active.
3	Disable ECC (Write Only)	When set to a one, disables buffer storage error correction.
4	Service Out	When set to a one, causes a Service Out tag in diagnostic mode to be sent.
5	Data Out	When set to a one, causes a Data Out tag in diagnostic mode to be sent.
6	Stop Out	When set to a one, causes a Stop Out tag in diagnostic mode to be sent.
7	Suppress Out	When set to a one, causes a Suppress Out tag in diagnostic mode to be sent.

BDPH Register

- Type = Read/Write
- Card = 01A-A1L2
- XRA Value = C5

The Buffer Device Pointer High (BDPH) register provides the high order half of the address used for drive channel storage cycles. It is incremented at the end of each drive storage cycle, except the last drive storage cycle, at the completion of a Read Data Flow operation. It is initialized before starting a Buffer Device Side operation. The BDPH register is reset by Power-on-Reset (POR).

Bit	Label	Description/Detail
0	Select Channel Adapter A	Specifies which of the channel adapters is to be selected.
1	Select Channel Adapter B	See Bit 0.
2	Select Channel Adapter C	See Bit 0.
3	Select Channel Adapter D	See Bit 0.
4	Device Address 8	Specifies which device address is to be used, or a displacement into a page of RAM.
5	Device Address 4	See Bit 4
6	Device Address 2	See Bit 4.
7	Device Address 1	See Bit 4.

BDPL Register

- Type = Read/Write
- Card = 01A-A1L2
- XRA Value = C6

The Buffer Device Pointer Low (BDPL) register provides the low order half of the address used for drive channel storage cycles. It is incremented at the end of each drive storage cycle, except the last drive storage cycle, at the completion of a Read Data Flow operation. It is initialized before starting a Buffer Device Side operation. The BCPL register is reset by a Power-on-Reset.

BWRP Register

- Type = Read/Write
- Card = 01A-A1L2
- XRA Value = D1

Bits 0-3 of the Buffer Wrap (BWRP) register control the setting of fixed 16, 32, 64, or 128K byte storage segments for Buffer Channel Side operations. Bits 4-7 control the setting of fixed 16, 32, 64, or 128K byte storage segments for Buffer Device Side operations. This register is reset by a Power-On-Reset.

Bit	Label	Description/Detail
0	Channel 128 K-byte Segment	Buffer Channel Side Operation
1	Channel 64 K-byte Segment	Buffer Channel Side Operation
2	Channel 32 K-byte Segment	Buffer Channel Side Operation
3	Channel 16 K-byte Segment	Buffer Channel Side Operation
4	Device 128 K-byte Segment	Buffer Device Side Operation
5	Device 64 K-byte Segment	Buffer Device Side Operation
6	Device 32 K-byte Segment	Buffer Device Side Operation
7	Device 16 K-byte Segment	Buffer Device Side Operation

External Register Bit Definitions (Continued)

CAE Register

The Channel Adapter Error (CAE) register is not a channel external register in the sense that it cannot be read directly. To get the data from the adapter error register you must transfer the data to an external register that can be read directly.

For the procedures, do the following steps (see "Register Display/Alter" on SDISK 1).

To read the CAE:

1. Set the channel card control (CCC) register to hexadecimal:

   85 for channel adapter A
   45 for channel adapter B
   25 for channel adapter C
   15 for channel adapter D

2. Set the channel card address (CCA) register to hexadecimal D3 to write the CAE into the channel adapter RAM.

3. Set the channel card address register to hexadecimal C3 to write the CAE into the channel data register (CDR).

4. Read the channel data register to get the contents of the CAE.

Bit	Definition
0	Multi-tag error
1	Channel adapter RAM write parity error
2	Channel adapter RAM read parity error
3	Buffer-data-in parity error
4	Channel adapter to status store data parity error
5	Channel adapter to status store response parity error
6	Status store to channel adapter data parity error
7	Status store to channel adapter response parity error

Note: There is one CAE register in each channel adapter. When an error occurs on channel adapter A, bit 4 of the CER register is set. Channel adapter B errors sets bit 5, and so on (see "CER Register" on DF 35).

External Register Bit Definitions (Continued) DF 33

CAS Register

The Channel Adapter Status (CAS) is a read only register. It is displayed by channel orders using the MD support diskette (see "Channel RAM Display" on SDISK 1). The CAS register is located on the channel adapter card for the channel adapter that is selected.

01A-A2C2 for channel adapter A
01A-A2D2 for channel adapter B
01A-A2E2 for channel adapter C
01A-A2F2 for channel adapter D

The Channel Adapter Status (CAS) register has the following bit definitions.

Bit	Label	Description/Detail
0	CA Offline	Bit 0 is active when the Power-On-Reset (POR) signal to the respective channel adapter shoe card is active. It means that the shoe card drivers are not on.
1	Offline Switch	Bit 1 is active when the Enable/Disable switch for the respective channel adapter on the operators panel is in the disabled position.
2-4	Channel Mode Switches	The Channel Mode Switch bits are set to the value of the three high order bits of the low order hex digit of the address switches (bits 4-6) on the operators panel. The bits are used by the microcode to control the operation mode of control unit buffer during data transfer mode.
5	Address Switch Parity Bad	Bit 5 is active when even parity is detected on the control unit address switches (high order hex digit and low order bit of the low order hex digit (bits 0-3, 7).
6	Collision Detected	Bit 6 is set if both control units in a two control unit subsystem have activated the collision detection hardware circuits. When Collision Detected is on, the 'adapters failure' to status store. This causes the failing channel adapter's bit to be set in the Channel Error Register (CER). Check 2 error and a level 6 interrupt then become active.
7	Reserved	

CCA Register

- Type = Read/Write
- Card = 01A-A1G2
- XRA Value = 03

The Channel Card Address Register (CCA) is used to present orders to the status store or channel adapter areas.

CCC Register

- Type = Read/Write
- Card = 01A-A1G2
- XRA Value = 00

The Channel Card Control (CCC) register is used by the microcode to control the selection of the channel adapters and specify the address that is to be used. It is also used with the CCA register.

Bit 0 selects channel adapter A
Bit 1 selects channel adapter B
Bit 2 selects channel adapter C
Bit 3 selects channel adapter D
Bits 4-7 specify the channel adapter RAM page.

CER Register

- Type = Read
- Card = 01A-A1G2
- XRA Value = 06

The Channel Error Register (CER) contains pointers to errors detected by the status store or channel adapter areas.

Notes:

1. Any active channel error register bit sets a Check 2 error.
2. All cards referenced by this table are on the 01A gate.

Bit	Label	Description/Detail
0	Status Store Basic Card Parity Error	Basic register parity check (internally checked). Status store basic (SSB) card - FRU121 (A1G2)
1	Status Store Communication Card Parity Error	Status store communication parity check (data from status store communication register to status store communication card checked). Status store communication (SCC) card - FRU122 (A1F2)
2	SSC Card to SSB Card Transfer Error	Remote control unit control transfer error (status store communication card to status store basic card).
3	XR Data Bus Parity Error	XR data parity error. XR data from the microprocessor card had bad parity. Microprocessor - FRU117 (A1D2)
4	Channel Adapter A Detected Error	Register parity check transfer error. Data from the channel adapter register to the status store card (A1G2) had bad parity. Channel Adapter A - FRU133 (A2C2)
5	Channel Adapter B Detected Error	Register parity check transfer error. Data from the channel adapter register to the status store card (A1G2) had bad parity. Channel Adapter B - FRU152 (A2D2)
6	Channel Adapter C Detected Error	Register parity check transfer error. Data from the channel adapter register to the status store card (A1G2) had bad parity. Channel Adapter C - FRU195 (A2E2)
7	Channel Adapter D Detected Error	Register parity check transfer error. Data from the channel adapter register to the status store card (A1G2) had bad parity. Channel Adapter D - FRU196 (A2F2)

Note: After the failing channel has been identified by the CER register bits 4-7, see "CAE Register" on DF 33 for more details.

CHM Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = EE

The CHM register is used to set the channel mode. Only microcode can change the contents of this XR through an XR write operation. This register is reset by a hardware reset.

Bit	Label	Description/Detail
0	Bytes in Flight 0	See Bit 1
1	Bytes in Flight	These two bits determine the maximum number of outstanding in tag requests that are permitted. Bits 0-1 In Tag Bits Count 00 15 01 31 10 63 11 127
2	Channel Timer 0	See Bit 3
3	Channel Timer 1	These two bits determine the maximum amount of time the buffer adapter waits for an out tag before setting a channel overrun error. If the timer is disabled, a channel overrun error cannot be set. Channel Time Timer 0-1 Selected 00 Disabled 01 16 us 10 64 us 11 256 us
4	Channel Group	This bit determines the group of channel adapters (local or remote) through which a channel data transfer takes place. Bit On = Remote Bit Off = Local
5	Channel Mode 1	See bit 7
6	Channel Mode 2	See bit 7
7	Channel Mode 3	These three bits determine the channel data transfer rate and mode. Channel Mode 0-2 Channel Mode 000 1.5 Mb/s Interlock (Service in first) 001 1.5 Mb/s Interlock (Data in first) 010 1.5 Mb/s Streaming 011 2.0 Mb/s Streaming 100 3.0 Mb/s Streaming 101 Reserved 110 4.5 Mb/s Streaming 111 Reserved

CMDT Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = E4

The CMDT register is used for diagnostic data transfers between the microprocessor and the buffer adapter, or buffer controller. The CMDT is reset to X'00' by a channel control reset.

CMM Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = ED

The CMM register is used to set the operation mode for the 4.5 Mb/s Buffer Adapter Card.

Bit	Label	Description/Detail
0	Reserved	Can be written or read for diagnostic purposes
1	Reserved	Can be written or read for diagnostic purposes
2	Diagnostic Mode 0	Bits 2 and 3 set the diagnostic mode
3	Diagnostic Mode 1	00 = No Diagnostics 01 = Reserved 10 = Buffer Channel Diagnostics 11 = Buffer Device Diagnostics
4	Maintain Separation	This bit is set for the Maintain Separation command.
5	Force 300 ns Clock Ring Error	When this bit is set it causes the 300 ns clock ring to go out of synchronization causing the 300 ns clock ring error to be set.
6	Force Toggle Feature Parity Error	When this bit is set the feature switch parity is defined as even and forces a feature switch parity error. When this bit is off the feature switch parity is defined as odd.
7	Pseudo Buffer End	This bit is set after receiving a buffer control interrupt at the end of a data transfer.

CMRP Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = E8

The CMRP register is the microcode interface for reading and writing the 4.5 Mb/s channel adapter internal registers. These registers are addressable by the page and register number in the CMRS register. The CMRP register holds the data of the register addressed by the CMRS register.

4.5 Mb/s Buffer Adapter Register Pages

Page #	CMRS Bits 1 - 3	# Regs Per Page	Type	Description
0	000	0	NA	Reserved
1	001	0	NA	Reserved
2	010	4	R	C2P0 Error and Feature Level Registers
3	011	0	NA	Reserved
4	100	0	NA	Reserved
5	101	2	R/W	Buffer Adapter Diagnostic Registers
6	110	0	NA	Reserved
7	111	0	NA	Reserved

The above figure lists the buffer adapter register pages with their respective page addresses (CMRS XR bits 1-3). The desired register address within the page must be specified by writing CMRS XR, bits 4-7.

CHM Register

- Type = Read/Write
- Card = 01A-A1K2 (with 4.5 Mb/s Channel or Improved Data Recording Capability features)
- XRA Value = EE

The CHM register is used to set the channel mode. Only microcode can change the contents of this XR through an XR write operation. This register is reset by a hardware reset.

Bit	Label	Description/Detail
0	Bytes in Flight 0	See Bit 1
1	Bytes in Flight	These two bits determine the maximum number of outstanding in tag requests that are permitted. Bits 0-1 In Tag Bits Count 00 15 01 31 10 63 11 127
2	Channel Timer 0	See Bit 3
3	Channel Timer 1	These two bits determine the maximum amount of time the buffer adapter waits for an out tag before setting a channel overrun error. If the timer is disabled, a channel overrun error cannot be set. Channel Timer 0-1 Time Selected 00 Disabled 01 16 us 10 64 us 11 256 us
4	Channel Group	This bit determines the group of channel adapters (local or remote) through which a channel data transfer takes place. Bit On = Remote Bit Off = Local
5	Channel Mode 1	See bit 7
6	Channel Mode 2	See bit 7
7	Channel Mode 3	These three bits determine the channel data transfer rate and mode. Channel Mode 0-2 Channel Mode 000 1.5 Mb/s Interlock (Service in first) 001 1.5 Mb/s Interlock (Data in first) 010 1.5 Mb/s Streaming 011 2.0 Mb/s Streaming 100 3.0 Mb/s Streaming 101 3.7 Mb/s Streaming 110 4.5 Mb/s Streaming 111 Reserved

CMDT Register

- Type = Read/Write
- Card = 01A-A1K2 (with the Improved Data Recording Capability feature)
- XRA Value = E4

The CMDT register is used for diagnostic data transfers between the microprocessor and the buffer adapter, or buffer controller. The CMDT is reset to X'00' by a channel control reset.

CMM Register

- Type = Read/Write
- Card = 01A-A1K2 (with the 4.5 Mb/s Channel or Improved Data Recording Capability features)
- XRA Value = ED

The CMM register is used to set the operation mode for the Buffer Adapter Card.

Bit	Label	Description/Detail
0	Improved Data Recording Capability	This bit turns on Improved Data Recording Capability Format.
1	Ram Write/Read	When set to 1, this bit specifies that the RAM selected for the Comp Ram Diagnostic is to be written. When set to 0, the selected RAM is read.
2	Diagnostic Mode 0	Bits 2 and 3 set the diagnostic mode
3	Diagnostic Mode 1	00 = No Diagnostics 01 = Buffer RAM Diagnostic 10 = Buffer Channel Diagnostics 11 = Buffer Device Diagnostics
4	Maintain Separation	This bit is set for the Maintain Separation command.
5	Force 300 ns Clock Ring Error	When this bit is set it causes the 300 ns clock ring to go out of synchronization causing the 300 ns clock ring error to be set.
6	Force Toggle Feature Parity Error	When this bit is set the feature switch parity is defined as even and forces a feature switch parity error. When this bit is off the feature switch parity is defined as odd.
7	Pseudo Buffer End	This bit is set after receiving a buffer control interrupt at the end of a data transfer.

CMRP Register

- Type = Read/Write
- Card = 01A-A1K2 (with 4.5 Mb/s Channel or Improved Data Recording Capability features)
- XRA Value = E8

The CMRP register is the microcode interface for reading and writing the channel adapter internal registers. These registers are addressable by the page and register number in the CMRS register. The CMRP register holds the data of the register addressed by the CMRS register.

Buffer Adapter Register Pages

Page #	CMRS Bits 1 - 3	# Regs Per Page	Type	Description
0	000	16	R	Comp 0 through Comp 3 Channel Byte Count Registers
1	001	0	NA	Reserved
2	010	3	R	C3P0 Error and Feature Level Registers
3	011	8	NA	Comp 0 through Comp 3 Error Registers
4	100	0	NA	Reserved
5	101	2	R/W	Buffer Adapter Diagnostic Registers
6	110	4	NA	Comp 0 through Comp 3 Diagnostic Registers
7	111	4	NA	Comp 0 through Comp 3 Configuration Registers

The above figure lists the buffer adapter register pages with their respective page addresses (CMRS XR bits 1-3). The desired register address within the page must be specified by writing CMRS XR, bits 4-7.

0 0 0 0 0 0 0 0 0 0

CMRS Register

- Type = Read/Write
- Card = 01A-A1K2 (with 4.5 Mb/s Channel or Improved Data Recording Capability features)
- XRA Value = E7

The CMRS register is the microcode interface for selecting and accessing registers on the 4.5 Mb/s or Improved Data Recording Capability buffer adapter card. These registers are organized into eight pages, and each page can contain up to 16 registers.

Bit	Label	Description/Detail
0	Auto increment CMRP register address	Setting this bit causes the CMRP register address to increment after each XR read of the CMRP XR.
1	CMRP page address 0	See bit 3.
2	CMRP page address 1	See bit 3.
3	CMRP page address 2	These bits select the CMRP register page to be accessed by either an XR read or write to the CMRP XR. There is a total of 8 CMRP register pages with a varying number of registers in each.
4	CMRP register address 0	See bit 7.
5	CMRP register address 1	See bit 7.
6	CMRP register address 2	See bit 7.
7	CMRP register address 3	These bits select the CMRP register to be accessed within a selected CMRP register page.

CMS Register

- Type = Read
- Card = 01a-A1K2 (with 4.5 Mb/s Channel or Improved Data Recording Capability features)
- XRA Value = EB

The CMS register is used to post status information and is synchronized to the MP interface so that it may be read by microcode at any time.

Bit	Label	Description/Detail
0	Comp Busy	Set when the Comps are busy initializing their respective Encoders and Decoders. Also set when Improved Data Recording Capability is on during a channel read or write.
1	Channel End	Set when the end data is detected during a channel read or a channel write.
2	Buffer Control End	Set when the buffer transfers the last byte of data to the buffer control.
3	Xfer Complete/Overrun	Set when stop out or end indications and out tags corresponding to all generated in tags have been received.
4	Channel Op Complete	Set when a channel operation is complete. Not set for a zero byte transfer.
5	4.5 Mb/s or Improved Data Recording Capability installed	This bit is set to 1 when the 4.5 Mb/s channel or Improved Data Recording Capability adapter card is installed.
6	Improved Data Recording Capability allowed	Improved Data Recording Capability is allowed when this bit is set to 1. In a dual control unit subsystem both control units must have the Improved Data Recording Capability feature installed before Improved Data Recording Capability can be allowed.
7	Any Error	Set by any of the error bits on CMRP register page 2.

0 0 0 0 0 0 0 0 0 0

CMRS Register

- Type = Read/Write
- Card = 01A-A1K2
- XRA Value = E7

The CMRS register is the microcode interface for selecting and accessing registers on the 4.5 Mb/s buffer adapter card. These registers are organized into eight pages, and each page can contain up to 16 registers.

Bit	Label	Description/Detail
0	Auto increment CMRP register address	Setting this bit causes the CMRP register address to increment after each XR read of the CMRP XR.
1	CMRP page address 0	See bit 3.
2	CMRP page address 1	See bit 3.
3	CMRP page address 2	These bits select the CMRP register page to be accessed by either an XR read or write to the CMRP XR. There is a total of 8 CMRP register pages with a varying number of registers in each.
4	CMRP register address 0	See bit 7.
5	CMRP register address 1	See bit 7.
6	CMRP register address 2	See bit 7.
7	CMRP register address 3	These bits select the CMRP register to be accessed within a selected CMRP register page.

CMS Register

- Type = Read
- Card = 01A-A1K2
- XRA Value = EB

The CMS register is used to post status information and is synchronized to the MP interface so that it may be read by microcode at any time.

Bit	Label	Description/Detail
0	Reserved	Always read as '0'.
1	Channel End	Set when the end data is detected during a channel read or a channel write.
2	Buffer Control End	Set when the buffer transfers the last byte of data to the buffer control.
3	Xfer Complete/Overrun	Set when the buffer has received stop out or end indications and has received out tags to correspond with all generated tags.
4	Channel Op Complete	Set when a channel operation is complete. Not set for a zero byte transfer.
5	4.5 Mb/s installed	This bit is set when the 4.5 Mb/s channel adapter card is installed.
6	Reserved	This bit is controlled by switch position 3 on the 4.5 Mb/s buffer adapter card and should be set to '0'.
6	Reserved	
7	Any Error	Set by any of the error bits on CMRP register page 2.

CRR Register

- Type = Read
- Card = 01A-A1G2
- XRA Value = 0F

The Channel Request Register (CRR) is used by status store to present status information about the channel adapter, status store, or message handling between the control units in a dual control unit subsystem.

Bit	Label	Description/Detail
0	Channel Adapter A Request	See Bit 3.
1	Channel Adapter B Request	See Bit 3.
2	Channel Adapter C Request	See Bit 3.
3	Channel Adapter D Request	These bits indicate that their respective channel adapter has met one of the following conditions: • The adapter is at the end of initial selection and status has been accepted by the channel. • The adapter has received a Halt I/O, Selective Reset, or System Reset from the channel.
4	Acknowledge	Indicates that the other control unit has acknowledged receipt of a message. This bit is reset when the microcode sends a Write Message Buffer order.
5	Received	Indicates that this control unit has received a message from the other control unit. This bit is reset when the microcode sends a Write Message Buffer order.
6	SS Order Ack	Indicates that the status store or the channel adapter has processed the order in the CCA register (A01). It is reset when register A01 is written into.
7	SS Response	Indicates that the status store or channel adapter has successfully processed the order that is in CCA register A01. This bit is valid only if bit 6 of this register is on.

DCB Register

- Type = Read/Write
- Card = 01A-A1Q2
- XRA Value = 68

The Device Control Bus (DCB) register is used to transfer information from the control unit microcode to the drive through 'bus out' using the Device Data Bus (DDB). It is also used to transfer information to the control unit microcode from the drive through 'bus in' using the DDB.

DCR Register

- Type = Read/Write
- Card = 01A-A1Q2
- XRA Value = 64

The Device Control Register (DCR) is used by the microcode to select and control the correct device lines.

Bit	Label	Description/Detail
0	Select Hi/Lo	When set to a zero, bit 0 gates the lines between the drive-adapter card and the drive (see Note), drivers and receivers. When set to a one, the (see Note) lines are gated to the drivers and receivers. The DCB and DTR registers are controlled by this bit. This bit is used also with bits 2 and 4.
1	Interrupt/ Secondary Select Hi/Lo	When set to a zero, permits the microcode to sense interrupts that are present (see Note). When set to a one, the interrupts (see Note) are sensed. The DIR register is controlled by this bit. When used as a secondary, and this bit is set to a zero, the serial data and clock are sent from the DSR and DSC register to the drives on the (see Note) interface. When set to a one, it is sent selected control unit (see Note). The DSR and DSC registers are controlled by this bit.
2	Enable Bus	When set to a one, permits the DCB register or write data flow, access to the device control bus. When set to a zero, the bus drivers are unconditionally disabled. The control unit that is enabled is controlled by DCR register bit 0.
3	ITD Enable	When set to a one, permits the DSC register, linked with the DSR register, to be used as an internal timer. It also degates the serial command and clock lines to the devices. When set to zero, the DSC and DSR registers operate as a serial interconnection.
4	Enable Write	When set to a one, with bit 2 also set to a one, permits the data from the write data flow, access to the drive control bus. When set to a zero, the write data flow does not have access to the drive control bus. DCR register bit 0 controls the control unit that is enabled.
5	ITC Time Out	When ITC equals zero. This bit will reset when a non- zero is set into the ITC.
6	ITD/Serial Command Complete	Set when the ITD or DSC contents equal zero. This occurs a the time of the timeout or after the secondary command has been sent to the drive. The bit resets when a non-zero value is set into the ITD register or a new secondary command is loaded into the DSR register.
7	Reset Repos	Sets the 'repositioning in latch'.

Note:

Single Control Unit Subsystem	Dual Control Unit Subsystem
Local = Control Unit 0 - Addr 0-7	Local = Control Unit 0 - Addr 0-7 Remote = Control Unit 0 - Addr 8-F Local = Control Unit 1- Addr 8-F Remote = Control Unit 1- Addr 0-7

DIR Register

- Type = Read
- Card = 01A-A1Q2
- XRA Value = 61

The Device Interrupt Register (DIR) is used to present interrupts from any drive to the microcode. An interrupting device causes its corresponding bit and the P bit to be set in the DIR register. The hardware sets an error if only the P bit is on.

Bit	Description
0	Interrupt from drive 0
1	Interrupt from drive 1
2	Interrupt from drive 2
3	Interrupt from drive 3
4	Interrupt from drive 4
5	Interrupt from drive 5
6	Interrupt from drive 6
7	Interrupt from drive 7

DLR Register

- Type = Read
- Card = 01A-A1Q2
- XRA Value = 21

The Device Level Register (DLR) contains miscellaneous information.

See the CARR section for the switch position assignments for the Drive Adapter Card (FRU118).

DSE Register

- Type = Read
- Card = 01A-A1Q2
- XRA Value = 67

The Device Status/Error (DSE) register shows device status and error conditions.

Note: All cards referenced by this table are on the 01A gate.

Bit	Label	Description/Detail
0	Drive Adapter-Card Parity Error	Bit 0 indicates that bad parity was detected by the drive adapter-card (A1Q2) on the device data bus (DDB). It is also used to permit interrupts from the drives to be signalled if the drive bus parity bit is on and no other drives bus lines are on.
1	Write Data Parity Error card	Bit 1 indicates that bad parity was detected on the MUX data path when the data was gated from the write data flow to the drive control bus. FRU116 (A1P2)
2	Drive Adapter-Card Parity Error	Bit 2 indicates that the device adapter-card had bad internal parity or there was an interrupt error. FRU118 (A1Q2)
3	Reserved	
4	Repositioning	Repositioning is used as a response to any serial sequence command that causes tape motion. It indicates that the drive is either repositioning or it is not at the command stoplock position.
5	Repositioning	Same as bit 4.
6	Reserved	
7	Reserved	

DTR Register

- Type = Read/Write
- Card = 01A-A1Q2
- XRA Value = 6B

The Device Tag Register (DTR) is used by the microcode to transfer control tags to and from the drive.

Bit	Label	Description/Detail
0	Select Out	Select Out is used to start the Initial Sequence to the drive and requires no response from the drive. Select Out must stay active during the complete connected part of the operation.
1	Address Out	Address Out is used to signal all the drives to decode the address that is on the bus. When the drive recognizes its address, its responds by placing its complement address on the bus and raising Address In.
2	Command Out	Command Out is a response to Address In during Initial sequence and indicates to the selected drive that the command on the bus is valid. Command Out stays active until Status In is received.
3	Clock A Out	Clock A Out is used during data transfer sequences and it is the odd parity of the nine data bits being transferred. During sense or control transfer sequences, Clock Out A is used as a response to Clock B In/Out. Clock A Out indicates to the selected drive that the control unit has accepted or provided the information on the bus that was requested by the drive generated Clock B In/Out line.
4	Gap In/Out	Gap In and Gap Out share a common bi-directional line. The microcode raises 'Gap Out' by writing in to the DTR register. The DTR register monitors the Gap In/Out line and raises Gap In for read operations.
5	Address In	Address In is used as a response to Address Out to indicate to the control unit that the address of the selected drive is valid. Address In is also used to indicate any error or unusual condition that is detected during a data transfer sequence.
6	Status In	Status In is used to indicate that the status information on the bus is valid. Status In is the response to Command Out during a Initial Sequence or a control unit ending sequence.
7	Clock B In	Clock B In/Out is a bi-directional line between the control unit and all attached drives. Its function is the same as Clock A Out.

ERA Register and ERAH (Holding)

ERA XR only

- Type = Read
- Card = 01A-A1D2
- XRA Value = B0

The ERAH is not a XR register, but it can be displayed using "CU Scan Rings - Error" (see SDISK 1).

Error register A (ERA) and error register B (ERB) are used to indicate check 1 error conditions. Normally, the processor is stopped before it reads the error registers. However, they can be read out using the support diskette Alter/Display program "CU Scan Rings" (see SDISK 1). The registers are also used to verify that the check 1 error detection circuits are working correctly.

ERAH is the holding register for the ERA register. If the check 1 error recovers on the retry operation, the ERAH or ERBH registers indicates the cause of the recovered check 1 error. If any bit is on in the ERA or ERB register, it means that the check 1 condition is a solid error and the ERA or ERB register(s) have meanings that are useful for troubleshooting.

Notes:

1. The ERA register does not include Check 1 errors that are caused by Forced Microcode Check 1 (PCR register, bit 5) errors.
2. All cards referenced by this table are on the 01A gate.
3. MD displays can indicate ERA and ERB as a single hex character field named 'ERAB'.
4. MD displays can indicate ERAH and ERBH as a single hex character field named 'HOLD'.

Bit	Label	Description/Detail
0	CS Data Parity Funnel Error	This bit is set when bad parity is detected in the micro- processor card (A1D2) on a word fetched from the control storage data bus or when the control storage source register indicates an invalid source.
1	Reg Source Funnel Error	This bit is set when the register source indicates an invalid source (valid sources are CS, LSR, JUMP, and XR registers). The error is inhibited until Initial Diagnostic Complete (PCR register bit 4) so that the microcode can initialize local storage. This is an internal error of the microprocessor card.
2	Microprocessor, Internal Data, or Clock Error	This bit is set when an error is detected by one of the three check latches in the microprocessor. 1. Control Storage Data Parity Error - Data transferred from the CS Data Bus to the Microprocessor or Data Bus. 2. Local Storage or External Register Data Parity Error - Data transferred from LS or XR Bus In to Microprocessor Data Bus In. 3. Registers internal to the microprocessor card have bad parity (even) or an invalid clock state (system clocks) was detected.
3	Current Interrupt Parity Error	This bit indicates that bad parity was detected in the 'current interrupt level' latches in the microprocessor card.
4	Processor Interrupt Level Parity Error	This bit indicates that bad parity was detected on the 'processor interrupt level' bus during an interrupt swap, in the microprocessor card.
5	LSR Address Parity Error	This bit indicates that bad parity was detected on the 'LSR selects and address' bus in the microprocessor card.
6	XR Address Parity Error	This bit indicates that bad parity was detected on the 'XR select and processor XR address' bus in the microprocessor card.
7	Processor Bus Out Parity Error	This bit indicates that bad parity was detected on 'processor bus out' during a register write operation. The error was detected in the microprocessor card.

ERB Register and ERBH (Holding)

ERB XR only

- Type = Read
- Card = 01A-A1D2
- XRA Value = F0

The ERBH is not a XR register, but it can be displayed using "CU Scan Rings - Error" (see SDISK 1).

Error register B (ERB) and error register A (ERA) are used to indicate check 1 error conditions. Normally, the processor is stopped before it reads the error registers. However, they can be read out using the support diskette Alter/Display program "CU Scan Rings" (see SDISK 1). The registers are also used to verify that the check 1 error detection circuits are working correctly.

ERBH is the holding register for the ERB register. If the check 1 error recovers on the retry operation, the ERBH or ERAH registers indicates the cause of the recovered check 1 error. If any bit is on in the ERB or ERA register, it means that the check 1 condition is a solid error and the ERB or ERA register(s) have meanings that are useful for troubleshooting.

Notes:

1. The ERA register does not include Check 1 errors that are caused by Forced Microcode Check 1 (PCR register, bit 5) errors.
2. All cards referenced by this table are on the 01A gate.
3. MD displays can indicate ERA and ERB as a single hex character field named 'ERAB'.
4. MD displays can indicate ERAH and ERBH as a single hex character field named 'HOLD'.

Bit	Label	Description/Detail
0	XR Address Compare Error	Set when the Processor XR Address bus bits 0-4 do not match the XR Address bus bits 0-4 (internal in the microprocessor card).
1	MP Register Error	Bad parity is detected in the IMR or PDR registers (internal in the microprocessor card).
2	Uncorrectable CS Read Error	The control storage error correction hardware detected an uncorrectable data word on a control storage fetch operation (error was detected by the CS card).
3	CS Address Parity Error	This bit indicates that bad parity was detected on the control storage address bus (error was detected by the CS card).
4	CS Refresh Error	This bit indicates that one of the three refresh error is in error (error was detected by the CS card).
5	Selection Check	This bit indicates that Multiple Card Selects was active (error was detected by the CS card).
6	Key Bit Check	The Key Bit Check bit indicates an error was detected from the control storage address bus parity bit (error was detected by the CS card).
7	CS Write Data Parity Error	This bit indicates that the data being written had bad parity (error was detected by the CS card).

MCR Register

The Maintenance Control Register (MCR) is not a readable register. The following description is for information only.

The four bits of the MCR register are set by individual MD commands. All bits are reset with a Reset MCR command.

The MCR is controlled by the "Microprocessor Control Utility," see SDISK 1.

Bit	Description
0	Ignore Errors
1	Address Compare Stop
2	Check Stop
3	Check 2 = Check 1
4	Address Compare Sync
5	Program Flag

MDI Register

- Type = Read
- Card = 01A-A1E2
- XRA Value = A4

The Maintenance Data In (MDI) register has two functions:

1. When Maintenance Tag Out (MTO) register bit 2 (Read XR Active) and Maintenance Tag In (MTI) register bit 4 (XR Address Error) both equal 1, this register defines the logic card that contains the external register at the time of an external register error.
2. When MTO bit 2 or MTI bit 4 does not equal 1, this register contains commands or data transferred between the functional microcode and the maintenance device; however, this data does not provide valid pointers to external register logic cards.

Diagnostic routines only display the MDI register when the register can define the logic card that contains the external register that was addressed at the time of the external register error.

Use the following procedure to read the contents of the MDI register.

1. Display the MTI register to verify that bit 4 equals 1. If Bit 4 does not equal 1, no further troubleshooting information can be read, even if the bit is turned on.
2. Display the MTO register to verify that bit 2 equals 1. If bit 2 does not equal 1, write hexadecimal 20 into the register to turn on bit 2.
3. Display the contents of the MDI register to determine the logic card that contains the external register that was addressed at the time of the external register error.

   To display the MDI register, see "Register Display/Alter" on SDISK 1.

Note: All cards referenced by this table are on the 01A gate.

Bit	Label	Description/Detail
0	Buffer Adapter	One of the following external registers was addressed during an external register error: BCPH, BCPL, BDPH, BDPL, BCSH, BCSL, BDSH, BDSL, BWRP, BCC, BCSE, BCR, BCSS, BCPC, BDC, BDSE, BDR, BDSS, BDAT, BDG0, BDG1, BMR, or BDAT. FRU114 (A1L2) FRU120 (A1K2)
1	Status Store	One of the following external registers was addressed during an external register error: CCC, CCA, CDR, CER, CMR, or CCR. FRU121 (A1G2)
2	Device Adapter	One of the following external registers was addressed during an external register error: DSH, DSL, DIR, DLR, ITC, DCR, DSE, DCB, DTR, DSC, or DSR. FRU118 (A1Q2)
3	Read Data Flow	One of the following external registers was addressed during an external register error: RCR, RSR, RER, RRC, RPR, or RDC. FRU119 (A1S2)
4	Microprocessor	One of the following external registers was addressed during an external register error: ITB, ERA, ERB, ITA, XRA, PER, JAL, PSR, JAH, PDR, PCR, IMR, or LSP. FRU117 (A1D2)
5	Write Data Flow	One of the following external registers was addressed during an external register error: WSE or WCR. FRU116 (A1P2)
6	Maintenance Adapter	One of the following external registers was addressed during an external register error: MTI, MTO, MDI, or MDO. FRU115 (A1E2)
7	Reserved	

MDO Register

- Type = Read/Write
- Card = 01A-A1E2
- XRA Value = A7

The Maintenance Data Out (MDO) register is used to transfer information between the microcode and the maintenance device.

MSB Register

- Type = Read
- Card = 01A-A1E2
- To display the MSB register, see "Microprocessor Control" on SDISK 1.

The Maintenance Status Byte (MSB) register contains the Maintenance Adapter and Microprocessor status.

Bit	Label	Description/Detail
0	Spare	
1	Status Modifier	This bit will always be off.
2	Extended Op in Progress	This bit indicates that the microprocessor is executing an Extended Op instruction (an instruction that requires more than one control storage fetch.
3	Address Compare Equal	This bit indicates a match between the compare address set by the Maintenance Device microcode and the control storage address that is referenced by the microprocessor.
4	Check 1 Hardware Error	This bit indicates a hard error in the microprocessor or other hardware circuits of this control unit.
5	MP Stopped	This bit is on if the microprocessor is stopped. The microprocessor may be stopped with a Stop MP command from the Maintenance Device, a Check 1 error condition, or by processor control.
6	Instruction Executed	This bit indicates to the microprocessor microcode that the microprocessor read an instruction from the control storage for execution during the last microprocessor cycle. This bit is used during a Force MP Instruction sequence to confirm the execution of the instruction before resetting force mode.
7	Error - MTI Status Stored	This bit indicates that error data is stored in the MTI register.

MTI Register

- Type = Read/Write
- Card = 01A-A1E2
- XRA Value = A1

The Maintenance Tag In (MTI) register controls the operation of the maintenance adapter (MA) and provides status and error conditions for the adapter and the subsystem.

To display the MTI register, see "Register Display/Alter" on SDISK 1.

Note: All cards referenced by this table are on the 01A gate.

Bit	Label	Description/Detail
0	Maintenance Adapter Request/Response	A status condition that indicates to the microprocessor that another byte of information is ready to be taken by the microprocessor, or that another byte of information can be received by the maintenance adapter. This bit also acknowledges microprocessor Status Out.
1	Data Transfer or MD Connection Busy	Bit 1 indicates a status condition that is active during all data transfers to and from the microprocessor or indicates that the MD byte transfer is in process.
2	Maintenance Device Enabled	A status condition that indicates that the maintenance device is on-line and enabled.
3	XR Address Bus Parity Error	The maintenance adapter card (A1E2) has detected bad parity on the XR address bus from the microprocessor card. FRU117 (A1D2)
4	XR Addressed Line Error	Either none or more than one XR addressed lines are active during an XR read or write cycle. External Register cards - FRU117 (A1D2); FRU115 (A1E2); FRU121 (A1G2); FRU120 (A1K2); FRU114 (A1L2); FRU116 (A1P2); FRU118 (A1Q2); FRU119 (A1S2)
5	MA Internal Card Error	The maintenance adapter card (A1E2) detected an error internal to the card. This can be caused by the MA card, bad clock lines to the MA card from the control store (CS) card (A1C2), or voltages to either card. FRU115 (A1E2); FRU134 (A1C2)
6	MD Parity Error	The maintenance adapter card detected bad parity on serial data in line from the maintenance device. FRU = Maintenance Device
7	Check 1	Indicates that a Check 1 occurred that has not been reset by a check or hardware reset.

External Register Bit Definitions (Continued)

MTO Register

- Type = Read/Write
- Card = 01A-A1E2
- XRA Value = A2

The Maintenance Tag Out (MTO) register is used by the microcode to control the operation of the maintenance adapter and report status and other information about the subsystem.

To display the MTO register, see "Register Display/Alter" on SDISK 1.

Bit	Label	Description/Detail
0	Not Used	
1	Wait Light	This bit is used by the microcode to indicate the amount of subsystem activity. Wait light blinks - Normal subsystem activity Wait light on continuous - No drive activity Wait light never on - subsystem in a loop or wait light circuitry problem (this is not a normal condition)
2	RD X/R Active	This bit gates the XR active latch to the MP.
3	Data Ready	This bit indicates that the data in the MDO register is ready to be transferred to the MD. For information only. Displaying the MTO register will change the values of bits 3-6.
4	MD Status Out	This bit indicates that the microcode needs the attention of the MD. For information only. Displaying the MTO register will change the values of bits 3-6.
5	Data Demand	This bit indicates that the microcode wants to send data to or receive data from the MA. For information only. Displaying the MTO register will change the values of bits 3-6.
6	Command/Data Received	This bit indicates to the MA that the MP has successfully received the command or data byte. For information only. Displaying the MTO register will change the values of bits 3-6.
7	Reserved	

PCR Register

- Type = Read/Write
- Card = 01A-A1D2
- XRA Value = BA

The microcode uses the Processor Control Register (PCR) to cause events or conditions to occur within the subsystem.

Bit	Label	Description/Detail
0	Force Interrupt	Forces an interrupt at levels 0 through 6, whichever is enabled. This directs the microcode to handle interrupts with more priority if they are not masked off. Interrupt priorities, high to low: Level 0 - Microprocessor of subsystem maintenance adapter Level 1 - Microprocessor (Timer) Level 2 and 3 - Read control Level 4 and 5 - Buffer control Level 6 - Status store Level 7 - All others Reset by the hardware automatically and will always read as a zero.
1	Return From Interrupt	Causes a PSW swap from the current level to the highest remaining level that has an interrupt pending. Reset by the hardware automatically and will always read as a zero.
2	Diagnostic Mode	When set, activates the 'diagnostic mode' line. Enables data with incorrect parity to be written to an external register. Prevents the MA from alerting the channel interface to disconnect during a check 1 condition.
3	Hardware Reset	When set, activates the hardware reset line. Causes all functional areas except the micro processor to initialize to a power-on condition. It is also forced active while power-on reset is active. Remains set for at least ten processor cycles.
4	Initial Diagnostic Complete	This bit is set by the microcode after the initial power-on diagnostics have successfully completed. Remains set until next power on sequence. Enables Reg Funnel Parity checker after all LSR locations have been initialized to good parity.
5	Forced Microcode Check 1	Activates the 'check 1' line when the microcode detects a non-recoverable error condition.
6	XR Address Extend 0	See Bit 7.
7	XR Address Extend 1	These two bits extend the XR addressing to 128 Read/Write registers. See 'External Register Addressing' on DF 3.

PER Register

- Type = Read
- Card = 01A-A1D2
- XRA Value = F5

The Processor Error Register (PER) contains status and error condition indicators.

Note: All cards referenced by this table are on the 01A gate.

Bit	Label	Description/Detail
0	MP Check 2	Set when a parity error is detected in the ITA/ITB timer registers (card A1D2). Reset by a check reset to the microprocessor, if the error no longer exists.
1	ITA/B = 0	Active if the ITA/ITB counter equals zero. When active, a level 1 (timer) interrupt is generated. Timer ITA/B is used by the microcode to time the different operations.
2	Collision Detect	Bit 2 on, indicates a problem in the dual control unit communication area. When one control unit attempts to communicate with the other control unit and does not receive a response, the control unit expecting the response causes bit 2 of the PER register in the control unit that did not respond to be set on. A microcode forced check 1 error is caused in the control unit that has PER register bit 2 on.
3	On-Line	Indicates the state of the online switch (one equals online).
4	XR Read Parity Error	Set if a read parity error is detected by the microprocessor card (A1D2) during an XR read operation. Reset by a Check Reset to the MA/MP. When active, causes XR Error and Check 2 to be set.
5	XR User Read Error	Set if the 'XR error ungated' line is active during an XR read operation. Reset by Check Reset to the MA/MP.
6	XR User Write Error	Set if the 'XR error ungated' line is active during an XR write operation. Reset by Check Reset to the MA/MP.
7	Normal Mode	Indicates the state of the Test/Normal switch. (1) for normal mode; (0) for test mode. See PANEL 1 for "Control Unit Switches and Indicators" for the function of the switch.

PRR Register

The Processor Reset Register (PRR) is used to send a check reset to any or all functional areas. Each functional area is assigned a particular bit in the register. When the register is written, the check reset line is activated and, if bit 3 is not active, all functional areas whose bit is active performs a check reset. This register is a virtual register (no hardware) and does not store what was written. It is always reset after the write is complete.

Bit	Label	Description/Detail
0	Drive-adapter	
1	Maintenance adapter/processor	
2	Status store/channel adapter	
3	Must be a zero for check reset	
4	Buffer (drive side)	
5	Buffer (channel side)	
6	Write data flow	
7	Read data flow	

PROCESSOR STATUS REGISTER

- Type = Read
- Card = 01A-A1D2
- XRA Value = 36, 76, B6, and F6

The Processor Status Register (PSR) contains status indicators pertinent to error conditions.

Bit	Label	Description/Detail
0	XR Error	This bit continuously samples the condition of the 'XR error latched' line and is set whenever any of the three XR Error bits (PER register bits 4, 5 or 6) are set. Once set, the bit remains set until a check reset is issued to the MA/MP functional area.
4	Check 2	This bit continuously samples the status of the 'Check 2 error' line. When a Check 2 condition exists, this bit will be active. See "External Registers Data Flow/Error Detection" in the OPER section for more information.

READ CONTROL REGISTER

- Type = Read/Write
- Card = 01A-A1S2
- XRA Value = 45

The Read Control Register (RCR) is used by the microcode to control the operation of the read data flow and condition it to do the needed read function.

Bit	Label	Description/Detail
0	Read Gate	This bit is used by the read detection circuits to gate the VFC from the write clock onto the read data. It becomes active when Gap In is sensed and reset at the end of the device operation.
1	Read LWR	This bit conditions the read detection circuits to perform a Loop-Write-to-Read LWR operation. It is used on a short LWR operation.
2	Read Condition	This bit is used to activate the read data flow. It becomes active at the time the read data flow should start detecting beginning sync and is reset at the end of the operation.
3	Inhibit External Pointers	This bit, when active, inhibits the ECC from processing any pointers other than ECC pointers.
4	Read/Write	This bit specifies the type of operation; one equals read and zero equals write. Bit 4 is set before the rise of read gate and must not change until the end of the operation.
5	Fwd/Bkwd	This bit is active for the same duration for read or write operations. It is on for a forward direction and off for a backward direction.
6	Gap Out Enable Command Complete	This bit permits 'Gap Out' to be set under the control of the microprocessor. 'Gap Out' is set with a fixed delay after 'End Sync' is sensed, or after BOB (without sensing the ending sync), ERG, or TM when IBG is sensed.
7	Density Enable	This bit permits the display of the density pattern being read. See bits 0-3 of the "RPR" on DF 80.

RDC Register

- Type = Read/Write
- Card = 01A-A1S2
- XRA Value = 4F

The Read Diagnostic Control (RDC) register controls the diagnostic status and functions of the read logic.

Bit	Label	Description/Detail
0 (See Note)	Select Tone	This bit, when a one, permits the microprocessor to read the tone zones in the Read Pattern Register (RPR). Zones A through F will appear in bit positions 0 through 5 respectively.
1 (See Note)	Select Amp Sense	This bit, when a one, permits the microprocessor to read the amp sense zones in the Read Pattern Register (RPR). Zones A through F will appear in bit positions 0 through 5 respectively.
2	Disable ECC	This bit, when a one, disables the error correction from being performed. This permits the data record to be read into the buffer uncorrected.
3	Check Character Read	This bit, when a one, causes all the characters read from the tape (including the four ECC check characters) to be sent to the buffer during data frames.
4	Disable Dead Track Threshold	This bit, when a one, disables dead-tracking that is due to persistent pointers.
5	Enable BOB Processing	This bit is set by the microcode when the read head is still in the IBG to enable the hardware part of BOB processing.
6	Inhibit Dropping Pointers	This bit, when a one, will not let the ECC drop the pointers.
7	ECC Diagnostic	This bit, when a one, passes ECC diagnostic information instead of data.

Note: When the state of bits 0 or 1 changes, the RPR must be reset before its new value can be used.

READ ERROR REGISTER

- Type = Read
- Card = 01A-A1S2
- XRA Value = 49

The microcode uses the Read Error Register (RER) to get the FRU information detected by the read data flow. All cards referenced by this table are on the 01A gate.

Bit	Label	Description/Detail
0	FRU0	Skew Buffer Zones A and B: This bit indicates that one of the following conditions has occurred: 1. Skew Buffer Hardware Error (card A2K2) - The error is determined by the demodulator module on the ECC card (A1R2). RER bit 5 is also activated. 2. The 'gate read cycle' lines from this card (A2K2) are not equal to the 'gate read cycle' lines from the other two Skew Buffer Hardware Error cards (A2L2 and A2M2). RER bit 7 is also activated. 3. The 'ROC equals zero' lines from this card (A2K2) are not equal to the 'ROC equals zero' lines from the other two Skew Buffer Hardware Error cards (A2L2 and A2M2). RER bit 7 is also activated. FRUs for condition 1: FRU123 (A2K2); FRU111 (A1R2); FRU119 (A1S2) FRUs for conditions 2 and 3: FRU123 (A2K2); FRU119 (A1S2)
1	FRU1	Skew Buffer Zones C and D: This bit indicates that one of the following conditions has occurred: 1. Skew Buffer Hardware Error (card A2L2) - The error is determined by the demodulator module on the ECC card (A1R2). RER bit 5 is also activated. 2. The 'gate read cycle' lines from this card (A2L2) are not equal to the 'gate read cycle' lines from the other two Skew Buffer Hardware Error cards (A2K2 and A2M2). RER bit 7 is also activated. 3. The 'ROC equals zero' lines from this card (A2L2) are not equal to the 'ROC equals zero' lines from the other two Skew Buffer Hardware Error cards (A2K2 and A2M2). RER bit 7 is also activated. FRUs for condition 1: FRU124 (A2L2); FRU111 (A1R2); FRU119 (A1S2) FRUs for conditions 2 and 3: FRU124 (A2L2); FRU119 (A1S2)
2	FRU2	Skew Buffer Zones E and F: This bit indicates that one of the following conditions has occurred: 1. Skew Buffer Hardware Error (card A2M2) - The error is determined by the demodulator module on the ECC card (A1R2). RER bit 5 is also activated. 2. The 'gate read cycle' lines from this card (A2M2) are not equal to the 'gate read cycle' lines from the other two Skew Buffer Hardware Error cards (A2K2 and A2L2). RER bit 7 is also activated. 3. The 'ROC equals zero' lines from this card (A2M2) are not equal to the 'ROC equals zero' lines from the other two Skew Buffer Hardware Error cards (A2K2 and A2M2). RER bit 7 is also activated. FRUs for condition 1: FRU125 (A2M2); FRU111 (A1R2); FRU119 (A1S2) FRUs for conditions 2 and 3: FRU125 (A2M2); FRU119 (A1S2)
3	Acceleration Check	This can be a normal condition. For some write conditions, the drive can have limited instantaneous speed variations (ISV), and when the speed is more than the limits, write errors can occur. The ISV can cause changes in the write data density. Based on a pre-determined limit of ISV, the acceleration check is turned on and the microcode repeats the write before a write error occurs. If this bit is on and write errors are occurring, troubleshoot the write errors. If this bit frequently occurs without any other write error conditions, it can be an indication of wear of the tape media, mechanical tape path parts or the read/write head.
4	CRC Hardware Failure	This bit indicates that the CRC checker on the ECC card has failed and activates a Check 2 condition. FRU111 (A1R2); FRU119 (A1S2)
5	FRU5	This bit indicates that one of the following conditions has occurred: 1. Skew Buffer Hardware Errors 1, 2 and 3 as determined by the demodulator module on the ECC card (A1R2). 2. ARP registers parity error during a sample period. 3. Correction registers parity error during a sample period. 4. Decode parity error during a sample period. 5. Incorrect parity on the corrected data bus during the residual byte. Possible FRUs. Condition 1: FRU123 (A2K2); FRU124 (A2L2); FRU125 (A2M2) Conditions 2-5: FRU111 (A1R2); FRU119 (A1S2)
6	FRU6	This bit indicates that one of the following conditions has occurred: 1. The data buffer did not respond correctly following the 'read data ready' signal. 2. The read clock and format did not respond correctly following the 'read data ready' signal. This bit also sets RER bit 7. Possible FRUs. FRU120 (A1K2); FRU119 (A1S2)
7	FRU7	This bit indicates that one of the following conditions has occurred: 1. Skew Buffer Hardware Errors 1, 2 and 3 as determined by the 'gate read cycle' and 'ROC equals zero' signals. Also sets the respective skew buffer hardware error bits (RER bits 0, 1 and 2). 2. The clock module on A1S2 is not cycling correctly. 3. The module 18 and module 8 counters are not in sequence. (Write/Read data flow counters are used to control data transfer.) 4. The read clock and FMT card detected bad parity on the corrected data bus during the residual byte. RER bit 3 will be set if this error occurs. 5. The data buffer did not respond correctly following the 'read data ready' signal. This condition also sets RERbit 6. 6. The read clock and FMT did not respond correctly following the 'read data ready' signal. This condition also sets RER bit 6. Possible FRUs. Condition 1: FRUs are indicated by bits 0-2. FRU123 (A2K2); FRU124 (A2L2); FRU125 (A2M2) Conditions 2 and 3: FRU119 (A1S2) Condition 4: FRU111 (A1R2); FRU119 (A1S2) Conditions 5 and 6: FRU120 (A1K2); FRU119 (A1S2)

RPR Register

- Type = Read
- Card = 01A-A1S2
- XRA Value = 4C

The Read Pattern Register (RPR) is a selectable register for pattern, tones, or amp sense. It is selected by the Read Diagnostic Control (RDC) register. In Normal mode, it is used by the microcode to determine the type of information being detected by the read logic. See the RDC register for more information.

Bit	Label	Description/Detail
0	IBG/ID18	The meaning of bits 0, 1, 2, and 3 depends on the setting of the Density Enable bit (RCR register bit 7). When Density Enable is not on, these bits indicate when an IBG, TM, ERG, or SPR pattern is being sensed. A TM indication will cause an interrupt level 2. This interrupt level is active when the RPR register bit 1 is set and RCR register bit 7 is not set. When Density Enable is on and a density pattern is being detected, bits 0, 1, 2, and 3 are an indication of the actual density being read.
1	TM/SID1	See Bit 0.
2	ERG/SID2	See Bit 0.
3	SPR/SID3	See Bit 0.
4	BOB	This bit indicates that a data block is being sensed by the read logic. It will be active when one or less zones are active and a no data condition does not exists. This bit causes a interrupt level 2. This level will be active when the RPR register bit 4 is present.
5	VOID	This bit indicates that a no data condition is being sensed.
6	NOA	This bit indicates that none of the other defined patterns exist.
7	Reserved	

Note: See "RCR Register" bit 7 and "RDC Register" bits 0 and 1 for more details.

RRC Register

- Type = Read
- Card = 01A-A1S2
- XRA Value = 4A

The Read Residual Count (RRC) register stores the residual byte count that is read from the tape. The count is equal to the number of pad bytes that were written and are in a number range of 0 to 13. The microprocessor uses the count to determine the location and number of pad bytes in the buffer so that the count is not sent to the channel.

Bit	Label	Description/Detail
0	Block IDA	Bits 0 and 1 form the encoded modulo 4 count of the block ID.
1	Block IDB	See Bit 0.
2	Reserved	
3	Reserved	
4-7		Contains the encoded residual byte count read from the drive.

RSR Register

- Type = Read/Write
- Card = 01A-A1S2
- XRA Value = 46

The Read Status Register (RSR) contains the status of the read or write operation as it progresses. It also contains the status of the error correction attempts.

Bit	Label	Description/Detail
0	Beginning Sync	This bit indicates that the beginning sync pattern was recognized by the read data flow card. When this bit is active, interrupt level 3 is signaled.
1	Ending Sync	This bit indicates that the ending sync pattern was recognized by the read data card. When this bit is active, interrupt level 3 is signaled.
2	Gap Out Timing	This bit is active when the IBG and TM or ERG or BOB are active in the Read Pattern Register (RPR). If bit 6 of the Read Control Register (RCR) is also active, interrupt level 3 is signaled, which causes 'gap out' to be sent to the drive. The drive must receive 'gap out' within a specified time in order to control the gap size.
3	Gap In	This bit is set when 'gap in' is sent by the drive during tape repositioning. It indicates that the end of the last record read or written was sensed at the read/write head.
4	Data Corrected	This bit is set when ECC corrections to the record just read are made. Bits 5-7 of this register indicate whether the corrections were successful.
5	Data Check	This bit indicates that the ECC could not correct this data block and it must be repositioned for a retry. A check 2 interrupt is signaled when this occurs.
6	Multitrack Indicator	This bit indicates that more ECC pointers were detected then the operating threshold permits. A check 2 interrupt is signaled when this occurs during write operations.
7	CRC Check	This bit indicates that a data check was detected. A check 2 interrupt is signaled when this occurs.

WCR Register

- Type = Read/Write
- Card = 01A-A1P2
- XRA Value = 40

The Write Control Register (WCR) controls the operation of the write data flow and conditions the appropriate write function.

Bit	Label	Description/Detail
0	Block IDA	Bits 0 and 1 form the modulo 4 count of the 2 bit ID. They are set to the starting ID (before Gap In) for the first record. On following write operations, the microcode must set the ID somewhere in the IBG before the record which they are to be used. They should not change again until the next IBG.
1	Block IDB	See Bit 0.
2	LWR	This bit conditions the write logic to execute a Loop-Write- to-Read operation.
3	DIAG	This bit conditions the modulation encoder to handle the diagnostic data supplied to the write data flow functional area.
4	Reserved	
5	Write Data Flow Op Enable	When this bit equals a one, bits 6 and 7 have the meaning indicated.
6	Write Mode A	Bits 5, 6, and 7 cause the Write Data Flow to write the following command information: BIT 5 6 7 — COMMAND 1 0 0 — Write Data 1 0 1 — Write TM 1 1 0 — Write ERG 1 1 1 — Write Density These bits must be valid before the write head is one third of the way through the preceding IBG, when writing a record. They cannot change again until Device Data Transfer Complete (Bit 0 of the BDS register) is detected. This indicates that a full record has been transferred to the drive. To continue writing to this drive, these bits must be valid before the write head is two thirds of the way through the IBG.
7	Write Mode Bits	See Bit 6.

WSE Register

- Type = Read
- Card = 01A-A1P2
- XRA Value = 43

The Write Status/Error (WSE) register contains the status of the write circuits and the write operation currently in progress.

Bit	Label	Description/Detail
0	Write Operation	This bit is active when 'gap in' is received from the drive. It is reset during a write operation if bit 5 of the Write Control register (WCR) does not become active during the IBG mark. When this bit is not active, there is no writing of data. Also, this bit is not affected by any resets to the write circuits.
1	End Write	This bit indicates that the last byte of the postamble has been written. The IBG mark must be still written.
2	Reserved	
3	Reserved	
4	Error 2	This bit indicates a write control error.
5	Error 3	This bit indicates a write data flow error.
6	Error 4	This bit indicates a multiplexed data parity error.
7	Reserved	

XRA Register

- Type = Read
- Card = 01A-A1D2
- XRA Value = F3

The External Register Address (XRA) register saves the value of the external register address during execution cycles of instructions that address XR registers. When an XR error is detected, this register is latched and it contains the address of the XR register being addressed. The XRA register is reset by MP Reset or Power-On-Reset (POR).

Note: All cards referenced by this table are on the 01A gate.

Bit	Label	Description/Detail
0	XR Address Extend Bit 0	Set from processor control register bit 6. See Bit 1.
1	XR Address Extend Bit 1	Set from processor control register bit 7. Bits 0 and 1 indicate which XR page to access. Bit 0 Bit 1 XR Page 0 0 A 0 1 B 1 0 C 1 1 D
2	XR Address Bus Bit 0	Bit 7 of current instruction. See Bit 6.
3	XR Address Bus Bit 1	Bit 8 of current instruction. See Bit 6.
4	XR Address Bus Bit 2	Bit 9 of current instruction. See Bit 6.
5	XR Address Bus Bit 3	Bit 10 of current instruction. See Bit 6.
6	XR Address Bus Bit 4	Bit 11 of current instruction. Bits 2 through 6 are set from CS Data Bus Hi/Lo bits 7 through 11 for instructions that address XR registers.
7	XR Address Bus Parity	Set for even parity for XR (external register) bus address bits 0 through 4. This bit is generated by the microprocessor card (A1D2) for even parity on the XR Address Bus (bits 0-4, and P).

4.5 Megabyte Buffer Adapter Internal Registers

The following is a list of internal 4.5 Mb/s buffer adapter registers. These registers can only be accessed by putting the page and register numbers into the CMRS register and reading or writing the CMRP register. See MI pages DF 36 and DF 37.

Page 2 Registers Type = Read Only

This page contains three registers used to report errors detected by the C2PO, and one register that displays the feature level.

REG	MNEMONIC	NAME	RESET
0	CTE0	C2PO Error 0	Check 5
1	CTXE	C2PO XR Error	Check 5
2	CMFL	Feature Level Register	None

CTE0 Register

Bit	Name/Description
0	Channel Overrun Error
1	100 ns Clock Ring Error
2	300 ns Clock Ring Error
3	BC Control Parity Error
4	BC Toggle Error
5	Channel Data Parity Error
6	Feature Level Parity Error
7	Reserved

CTXE Register

Bit	Name/Description
0	Reserved
1	XR Write Data Parity Error
2	XR Read Data Parity Error
3	XR Output Parity Error
4	Reserved
5	Reserved
6	Reserved
7	Reserved

CMFL Register

Bit	Name/Description
0	4.5 Mb/s Buffer Adapter Card Installed
1	EC Level 0
2	EC Level 1
3	Reserved
4	Tailgate A Installed
5	Tailgate B Installed
6	Tailgate C Installed
7	Tailgate D Installed

Page 5 Registers Type = Read/Write

This page contains two registers that provide the microcode interface for the diagnostic operations on the buffer adapter card.

REG	MNEMONIC	NAME	RESET
0	CMD0	Diagnostic Register 0	Channel Control
1	CMD1	Diagnostic Register 1	Channel Control

CMD0 Register

Bit	Name/Description
0	Shift Gate Select 0
1	Shift Gate Select 1
2	Shift Gate Select 2
3	Shift Gate Enable
4	Gate BC
5	Disable ECC
6	Reserved
7	Reserved

CMD1 Register

Bit	Name/Description	
0	[Scan Out Data (Read)]	[Scan In Data (Write)]
1	[Service In (Read)]	[Scan A Clock (Write)]
2	[Data In (Read)]	[Scan B Clock (Write)]
3	[Write End (Read)]	[Read End (Write)]
4	Service Out	
5	Data Out	
6	Stop Out	
7	Suppress out	

Note: All of the internal buffer adapter registers are present if the buffer adapter card supports the Improved Data Recording Capability feature. Only the CET0, CTXE, CMFL, CMD0, and CMD1 registers are present if the 4.5 Mb/s without the Improved Data Recording Capability feature is present. None of the registers are present if the Improved Data Recording Capability or the 4.5 Mb/s channel features are not installed.

These are internal registers and cannot be accessed directly. These registers can only be accessed by putting the page and register numbers into the CMRS register and reading or writing the CMRP register. See MI page DF 36 and 37 for more information.

Page 0 Registers

Type = Read Only

This page contains four sets of channel byte count registers from COMP0-3. The four channel byte count registers in each COMP count the total number of bytes transferred to or from the channel. Channel byte count 0 is the most significant byte of the count field. The registers can be reset by Channel control.

REG	MNEMONIC	NAME
0	CP0B0	COMP0 Channel Byte Count 0
1	CP0B1	COMP0 Channel Byte Count 1
2	CP0B2	COMP0 Channel Byte Count 2
3	CP0B3	COMP0 Channel Byte Count 3
4	CP1B0	COMP1 Channel Byte Count 0
5	CP1B1	COMP1 Channel Byte Count 1
6	CP1B2	COMP1 Channel Byte Count 2
7	CP1B3	COMP1 Channel Byte Count 3
8	CP2B0	COMP2 Channel Byte Count 0
9	CP2B1	COMP2 Channel Byte Count 1
A	CP2B2	COMP2 Channel Byte Count 2
B	CP2B3	COMP2 Channel Byte Count 3
C	CP3B0	COMP3 Channel Byte Count 0
D	CP3B1	COMP3 Channel Byte Count 1
E	CP3B2	COMP3 Channel Byte Count 2
F	CP3B3	COMP3 Channel Byte Count 3

Page 2 Registers

Type = Read Only

This page contains three registers used to report errors detected by the C3PO or display the buffer adapter feature level.

REG	MNEMONIC	NAME	RESET
0	CTE0	C3PO Error 0	Check 5
1	CTXE	C3PO XR Error	Check 5
2	CMFL	Buffer Adapter feature level	None

	CTE0 Register	CTXE Register	CMFL Register
Bit	*Name/Description*	*Name/Description*	*Name/Description*
0	Channel Overrun Error	Comp XR Error	Improved Data Recording Capability installed
1	100 ns Clock Ring Error	XR Write Data Parity Error	Comp EC Level 0
2	300 ns Clock Ring Error	XR Read Data Parity Error	Comp EC Level 1
3	Comp Control Parity Error	XR Output Parity Error	Improved Data Recording Capability allowed

	CTE0 Register	CTXE Register	CMFL Register
4	Channel Toggle Error	Reserved	Tailgate A Installed
5	Channel Data Parity Error	Reserved	Tailgate B Installed
6	Feature Level Parity Error	Reserved	Tailgate C Installed
7	CRC Error	Reserved	Tailgate D Installed

Page 3 Registers

Type = Read Only

This Improved Data Recording Capability page consists of four sets of two error registers found in COMP0-3. Each COMP has two error registers, COMP Error 0 and COMP Error 1. The bit organization is the same for each COMP register.

REG	MNEMONIC	NAME	RESET
0	CP0E0	COMP0 Error 0	Check 5
1	CP0E1	COMP0 Error 1	Check 5
2	CP1E0	COMP0 Error 0	Check 5
3	CP1E1	COMP0 Error 1	Check 5
4	CP2E0	COMP0 Error 0	Check 5
5	CP2E1	COMP0 Error 1	Check 5
6	CP3E0	COMP0 Error 0	Check 5
7	CP3E1	COMP0 Error 1	Check 5

	COMP0-3 Error 0	COMP0-3 Error 1
Bit	*Name/Description*	*Name/Description*
0	Upper CRC Error 0 (UCRC0)	Channel Adapter Data Parity Error
1	Upper CRC Error 1 (UCRC1)	Channel Adapter Master Transfer Error
2	Lower CRC Error 0 (LCRC0)	C3PO to Channel Adapter Interface Error
3	Lower CRC Error 1 (LCRC1)	Buffer Control Channel Interface Error
4	Lower CRC Error 2 (LCRC2)	Buffer Control Master Transfer Error
5	Lower CRC Error 3 (LCRC3)	C3PO 100 ns Clock Ring Error
6	Initialization Error	Channel Byte Count Overflow
7	Encode Not Equal to Decode	C3PO to Channel Adapter Overflow Error

0 0 0 0 0 0 0 0 0 0

Page 5 Registers

Type = Read/Write

This page contains two registers that provide the microcode interface for the diagnostic operations on the buffer adapter card.

REG	MNEMONIC	NAME	RESET
0	CMD0	Diagnostic Register 0	Channel Control
1	CMD1	Diagnostic Register 1	Channel Control

	CMD0 Register	CMD1 Register
Bit	*Name/Description*	*Name/Description*
0	Shift Gate Select 0	Scan Out Data (Read) or Scan In Data (Write)
1	Shift Gate Select 1	Service In (Read) or Scan A Clock (Write)
2	Shift Gate Select 2	Data In (Read) or Scan B Clock (Write)
3	Shift Gate Enable	Write End (Read) or Read End (Write)
4	Gate BC	Service Out
5	Disable ECC	Data Out
6	Reserved	Stop Out
7	Reserved	Suppress out

Page 6 Registers

Type = Read/Write

This page contains four registers in COMP0-3 that are used to select internal diagnostic functions. The organization of these COMP Diagnostic Registers is the same for each COMP.

REG	MNEMONIC	NAME	RESET
0	CP0D	COMP0 Diagnostic	Channel Control
1	CP1D	COMP1 Diagnostic	Channel Control
2	CP2D	COMP2 Diagnostic	Channel Control
3	CP3D	COMP3 Diagnostic	Channel Control

	CMP0-3 Diagnostic Registers
Bit	*Name/Description*
0	RAM Select 0
1	RAM Select 1
2	RAM Select 2
3	Disable Encoder and Decoder
4	Force Bad Parity
5	Force Busy
6	Force Encode Statistic RAM Initialization Error
7	Force Decode Statistic RAM Initialization Error

Page 7 Registers

Type = Read/Write

This page consists of four registers in COMP0-3 that are used to establish operation parameters at power on time. The organization of the COMP configuration registers is the same for each COMP.

REG	MNEMONIC	NAME	RESET
0	CP0C	COMP0 Configuration	POR
1	CP1C	COMP1 Configuration	POR
2	CP2C	COMP2 Configuration	POR
3	CP3C	COMP3 Configuration	POR

	CMP0-3 Configuration Registers
Bit	*Name/Description*
0	COMP Online/Offline (1 = online)
1	COMP ID 0
2	COMP ID 1
3	COMP ID 2
4	COMP Count 0
5	COMP Count 1
6	1 or 2 Statistics RAMs (1 = Stat. RAM 2)
7	Global CRC

0 0 0 0 0 0 0 0 0 0

CST Table

The Command Status Table (CST) contains information about the command currently executing with a drive. The fields in the CST are set by microcode. This table is accessed by the drive address using the support diskette Subsystem Display/Alter program.

Word 0

Bits	Field	Function	Detail
0-3	ADSTAT	Provides initial status and interrupt condition indications generated by the channel adapter.	0 - CCW accepted 1 - End of command chain 2 - Interface disconnect 3 - Selective reset 5 - Data path not available 6 - Invalid buffer conditions 7 - CCR Interrupt - CCR stacked, refused, or channel did not chain from the device end after a CCR. 8 - Subsystem error 9 - Command sequence invalid A - Reserved different group B - Command reject C - Bus out parity error D Deferred unit check E Device not ready F Device file protected
4-7	DRIVE	Provides the drive address for which a channel command was received.	
8-12	CMD	Indicates which 5-bit channel command code is to be executed.	The 5-bit channel command codes accepted by the control unit are: **SENSE COMMANDS:** '00' - Modesets other than 3480 '08' - Read block ID '10' - Sense '18' - Sense I/O device '20' - Sense path group ID '28' - Read buffered log **READ/WRITE COMMANDS:** '80' - No operation '88' - Locate block '90' - Synchronize buffer '98' - Write 'A0' - Read 'A8' - Read backward 'B0' - Test I/O 'B8' - Data security erase **CONTROL COMMANDS:** 'C0' - Rewind 'C8' - Rewind unload 'D0' - Erase gap 'D8' - Write tape mark 'E0' - Forward space block 'E8' - Backspace block 'F0' - Forward space file 'F8' - Backspace file **MISCELLANEOUS COMMANDS:** '40' - Control access '48' - Set path group ID '50' - Suspend multipath reconnection '58' - Read data buffer '60' - 3480 mode set '68' - Load display '70' - Assign '78' - Unassign
13	SPVRINH	Indicates that supervisor operations are inhibited.	
14-15		Reserved	

Bits	Field	Function	Detail
0-3	CHANNEL	Identifies which of this control unit's channel adapters received the command.	1 0 0 0 = Channel adapter A 0 1 0 0 = Channel adapter B 0 0 1 0 = Channel adapter C 0 0 0 1 = Channel adapter D
4	RECCU	Receiving CU's bit indicates which control unit received the command.	0 = Control unit 0 1 = Control unit 1
5	PENDING	Command Pending bit indicates that a command is in progress for a drive.	
6	FIRST	1st pass complete bit indicates that the first part of a given command is complete.	
7	RETRY	Command Retry bit indicates that the channel command retry status for the addressed drive has been accepted.	
8	RECERR	Record-In Error bit indicates that the read command has a permanent error, but must transfer any available read data to the channel before performing a unit check on the command.	
9	NODATA	Indicates that a read operation had to be performed (because no data was in the buffer for this drive) when a read command was sent from the channel.	

Bits	Field	Function	Detail
10	WRTMODE	Write Mode bit indicates whether the drive is operating in tape write or buffer write mode.	0 = Buffer write mode 1 = Tape write mode
11	NOTIFY	Indicates that Continue Command execution is to be notified by scan when a drive operation has been marked complete.	
12-15	CCPARM	The Continue Command execution parameter is used by Continue Command execution when it has been notified by scan that a device operation has been marked complete.	**DEVICE PREPARATION CODES:** 0 0 0 1 = Read ahead stopped 0 0 1 1 = Buffer write operation complete 0 0 1 0 = Repositioning complete 0 1 0 0 = Spare code 0 1 0 1 = Spare code 0 1 1 0 = Spare code **BUFFER MANAGEMENT CODES:** 0 1 1 1 = Buffer deallocation pending 1 0 0 0 = Device sending in progress 1 0 0 1 = Spare code 1 0 1 0 = Spare code 1 0 1 1 = Spare code **SPECIAL EXECUTION CODES:** 1 1 0 0 = Sector location complete 1 1 0 1 = Selective reset buffer write complete 1 1 1 0 = Repositioning because of off-line sequence 1 1 1 1 = Spare code

Control Storage Tables and Logs (Continued)

CST Table (Continued)

Word 2

Bits	Field	Function	Detail
0	LOCDIR	Indicates the search direction by the microprocessor for the Locate Block command.	0 = Forward search in progress 1 = Backward search in progress
1	CHANGE	Indicates whether a change in search direction for the Locate Block command has occurred. Also indicates if the read direction has been changed to determine when to set the Inhibit ERPS in the Logical Device Table (LDT) and the Suppress Read Ahead bit 4 in the CST.	
2	NERP	Permanent Inhibit CU ERPS bit indicates that the Inhibit ERPS bit in the Logical Device Table (LDT) for this device should not be reset at the end of the command chain.	
3	INTDIS	Indicates that a interface disconnect has been detected and the channel adapter has not responded with device freed. This bit is set by OCSSPMOS and reset by OCSMDFOS when the device freed has occurred.	
4	SUPRDA	Suppress Read Ahead bit is set whenever a write type command has been received or whenever the read commands that have been received have changed direction twice. When set, this bit causes read ahead operations to be inhibited until a tape mark has been read or written, or that a Locate Block, Rewind Unload Device operation has been initiated.	
5	CONCONN	Contingent Connection bit indicates that the drive is connected to the channel that issued the command (which has unit checked) until the next SIO has been accepted by the control unit.	
6	DISCON	Indicates that an interface disconnect has been detected by the channel adapter and has been acknowledged by the microcode.	
7	SELRST	Indicates that a 'Selective Reset' has been detected by the channel adapter and that the reset is in progress.	
8	CHEND	Indicates that a 'Channel End' status byte has been accepted by the channel and that a Device End has not been received from the addressed drive.	
9	PERROR	Indicates that a 'Permanent Error' has occurred with write data in the drive's buffer segment. All existing write data will be deleted from the buffer segment if a tape motion command is received.	
10	CCRINT	Indicates that the channel adapter has generated a Channel Command Retry Interrupt (CCR Interrupt) because a CCR was either stacked or refused by the channel.	
11	ADUCK	Indicates that the channel adapter generated a unit check during initial status and presented the status to the channel.	
12	PTRANS	Indicates that a 'Permanent Parameter Data Transfer Error' occurred and that the current command must be unit checked.	
13	SYSRES	Indicates that a 'System Reset' was detected by the channel adapter.	
14	LBBIT	The 'Load Balanced Requested Bit' indicates that the balancing algorithm has determined that the addressed drive can be connected to the remote control unit when conditions are appropriate.	
15	SENDEV	Indicates that a drive whose buffer is assigned to the local control unit will operate better with the remote control unit and should be connected to it when conditions are appropriate.	

Control Storage Tables and Logs (Continued)

CUT Table

The Control Unit Operations Table (CUT) contains information that only pertains to the control unit. It also contains flags that control the operation of the control unit.

Word 0

Bits	Field	Function	Detail
0	INRDAHD	Inhibits read ahead operations on any drive connected to this control unit (Set by MD only). See Note 1.	
1	INBUFWR	Inhibits buffered write operations for any device connected to this control unit (Set by MD only). See Note 1.	
2	INLDBAL	Inhibits this control unit from load balancing a drive to the other control unit (Set by MD only). See Note 1.	
3	INERPS	Inhibits this control unit from performing any internal ERPS (Set by MD only). See Note 1.	
4	INRCNCT	Inhibits this control unit from using the reconnect algorithm and Reconnect Timer (ITC), (Set by MD only). See Note 1.	
5	OFFLBUFL	Indicates to the sending device to set Device Error. Causes the buffered log to be transferred to the host (Set by MD only). See Note 1.	
6	FORCELOG	Causes this control unit to be in forced logging mode. Sense data is logged at the host for all errors (Set by MD only). See Note 2.	
7	INELYST	Inhibits this control unit from using the early start algorithm and Early Start Timer (ITD), (Set by MD only). See Note 1.	
8	DEFERUC	Indicates a deferred unit check. Unit check will be presented to the next CCW processed by this control unit.	
9	DIAGREAD	Indicates that this control unit is in LWR with ECC disabled. This bit is set at the same time that Bit 3 in the Read Diagnostic Control (RDC) register is set.	Setting this bit causes: All 18 tracks of data are read into the buffer from tape. No Block ID Errors will be flagged. All data read into the buffer will be transferred to the channel.
10	INITTIO	Indicates that Test I/O's are scheduled for all drives and are executing.	
11	INHSEL	Inhibits this control unit from selecting any drive.	
12	DISKIML	Indicates that this control unit has just been IML'ed from diskette device. This bit is only valid during initialization and resets later.	
13	NOPAIRS	Indicates that no buffer segments are available to join two segments to double the size of the buffer for a drive.	
14	INCRC	Indicates that Cyclic Redundancy Check (CRC) errors, from the read data flow, will not be flagged during read operations.	
15	INBLKID	Indicates that Block ID errors will not be flagged during read operations.	

Notes:

1. These functions can be reset by:

   a. Disconnecting the MD from the control unit.
   b. Using the trace/match control reset function on the support diskette. See "Trace/Match Control-Select Control Options" on SDISK 1.

2. Forced logging mode can be reset by:

   a. An IML.
   b. Using the trace/match control reset function on the support diskette. See "Trace/Match Control-Select Control Options" on SDISK 1.

Control Storage Tables and Logs (Continued)

CUT Table (Continued)

Word 1

Bits	Field	Function	Detail
0	NUMOCU	Indicates that two CUs can communicate with each other.	0 = One CU on status store communication is not active 1 = Two CUs and status store communication is active.
1-5	NUMDEV	Indicates the number of drives in the subsystem.	0 0001 = 1 drive 1 0000 = 16 drives
6	OCUADDR	Indicates the setting of the CU0/CU1 toggle switch.	0 = Control unit 0 1 = Control unit 1
7	SSFEAT	Indicates that this control unit has the communicating status store installed.	
8-15	NUMSEG	Indicates the number of 32K byte buffer segments that are installed on this control unit.	

Word 2

Bits	Field	Function	Detail
0-3	CAATCH	Bit mask that indicates which channel adapters are attached to this control unit.	1 0 0 0 = Channel adapter A 0 1 0 0 = Channel adapter B 0 0 1 0 = Channel adapter C 0 0 0 1 = Channel adapter D 1 1 1 1 = All channel adapters
4	MBINUSE	Indicates that the message buffer in the status store is in use.	
5	FIRSTMSG	Flag that is set after the first message has been sent to the other control unit.	
6	UNEXP6	Indicates that an attempt has been made to clear an unexpected level 6 interrupt by having the other control unit disconnect.	
7	CK1ERR	Indicates that a Check 1 error has occurred.	
8	NOSIX	Indicates that level 6 interrupts should not be re-enabled.	
9	CUOFF	Indicates that this control unit has completed offline processing.	
10	LPROOFF	Indicates that an offline request for the local control unit is being processed.	
11	RPROOFF	Indicates that an offline request for the remote control unit is being processed.	
12-15	OFFCNT	Contains the counter that indicates the number of drives that must be processed before offline processing will be completed.	

CUT Table (Continued)

Word 3

Bits	Field	Function	Detail
0	MBBUSY	Indicates that the Message Buffer In Use bit should be set on.	
1	CMPCTL	Indicates that Coordinate MP Assignments is in the process of buffer switch assignment and status should be stacked.	
2	OCUCONNT	Indicates that the other control unit has reconnected and asked for either a copy of control storage or all PGM and PGT tables.	
3	RMTCK1	Indicates that the other control unit is recovering from a check 1 error.	
4	MDCONNT	Indicates that the other control unit has reconnected for Maintenance Device purposes.	
5	CK1RECOV	Indicates that this control unit has successfully executed a remote check 1 recovery procedure.	
6	OFFMSGRS	Indicates that this control unit has either received or sent a 2 Control Unit Offline message.	
7	LDBLINIT	Indicates that load balance is in process and waiting for Fault Count from the other control unit.	
8-15	LDBALTH	Contains the threshold value for the load balance algorithm. If the difference between the total Fault Counts of the two control units is not greater than this threshold, the load balance algorithm will not be performed.	

Word 4

Bits	Field	Function	Detail
0-15	FLTLIM	Contains the Fault Count for this control unit. If the Total Fault Count reaches the limit, the load balance algorithm is performed.	
16-31	TOTFLT	Contain the number of faults in this control unit.	
32-39	CUBL15	Contains the Control Unit Equipment Checks. It is put into Format 21 sense by any drive, then reset.	
40-47	CUBL16	Contains the count of the number of 16K byte buffer segments that have been de-marked.	

Control Storage Tables and Logs (Continued)

DGHELO Log

The Diagnostic Hardware Error Log (DGHELO) contains data stored when a hardware error occurs. This data is the microcode error code, the hardware error code, and all readable error registers.

Table updates are under the control of the maintenance device. When the diagnostic overlay is enabled the table is updated each time the sense builder is called, unless the error is a read or write data flow error and the control unit ERP is doing recovery when the error occurs.

DGHELO entries are twelve words long and are separated by the contents of word zero (CDEF). The log is 560 words long and wraps to ensure that the last 18 words are saved.

DGHELO can be displayed by the MD support diskette function "Storage Display/Alter-Control/Unit Tables" (see SDISK 1). When DGHELO is entered, the latest error is shown in the top line of the MD display. Since DGHELO is a wrap log, the next entry on the MD display will be the oldest entry in the log. If you scroll the display forward or backward to see additional entries, record the microcode table address, so you will know when you have returned to the latest entry.

Word	Bits	Definition
0	0-15	A four-character constant ('CDEF') to identify each entry.
1	0-15	The microcode error code. This error code is the same as the control unit error code stored in sense bytes 10 and 11, or 12 and 13, or 14 and 15 of Format 20 sense.
2	0-7 8-15	Drive address CU flag byte
3	0-15	The hardware error code. This is the same as the control unit error code stored in bytes 16 and 17 of Format 20 sense.
4 (See Note)	0-7 8-15	Error register CER Error register PER
5 (See Note)	0-7 8-15	Error register WSE Error register RSR
6 (See Note)	0-7 8-15	Error register RER Error register DSE
7 (See Note)	0-7 8-15	Error register RPR Error register MTI
8 (See Note)	0-7 8-15	BCSE Group 0 BCSE Group 1
9 (See Note)	0-7 8-15	BCSE Group 2 BCSE Group 3
10 (See Note)	0-7 8-15	BDSE Group 0 BDSE Group 1
11 (See Note)	0-7 8-15	BDSE Group 2 BDSE Group 3

Note: See the DF section Table of Contents to find the location of external register detailed descriptions.

Control Storage Tables and Logs (Continued)

DOT Table

The Device Operation Table (DOT) contains information about scheduled, active (selected), and completed drive operations. There is one entry for each drive. The table is accessed by the drive address.

Word 2

Bits	Field	Function	Detail
0-3		Not used.	
4	ERPSR	Indicates that ERP is active for this drive operation.	
5	VALID	When on, this bit indicates the service is waiting to execute an operation. When off, the other DOT fields are not valid.	
6	STARTED	Indicates that the drive operation has started.	
7	COMPLETE	Indicates that the drive operation has completed.	
8	INFOSEQ	Indicates information sequence operation (See Note).	Control unit to drive commands. For example: Drive test I/O, drive sense, read control storage, read LSRs, and read drive external registers.
9	CNTLSEQ	Indicates control sequence operation (See Note).	Operations that do not involve data transfer.
10	BUFRXFR	Indicates that data transferred is to be held in the buffer (Read only, See Note).	
11-15	DEVCMD	Drive command code to be issued (See Note).	Command codes are described in the OPER section.

Note: Operational Modes:

Bits:	8	9	10	11-15	
	1	1	1	X	Synchronous Command Mode
	0	0	0	0	Diagnostic Monitor
	0	0	X	X	Data Transfer
	0	0	1	X	Read Operation
	0	0	0	X	Space Operation

Control Storage Tables and Logs (Continued)

DOT Table

The Device Operation Table (DOT) contains information about scheduled, active (selected), and completed drive operations. There is one entry for each drive. The table is accessed by the drive address.

Word 0

Bits	Field	Function	Detail
0-15	CHAIN	Contains a pointer to the next 'DOT' entry.	

Word 1

Bits	Field	Function	Detail
0-7	DVADRDOT	The device address of this entry.	
8-15		Used by ERP to control ECC.	

Word 2

Bits	Field	Function	Detail
0-3		Not used.	
4	ERPSR	Indicates that ERP is active for this drive operation.	
5	VALID	When on, this bit indicates the service is waiting to execute an operation. When off, the other DOT fields are not valid.	
6	STARTED	Indicates that the drive operation has started.	
7	COMPLETE	Indicates that the drive operation has completed.	
8	INFOSEQ	Indicates information sequence operation (See Note).	Control Unit to drive commands. For example: Drive test I/O, drive sense, read control storage, read LSRs, and read drive external registers.
9	CNTLSEQ	Indicates control sequence operation (See Note).	Operations that do not involve data transfer.
10	BUFRXFR	Indicates that data transferred is to be held in the buffer (Read only, See Note).	
11-15	DEVCMD	Drive command code to be issued (See Note).	Command codes are described in the OPER section.

Note: Operational Modes:

Bits:	8	9	10	11-15	
	1	1	1	X	Synchronous Command Mode
	0	0	0	0	Diagnostic Monitor
	0	0	X	X	Data Transfer
	0	0	1	X	Read Operation
	0	0	0	X	Space Operation

0 0 0 0 0 0 0 0 0 0

LDT Table

The Logical Device Table (LDT) contains current information about each drive which is not directly related to a particular buffer segment.

Word 0

Bits	Field	Function
0-7	DEVFLT	Contains the fault count for this drive since the last reset of 'Fault Count'.
8	INHAUSP	Inhibits this control unit from issuing a forward or backward 'Auto Space' command to this drive.
9	INHRDAH	Inhibits performing read ahead operations.
10	INHREC	Inhibits using the Reconnect Timer (ITC).
11	INHSERST	Inhibits using the serial interconnection to start this drive.
12	INHERP	Inhibits performing internal ERPS.
13	MDDEV	Indicates that this drive is reserved to the MD.
14	ERPDEV	Indicates that this drive is reserved to the ERP.
15	CALLERP	Indicates to call the ERP after Gap Out processing, even if the record was read with no errors.

Word 1

Bits	Field	Function
0	INHWROP	Inhibits this control unit from starting a Write operation, from the buffer to this drive.
1	IBGTOUT	Indicates that during Gap Out processing an IBG Time Out occurred on the last IBG.
2	ENDSYC	Indicates the 'Ending Sync' was detected during the read of the last record.
3	STRBC	Indicates that writing has started but the read-to-write head timer did not time out.
4	WR1REC	Indicates that the first record of a Write operation is ready to be written.
5	RD1REC	Indicates that writing has started but the first record has not been 'read back checked'.
6-7	TWOBITID	Is the modulo 4 count used to identify a Write operation with its 'read back check'.
8	BUFFPIN	Indicates that this drive's buffer is pinned to this control unit.
9	PCUDA	Permits the control unit's deallocation of this drive.
10	TPMARK	Indicates that the last record was a tape mark.
11	SYNCMODE	Indicates that this drive is in Synchronous Data Transfer mode (blocksize is more than 64K).
12	RDAHOP	Indicates that the current Read operation is not scheduled (Read Ahead).
13	TINHWROP	Indicates that a Read Data Buffer operation is in progress and Write operations are not to be scheduled.
14	DISERP	Indicates to disable the ERP flag for errors during channel data transfers.

Control Storage Tables and Logs (Continued)

LDT Table (Continued)

Word 2

Bits	Field	Function
0-15	CHID1	Contains the high order channel block ID.

Word 3

Bits	Field	Function
0-15	CHID2	Contains the low order channel block ID.

Word 4

Bits	Field	Function
0-15	DEVID1	Contains the high order device block ID.

Word 5

Bits	Field	Function
0-15	DEVID2	Contains the low order device block ID.

Word 6

Bits	Field	Function
0-15	BLCKSIZ	Contains the blocksize/16 of the largest block in this file.

Word 7

Bits	Field	Function
0-15	BSTPTR	Contains the buffer status table PTR under normal conditions.

Word 8

Bits	Field	Function
0-15	ERPBST	Contains the buffer status table PTR under ERP conditions.

Word 9

Bits	Field	Function
0	SCNALGOR	Indicates that Scan is needed to compute the reconnect time for this device.
1	SCNALGOE	Indicates that Scan is needed to compute the early start time for this device.
2	SCNREC	Indicates that when the ITC times out, Scan should call Reconnect for this device.
3	SCNFOREC	Indicates that Reconnect should be called in despite the ITC timer.
4-15	SCNRSVD	Reserved

Word 10

Bits	Field	Function
0-7	IBGTOCNT	Contains the counter for the number of erase gaps (IBGOUTS) that occurred during a write operation.
8	GLOC	Indicates that this is the first Gap-In after a Disconnected Locate operation.
9	NOBID	Indicates that not to check Bids for correct during Space Ops.
10	DBSDEV	Indicates that this device is assigned to the MP by buffer management for buffer deallocation purposes.
11	ALLNOREP	
12-15	FIROVRN	Contains the number of Device- Buffer Overruns that have occurred while writing a record from the buffer to tape.

Word 11

Bits	Field	Function
0-15	LOXNT	Contains the local transfer count.

Word 12

Bits	Field	Function
0-15	REXNT	Contains the remote transfer count.

Control Storage Tables and Logs (Continued)

Control Storage Tables and Logs (Continued)

PGM Table

The Path Group Map (PGM) consists of seven data words for each entry. (Each drive has a separate seven-word entry.) The table is accessed by the drive address.

Word 0

Bits	Field	Function	Detail
0-7	MAP	The first byte is the path group mask that has a bit set for each channel adapter interface that is a member of the path.	Bits 0-3 represent control unit 0 channel adapters A through D Bits 4-7 represent control unit 1 channel adapters A through D Bit format: 1 0 0 0 = A 0 1 0 0 = B 0 0 1 0 = C 0 0 0 1 = D
8-13		Not used.	
14	ALLASND	Indicates that all 8 channel paths have drives assigned. This allows the control unit to differentiate between the All Assigned and None Assigned conditions of the channel assignment in status store.	
15	PSWDREC	Indicates that a valid password has been set by a control access command.	

Word 1

Bits	Field	Function	Detail
0-7		Not used.	
8-15	PASSWRD1	Contains the password (if any) set by the control access command.	Passwords are generated by the host system.

Word 2

Bits	Field	Function	Detail
0-7	PASSWRD2	Contains the password (if any) set by the control access command.	Passwords are generated by the host system.
8-15	PASSWRD3	Contains the password (if any) set by the control access command.	

Word 3

Bits	Field	Function	Detail
0-7	PASSWRD4	Contains the password (if any) set by the control access command.	Passwords are generated by the host system.
8-15	PASSWRD5	Contains the password (if any) set by the control access command.	

Word 4

Bits	Field	Function	Detail
0-7	PASSWRD6	Contains the password (if any) set by the control access command.	Passwords are generated by the host system.
8-15	PASSWRD7	Contains the password (if any) set by the control access command.	

Word 5

Bits	Field	Function	Detail
0-7	PASSWRD8	Contains the password (if any) set by the control access command.	Passwords are generated by the host system.
8-15	PASSWRD9	Contains the password (if any) set by the control access command.	

Word 6

Bits	Field	Function	Detail
0-7	PASSWRDA	Contains the password (if any) set by the control access command.	Passwords are generated by the host system.
8-15	PASSWRDB	Contains the password (if any) set by the control access command.	

PGT Table

The Path Group ID Table (PGT) contains the path group identification of each channel adapter interface for both control units. It also contains the Path Group Management byte that includes information about the path mode of the interface (single or multipath). There is one PGT for each channel.

The Path Group ID Table is affected by Set Path Group ID commands addressed to drives connected to both local and remote control units in a two control unit subsystem. This ensures that both control units will contain the same path group ID information after the execution of any Set Path Group ID commands.

There is an entry in this table for each control unit and adapter combination. (Up to eight entries In a maximum, dual control unit, eight channel subsystem.) The table is accessed by specifying the control unit number and channel adapter.

Byte 0

Bits	Field	Function	Detail
0	SYSERR	A system reset is being processed within the control unit. The reset may have been caused by the channel or control unit.	
1-2	Reserved		
3	IDREC	The ID Received bit is set if a path group ID has been received for the channel interface since the last Power-On or system reset.	
4	PATHMODE	Set for channel interfaces in multipath mode. Reset for interfaces in single path mode.	0 = Single path
5-7	GROUP	Identifies a path group ID that has been received by the control unit over this channel. These three bits are a shorthand identifier of the 11 byte Path Sweep GROUP ID.	0 0 0 = Path group 0 0 0 1 = Path group 1 0 1 0 = Path group 2 0 1 1 = Path group 3 1 0 0 = Path group 4 1 0 1 = Path group 5 1 1 0 = Path group 6 1 1 1 = Path group 7

Bytes 13 and 14

Bits	Field	Function	Detail
0	CADIS	Indicates that this channel adapter is disabled.	
1	PRODIS	Indicates that this channel adapter is processing a channel adapter disable sequence.	Disable sequence is initiated by moving the Disable switch to Disable or the Off-line/On-line switch to Off-line.
2	Reserved		
3	Reserved		
4-7	Reserved		
8	PROSYS	Indicates that the system reset for this channel is in progress.	
9-15	Reserved		

PST Table

The Pattern Sequence Table (PST) contains 16 entries which indicates the sequence of written and read back check patterns during a Device Data Transfer operation.

SNERRH Table

The Sense Error History Table (SNERRH) contains the sense builder call entry parameters and the first four words of drive sense that result from a drive unit check. The table is updated each time the sense builder is called. It is 256 words long and wraps when filled so that the last 20 to 40 errors are saved.

SNERRH can be displayed by using the "Storage Display/Alter - Control Unit Tables" function, see SDISK 1. When SNERRH is entered, the latest error record is shown in the top line of the MD display. Since SNERRH is a wrap log, the next entry on the MD display will be the oldest entry in the log. If you scroll the display forward or backward to see additional entries, record the microcode table address so you know when you have returned to the latest entry.

- ABCD indicates that a control unit or channel error has occurred and is four words long (see Figure 1).
- EFAB indicates that a drive error has occurred and is five words long (see Figure 3).

Word	Bits	Definition
0	0-15	A four-character constant ('ABCD') to identify each entry.
1	0-15	Microcode error code - (Control unit sense bytes 10 and 11)
2	0-3 4-7 8-15	Log Request Code Indicates the drive address Contains sense byte 9 - (Control unit flag byte)
3	0-7 8-15	Microcode error recovery action code Reserved

Figure 1. Control Unit or Channel Errors Table

SENSE BUILDER REQUEST LABELS

BUFLOG	Present buffered log (format 21). Counter overflow or unload.
CHECK 1	Check 1 recovery started at this time.
CUERR	Control unit error not attributable to a particular drive.
PERM	Recovery unsuccessful, present unit check with the data now in the sense table.
POST	Enter and error code and ERA code into the sense table.
POSTERA	Enter and ERA code only into the sense table.
POSTPERM	Single invocation yielding both POST and PERM.
RECOVER	Recovery successful, clear the sense table.
SNSRESET	Unequivocal clear (RESET) the sense tables.
SNSTRACE	Entry only in SNERRH, not in sense tables.

These are microcode operations and will be used to report errors to your next level of support.

Word 0	Word 1	Word 2	Word 3	Description
ABCD	vvvv	1xyy	zz--	Device side POSTPERM
ABCD	vvvv	2xyy	zz--	Device side POST
ABCD	0000	2xyy	zz--	Device side POSTERA
ABCD	0000	3x00	zz--	Device side RECOVER
ABCD	0000	4x00	zz--	Device side PERM
ABCD	0000	5x00	zz--	BUFLOG
ABCD	vvvv	6xyy	zz--	Device side SNSTRACE
ABCD	0000	7x00	00--	Device side SNSRESET
ABCD	vvvv	8xyy	zz--	CHECK1 trace entry
ABCD	vvvv	9xyy	zz--	Channel side POSTPERM
ABCD	0000	Axyy	zz--	Channel side POSTERA
ABCD	0000	Bx00	00--	Channel side RECOVER
ABCD	0000	Cx00	zz--	Channel side PERM
ABCD	vvvv	D0yy	zz--	CUERR
ABCD	vvvv	Exyy	zz--	Channel side SNSTRACE
ABCD	0000	Fx00	00--	Channel side SNSRESET

Figure 2. Control Unit or Channel Errors Words

vvvv Bits 0-15 of WORD 1 (see Figure 1).

x Bits 4-7 of WORD 2 (see Figure 1).

yy Bits 8-15 of WORD 2 (see Figure 1).

zz Bits 0-7 of WORD 3 (see Figure 1).

Word	Bits	Definition
0	0-15	A four-character constant ('EFAB') to identify each entry.
1	0-7 8-15	Indicates the drive ERP code. Indicates drive address.
2	0-7 8-15	Device flag 1. The device flag is associated with the first error that was detected for the current command. Device flag 2. The device flag is associated with the last error that was detected.
3	0-7 8-15	Device Command Code 1. Indicates that the command was active or last issued at the time of the first error that is defined in Word 3 bits 8 through 15. Device error code 1. This code is associated with the first error detected for the current command.
4	0-7 8-15	Device Command Code 2. Indicates that the command was active or last issued at the time of the second or last error that is defined in Word 4 bits 8 through 15. Device error code 2. This code is associated with the second or last error detected.

Figure 3. Drive Errors

Drive Status Bits 0-15

When Status In is active, the information on the bus from the drive is status bits 0-7 or 8-15 for the selected drive.

The status bits are sent to the control unit for the following conditions.

- At the end of any Initial Sequence
- During the Ending Sequence, of a Transfer Sequence

A status bit that is the result of a control unit initiated operation is sent only to that control unit. Status that is not associated with a control unit operation is sent to both control units.

Bit	Label	Description/Detail
0	Prep Move Executed	This bit is set when a Serial command execution begins. If the command cannot be completed, a Unit Check (UC) is set. The bit is reset after status is sent by the Parallel command. If the Parallel is a motion command, it must be the same command as the Serial command or UC is set, and no motion occurs.
1	Repositioning	This bit is set at the end of a motion command as the drive begins the repositioning operation. It stays set until the drive enters Stoplock. If a new command is received and the drive is at the wrong Stoplock position to execute the command, this bit is set and is in the initial status for that command. This bit is reset when the correct Stoplock is reached, or at Gap In time if the command stays connected and the command is in the opposite direction to the last command.
2	Not-Ready-To-Ready	Bit 2 is set when the drive goes into Stoplock after establishing tension and a radius during a load operation. If the drive Ready switch is active, or when placed in the active position, a CU Alert is sent to the control unit. Moving the Online/Offline switch to the online position on a loaded and ready drive will also set this bit. This bit is reset after status is sent during normal interface sequences by the first control unit to select the drive.
3	New Sector	Bit 3 is set when a Write command is in progress and a new sector number is detected from the drive table, as the command is executing. It is reset the next time status is sent to the control unit. The drive may find a new sector number after the control unit ends a Write operation. The ending status will not show the sector status but the initial status for the next command will.
4	Device End for Disconnected Command	This bit is set at the end of any disconnected command. A control unit Alert is sent on the interface that issued the command. UC may be active when this status is set. Bit 4 is reset after status is sent during normal interface operations. Enables Reg Funnel Parity checker after all LSR locations have been initialized to good parity before this bit is set. Microcode can change active conditions.
5	Device End	Bit 5 is set when the drive has completed any connected command. It is reset after status is sent during the ending sequence.
6	Unit Check	Bit 6 is set when the drive has detected an error condition that it can not recover from by itself. If a command was in process, it is sent with Device End. If no command was in process, UC will be in the initial status of the next command. The bit is reset after status is sent.
7	Manual Rewind/Unload	Bit 7 is set when tape tension is up, the Ready/Not Ready switch is in the inactive position and the rewind/unload switch is pressed.
8	Address High	This bit is active during status presentation when the drive address switch is set to hexadecimal address 8-F. It is reset after status is presented.
9	Ready	This bit is set after a Load-Op operation when tension is set, the machine reel has rotated at least one revolution, and BOT status is detected (except a mid-tape-load). It is reset by a Rewind-Unload operation or any drive error condition that causes a loss of tension or requires the motor stopping. Bit 1 is also set when the drive Ready switch activated if it had been inactive during the load operation.
10	Patched	This bit is set after a successful Patch load to a drive. It stays on until a power down condition, power on reset, or a Reset command.
11	Load Point	This bit is set when the drive motion is backward and the BOT is sensed. Drive motion is stopped and no backwards commands are accepted until BOT is reset with the next forward operation. If a data error is received while moving the tape forward from BOT, and a backward command is executed for ERP, BOT will not be detected.
12	File Protected Cartridge	This bit is set when a cartridge is loaded if the tape is file protected. It stays active until the current cartridge is unloaded and reset during an unload operation.
13	Tape Indicate (EOT) or Logical End of Tape	This bit is set when the drive motion is forward and EOT is sensed. Drive motion is not stopped and the EOT status stays active until a backward operation moves the tape backward and passes EOT.
14	Physical End of Tape (PEOT)	This bit is set when the microcode senses the physical end of tape. Tape motion is stopped and UC is set.
15	Reserved	

Drive External Registers

The following registers are drive external registers that can be accessed using the support diskette, "Register Display/Alter" option (see SDISK 1).

Note: Bit positions marked 'x' may be on or off. Only the important drive external registers and bits are defined.

	BIT							
REGISTER	0	1	2	3	4	5	6	7
X01	x	x	High Addr Bit	x	Rewind Switch	x	x	x
X02	x	x	Offline Switch	x	x	x	x	x
X03	Air Loss Switch	x	Over Temp Sw	x	x	Cartridge Present Sensor	x	R/Unload Switch
X07	x	x	LED Open Error	Message Display Error	Timer Error 1	Timer Error 2	Intf A Error	Intf B Error
X08	File Protect Sensor	Loader Extract Sensor	Tape Path SNSR-A	Tape Path SNSR-B	Cartridge Latched Sensor	x	x	x
X09	Rdy/Not Rdy Switch	x	Module Parity Error	Counter Parity Error	Module Parity Error	Gap CNT Parity Error	Timer Parity Error	x
X10	Serial Command Error	x	x	x	x	x	x	x
X11	Analog Cnvrter Error	File Motor Error	Machine Motor Error	x	Power Amp Error	Tension Loss	x	24V dc Failure
X20	x	x	x	x	x	Tag/Bus Parity Error	x	x
X25	0/8	1/9	2/A	Drive Address 3/B	4/C	5/D	6/E	7/F
X26	(8)	Drive ID (4)	(2)	(1)	x	(4)	Logical Address (2)	(1)
X27	x	x	x	x	x	x	INTFC A Selected	INTFC B Selected

Contents

CONTINUED ON OPER 2.

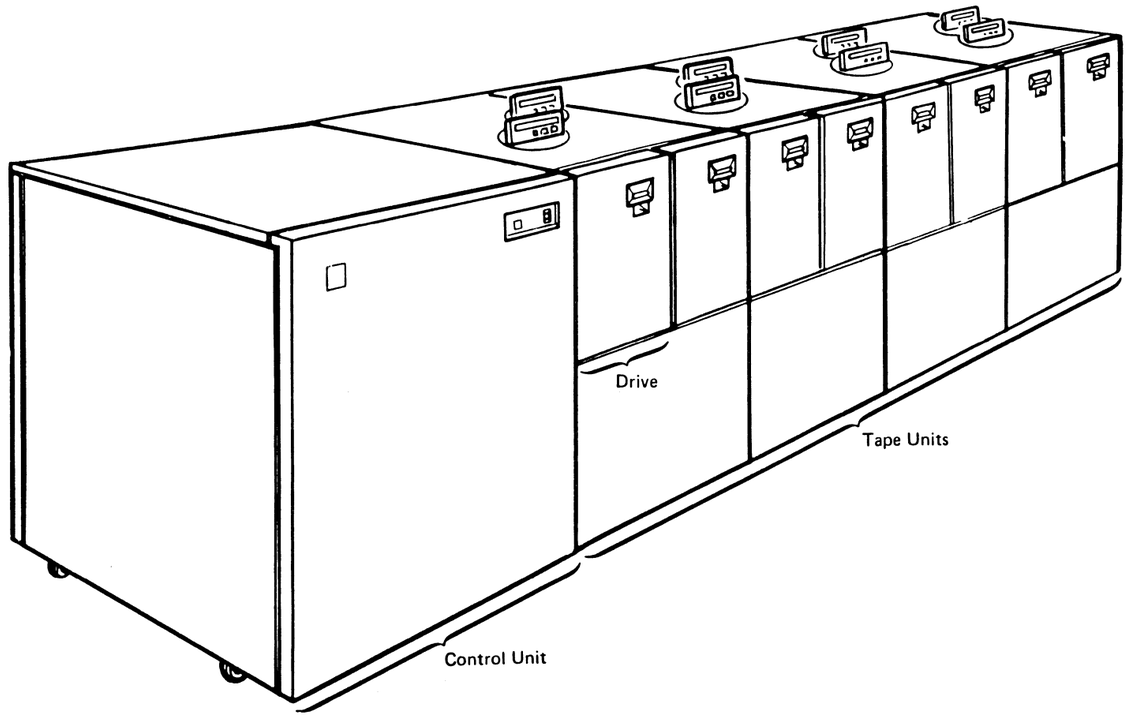
Introduction

This section explains the theory of operation for the 3480 tape subsystem. Topics included in this section are:

- **Control Unit,** which describes the functional areas of the control unit.
- **Tape Unit,** which describes the functional areas of the tape unit.
- **Drive,** which describes the functional areas of the drive (two in each tape unit).
- **Data Flow,** which describes the major data paths through the subsystem.
- **Subsystem Initialization,** which describes power on sequencing, initial microprogram load, and channel selection.
- **Subsystem Configuration,** which describes single and dual control unit configurations.
- **Channel Commands,** which describes the channel commands that can be accepted by the subsystem.
- **IML Diskette Drive,** which describes the IML diskette drive operation.

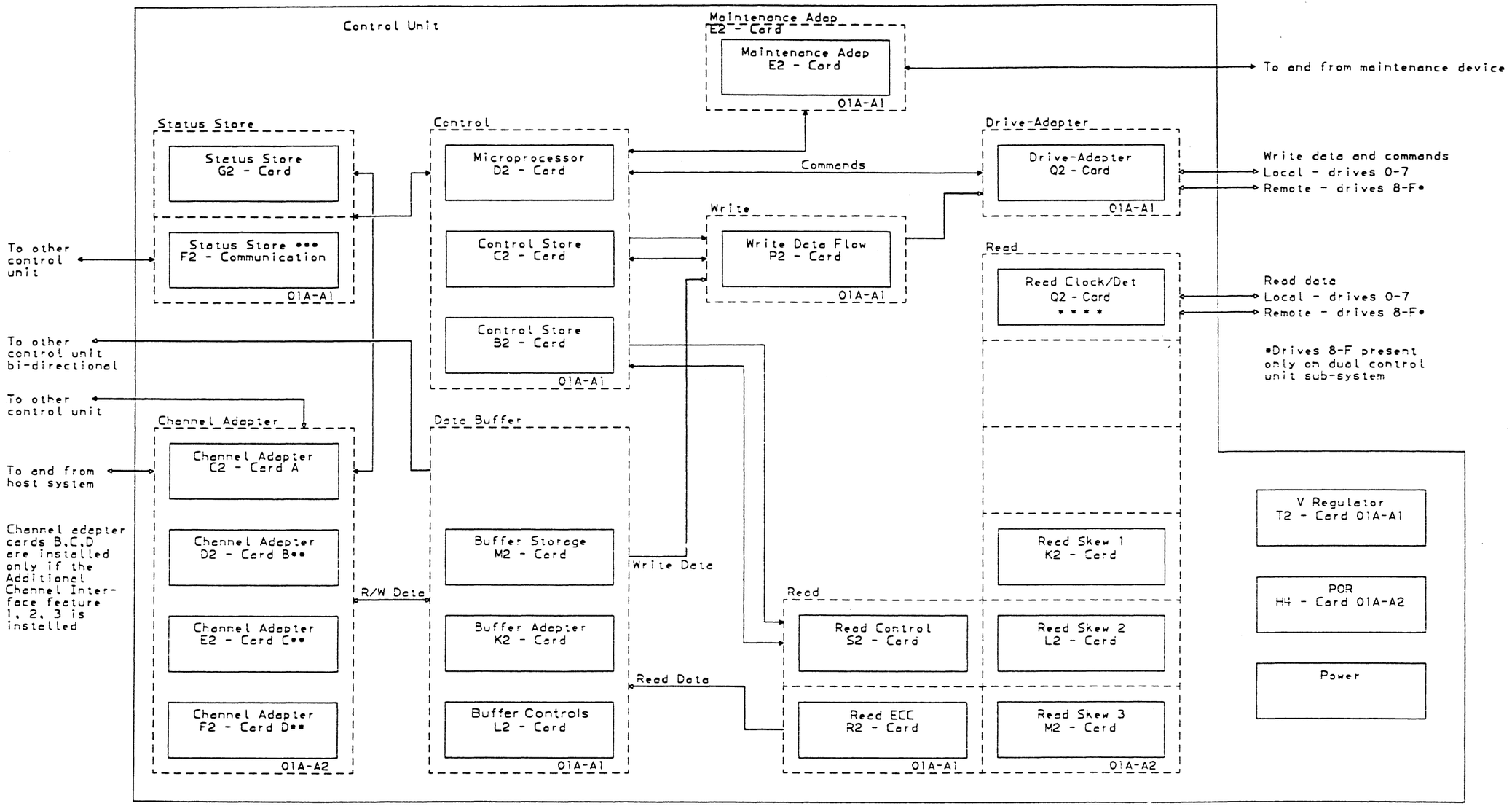
The flow of information in each topic is from general to detailed. An overview at the beginning of the topic introduces the topic and describes its content.

Diagrams and illustrations are used to supplement the theory text. The diagrams and illustrations show subsystem operations and data flow concepts; therefore, they may not duplicate actual machine circuits or total operations.



Control Unit Functional Area

This is a high level drawing showing theory only. For detail point-to-point wiring see the machine logic.



* * * This is a feature on the 3480 Model A11 and standard on the 3480 Model A22.

* * * * This FRU is EC Sensitive. See CARR-CU 4.

Control Unit (Continued)

The diagram on the preceding page shows the functional areas of the 3480 control unit. This topic explains the purpose of the functional areas. A brief description of the control unit power components is also included.

The control unit functional areas can be separated into two categories: data handling and control.

The **data handling** functional areas provide the data paths to transfer data between the host system and the drives for read and write operations. The bold lines in the diagram identify the read and write data paths. The data handling areas include:

- Channel Adapter
- Data Buffer
- Write
- Read
- Drive Adapter

The **control** functional areas control the movement of data and information within the subsystem and between the subsystem and host system. The control areas include:

- Control
- Status Store
- Maintenance Adapter

Data Movement

The microprocessor, within the control functional area, controls data movement between the tape subsystem and host system, and the data flow within the subsystem.

The data buffer area contains user-programmed information. Components of the control unit operate asynchronously to process data in and out of the data buffer, schedule I/O operations with the host system, and controls drive operations and data flow.

When a buffered write operation occurs, data is transferred at channel data speed to the buffer. The controller signals the host channel that the data has been written on tape; although, in reality, the data is still in the buffer. When the control unit's workload permits scheduling work for the drive that the data was intended for, the data is transferred to the drive and written on tape.

During read operations the control unit pre-reads data from the drive into the data buffer. When the host requests the data from the subsystem, the control unit responds immediately and transfers the data to the host at channel speed.

Data Handling Functional Areas

Data handling functional areas provide the data paths to transfer data between the host system and the drives for read and write operations. The data handling area formats data to be sent to the drives. This area also processes data received from the drives to put it in a form that can be accepted by the host system. Error checking is also performed by the data handling functional areas.

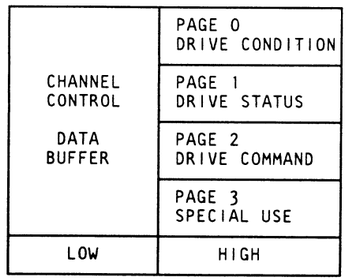
Channel Adapter

The channel adapter connects the control unit to a System/370 channel interface. The channel adapter monitors all channel sequences, either independently or along with the microprocessor, through the status store card.

There can be up to four channel adapters, A through D, installed in a control unit. The adapters are the same, and each adapter is on one logic card.

Channel Adapter RAM: The channel RAM keeps track of various control unit conditions, about which the channel adapter needs information to make decisions quickly. The RAM also monitors the status for each drive attached to the control unit that is transferred to the channel.

The channel adapter RAM can be thought of as being divided into two halves, a low half and a high half. The low half of the RAM is used as a buffer for control data to or from the channel. The high half of the RAM is divided into four pages. Page 0 is for storing drive conditions. Page 1 is for the channel status for each drive. Page 2 is used for the last channel command given to each drive. Page 3 is for special use. There is a channel adapter 'RAM' in each channel adapter.



PAGE size = 16 bytes
RAM size = 128 bytes

Channel Adapter Orders: The microprogram gives the channel adapter an order by writing an address into the channel adapter address register and then writing the order into the channel adapter order register.

In addition to orders from the microprocessor sent to the status store, there is a small set of orders from the channel adapter to the status store.

Malfunction Reset: Malfunction reset is microprogram controlled. If the microprogram determines that a specific channel adapter is causing nonrecoverable errors, the bit corresponding to the channel adapter is set in the channel modifier register on the status store card. This causes the 'malfunction reset' line to that channel adapter to become active. When this occurs, the channel adapter card logically disconnects from all interfaces and is reset. As long as the 'malfunction reset' line is active, the channel adapter is not active.

Channel Interface

The channel adapter recognizes the following channel sequences or conditions:

- Initial Selection
- Polling Sequence
- Ending Sequence
- Interface Disconnect
- Selective/System Reset
- Buffer Data Send/Receive
- Control Information Data Send/Receive
- Go Online
- Go Offline
- Check Reset

The channel interface is the standard System/370 interface. The tag and bus cables connect to shoe card connectors at the bottom of the control unit. All active line levels between the channel adapter and the shoe cards are minus.

Channel Adapter to Status Store Communication

The status store/channel adapter bus has two uses. First, it is the communication path between the microprogram and the channel adapter. Second, the status store supplies information to the channel adapter to determine initial status to be sent to the channel.

Microprogram-to-channel adapter communication is done by external registers. The contents of these registers are gated to the status store/channel adapter bus. Gating is controlled by status store.

The status store/channel adapter bus consists of nine bidirectional data bus lines, five response lines, and 10 control lines. All active status store/channel adapter communication lines are minus.

Channel Adapter to Data Buffer Communication

The channel adapter/buffer bus is the path for transferring customer data. There are two buses: one for the buffer, and one for the remote buffer. The microprogram controls which communication bus the channel adapter card uses at a given time. The microprogram assigns a buffer in the status store, and the channel adapter makes the correct connection to send/receive data.

The bi-directional data bus has nine data lines (eight lines for data and one for parity) and seven control lines. All active line levels except the "data OK to parity check" line are minus.

Control Unit (Continued)

Data Buffer

The data buffer contains a buffer control card, a buffer adapter card. and one or two buffer storage cards. The data buffer is temporary storage for data being transferred between the control unit and the channel. The buffer permits data transfer between the channel and the control unit at channel speed without the mechanical speed restrictions of the drives.

The buffer has data input and output buses. A write operation consists of sending data from the channel to the buffer, followed by sending data from the buffer to the write data flow path. A read operation consists of sending data from the read data flow path to the buffer, followed by sending data from the buffer to the channel. The microprocessor can read and write the buffer at the same time.

Buffer Data Write/Read: Data is written into the buffer from the read data flow path or channel through a CRC generator. Then it is moved to an input/output register and becomes two bytes wide. Next the data is sent through two single byte multiplexors to a random access memory (RAM). Data is sent from the RAM to storage through the multiplexers in 2-byte blocks of 16 bytes.

Data read from the buffer by the write data flow or channel follows a similar data path. Blocks of 16 bytes are sent from memory to the RAM through the multiplexors. From there it is sent to the two input/output registers through the multiplexers. The data is then sent through a CRC checker one byte at a time to either the write data flow or the channel.

The data transfer is started when the microprocessor sets a Read or Write command in either the buffer channel or device command registers. When the transfer is complete, the buffer sets the status in the buffer channel or device status registers, and sends an interrupt to the microprocessor, which then reads the status.

Buffer Control Card

The buffer control card contains external registers that monitor and record subsystem conditions and status. It also includes the channel buffer FRU and device buffer FRU registers. The buffer control card controls the data buffer, decodes commands and generates controls to the buffer address, buffer lines, and storage cards. When an error is detected, error registers are collected and read by the microprocessor over the external register bus. These registers become part of an error code that points to a possible FRU. All clock and reset signals needed by the buffer are received on this card and sent to the other buffer cards.

Error Checking: All bus, CRC, and parity errors are monitored by two error assembly circuits that set bits in the two buffer error registers. These registers are used to build an error code that can be read by the microprocessor. Parity checking is done on the external register data bus and errors are reported by way of the 'XR error' and 'XR active' lines. A hardware error causes a Check 2 error to occur.

Buffer Adapter Card

The buffer adapter card contains:

- Synchronization registers that communicate with the channel adapter and the read/write data bus.
- CRC generators and checkers to check for storage bit failures.
- Device and channel pointers.
- Device and channel stop registers.
- The buffer adapter card has been redesigned for the 4.5 Mb/s channel data rate, and replaces the old card when the 4.5 Mb/s channel data rate feature is installed.

The buffer adapter card compares the current and stop addresses of the devices and channel and sends the result to the buffer control card. Parity is checked for all data going in and out of storage, the read and write data paths, and the channel adapter.

Error Checking: Two error assembly circuits monitor all bus, CRC, and parity errors and set bits in two buffer error registers. These registers are used to build an error code that can be read by the microprocessor that points to a possible FRU. Parity checking is done on the XR data bus and errors are reported through the 'XR error' and 'XR active' lines. A hardware error is a Check 2 error.

Buffer Storage Cards

The buffer storage is EC sensitive and contains either one or two logic cards.

Single card buffers have sizes of 512K bytes, 1024K bytes, or 2048K bytes of storage in an 18 by 256K bits or 1024K bits matrix. Write and read operations are done in 16 byte biocks.

In the two card buffer storage, each card contains 256K bytes of storage in an 18 by 128K bit matrix. Write and read operations are done in 16 byte blocks.

Error Checking: Error checking is supplied by two signals leaving the buffer adapter card. Address parity is generated on the buffer adapter card and is then checked externally. The 'address valid' signal indicates that the address selected is valid and is assigned to the card.

Write

The write functional area contains the write data flow card that processes and controls the data that is to be recorded on tape. The microprocessor specifies the operation sequence, controls command execution in the drive, and checks the operation sequence. The data buffer stores the data until it is processed. The drive starts by responding with 'gap in' as a synchronizing start point. The processed data and one clock timing are sent to the device adapter, and the device adapter sends the data to the drive.

Initial processing is done in byte parallel form. ECC and CRC bytes are generated and combined with the data into a formatted sequence. A bit pattern of all ones is generated for preamble, postamble, and sync/resync symbols, and is inserted into the data format.

The combined data is serialized longitudinally by encoded byte and diagonally by bit. Nine 'write data' lines, one 'write data parity' line, and one 'clock' line are sent to the selected drive through the drive adapter.

Control lines and clock lines to the data flow section come from the control section of the write data flow card. Control lines and clock lines are used to control switching, modes of operation, and generation of special marks. Errors are detected and returned to the write data flow card for error reporting and sampling.

Data Buffer

The data buffer contains a buffer control card, a buffer adapter card, and one or two buffer storage cards. The data buffer is temporary storage for data being transferred between the control unit and the channel. The buffer permits data transfer between the channel and the control unit at channel speed without the mechanical speed restrictions of the drives.

The buffer has data input and output buses. A write operation consists of sending data from the channel to the buffer, followed by sending data from the buffer to the write data flow path. A read operation consists of sending data from the read data flow path to the buffer, followed by sending data from the buffer to the channel. The microprocessor can read and write the buffer at the same time.

Buffer Data Write/Read: Data is written into the buffer from the read data flow path or channel through a CRC generator. Then it is moved to an input/output register and becomes two bytes wide. Next the data is sent through two single byte multiplexors to a random access memory (RAM). Data is sent from the RAM to storage through the multiplexers in 2-byte blocks of 16 bytes.

Data read from the buffer by the write data flow or channel follows a similar data path. Blocks of 16 bytes are sent from memory to the RAM through the multiplexors. From there it is sent to the two input/output registers through the multiplexers. The data is then sent through a CRC checker one byte at a time to either the write data flow or the channel.

The data transfer is started when the microprocessor sets a Read or Write command in either the buffer channel or device command registers. When the transfer is complete, the buffer sets the status in the buffer channel or device status registers, and sends an interrupt to the microprocessor, which then reads the status.

Buffer Control Card

The buffer control card contains external registers that monitor and record subsystem conditions and status. It also includes the channel buffer FRU and device buffer FRU registers. The buffer control card controls the data buffer, decodes commands and generates controls to the buffer address, buffer lines, and storage cards. When an error is detected, error registers are collected and read by the microprocessor over the external register bus. These registers become part of an error code that points to a possible FRU. All clock and reset signals needed by the buffer are received on this card and sent to the other buffer cards.

Error Checking: All bus, CRC, and parity errors are monitored by two error assembly circuits that set bits in the two buffer error registers. These registers are used to build an error code that can be read by the microprocessor. Parity checking is done on the external register data bus and errors are reported by way of the 'XR error' and 'XR active' lines. A hardware error causes a Check 2 error to occur.

Buffer Adapter Card

The Buffer Adapter card is EC and Feature sensitive and can contain:

- Synchronization registers that communicate with the channel adapter and the read/write data bus.
- CRC generators and checkers to check for storage bit failures.
- Device and channel pointers.
- Device and channel stop registers.
- 4.5 Mb/s channel feature
- Improved Data Recording Capability feature

The buffer adapter card compares the current and stop addresses of the devices and channel and sends the result to the buffer control card. Parity is checked for all data going in and out of storage, the read and write data paths, and the channel adapter.

Error Checking: Two error assembly circuits monitor all bus, CRC, and parity errors and set bits in two buffer error registers. These registers are used to build an error code that can be read by the microprocessor that points to a possible FRU. Parity checking is done on the XR data bus and errors are reported through the 'XR error' and 'XR active' lines. A hardware error is a Check 2 error.

Buffer Storage Cards

The buffer storage is EC sensitive and contains either one or two logic cards.

Single card buffers have sizes of 512K bytes, 1024K bytes, or 2048K bytes of storage in an 18 by 256K bits or 1024K bits matrix. Write and read operations are done in 16 byte blocks.

In the two card buffer storage, each card contains 256K bytes of storage in an 18 by 128K bit matrix. Write and read operations are done in 16 byte blocks.

Error Checking: Error checking is supplied by two signals leaving the buffer adapter card. Address parity is generated on the buffer adapter card and is then checked externally. The 'address valid' signal indicates that the address selected is valid and is assigned to the card.

Write

The write functional area contains the write data flow card that processes and controls the data that is to be recorded on tape. The microprocessor specifies the operation sequence, controls command execution in the drive, and checks the operation sequence. The data buffer stores the data until it is processed. The drive starts by responding with 'gap in' as a synchronizing start point. The processed data and one clock timing are sent to the device adapter, and the device adapter sends the data to the drive.

Initial processing is done in byte parallel form. ECC and CRC bytes are generated and combined with the data into a formatted sequence. A bit pattern of all ones is generated for preamble, postamble, and sync/resync symbols, and is inserted into the data format.

The combined data is serialized longitudinally by encoded byte and diagonally by bit. Nine 'write data' lines, one 'write data parity' line, and one 'clock' line are sent to the selected drive through the drive adapter.

Control lines and clock lines to the data flow section come from the control section of the write data flow card. Control lines and clock lines are used to control switching, modes of operation, and generation of special marks. Errors are detected and returned to the write data flow card for error reporting and sampling.

0 0 0 0 0 0 0 0 0 0

Control Unit (Continued)

Read

The read area of the control unit consists of:

- One or three Read Detect Cards (EC sensitive)
- Three read deskew cards
- A read ECC correction card
- A read clock and format card.

The read area receives the read data from the drive, detects the encoded data, and detects the sync pattern. When the read area detects a sync pattern, the data is deserialized to byte format, deskewed, and the pointers are stored. The deskewed data is demodulated and placed in an ECC buffer. Then the data is transferred to the data buffer.

Read Clock/Detect Cards

The read data is sent from the drive to the read/clock detect cards. These cards detect the data and conditions, and recover the timing and signaling information read from six tracks of the tape.

Read Skew Cards

The read data is sent from the read/clock detect cards to the read deskew cards. The read deskew cards are used to deserialize and deskew data from the tape. Each card has six separate data paths; however, the three cards (18 data tracks) must communicate with each other to deskew the data.

Read ECC/CORR Card

The read ECC/CORR card receives its control and timing from the read clock/format card. Data and detection pointers are received from the read deskew cards. The output-corrected data is sent to the data buffer. The read ECC/CORR card:

- Demodulates the data
- Generates error syndromes, error patterns, and pointers
- Performs error correction
- Conducts CRC checking.

The syndrome generator receives 18 demodulated read data bytes one at a time, and generates four syndromes per data frame. Two syndromes are vertical syndrome bytes, and two are diagonal syndrome bytes.

The pointer system receives pointers to erroneous tracks from the read detection, deskew, demodulation, and error pattern generators. The pointer values are stored in registers, and sent to the error pattern generators in the correct format. The ECC/CORR card also signals the skew buffer to dead track any tracks with continuous errors.

The error pattern generation system consists of two error pattern generators, one generator for each group of nine tracks. The generation system uses syndromes from the syndrome generator and the pointers from the pointer system to generate error patterns.

The correction system deserializes the error patterns from the error pattern generators. The corrected data byte is then stored in the correction register, and sent to the data buffer and clock and format card.

A 16-bit Cyclic Redundancy Check (CRC) character is generated by the write data flow card when the data record is written on tape. The check characters are generated for all data bytes and resynchronization data patterns. During a read operation, the same CRC character should be generated. After reading the check character, the CRC register should equal zero. If the CRC register does not equal zero, a read error is indicated.

Read Clock and Format Card

The read clock and format card supplies clock timings and control for the read data flow, and communicates with the microprocessor. The read clock and format card controls when the deskew will read out, and identifies synchronization and resynchronization bytes. This card also supplies the control lines and clock timings for the read ECC card.

Drive-Adapter

The drive-adapter supplies the communication link between the control unit and its attached drives. With a two control unit subsystem configuration, dual control unit communication compatibility provides a second communication path for up to eight additional drives for each control unit. Therefore, any control unit can communicate with up to 16 drives in the maximum configuration. See the write-up on Dual Control Unit subsystems in this section.

The drive-adapter card is controlled by the microprocessor. The microprocessor writes in external registers on the drive-adapter card to set up the communication paths.

Control Unit (Continued)

Control Functional Areas

The control functional areas control the movement of data within the subsystem and between the subsystem and host system. In addition, these areas provide for communication between functional areas and between control units in a dual control unit subsystem configuration. The control areas also provide for error logging and status information transfer to the host system.

Control

The microprocessor card in the control functional area contains a microprocessor, local storage register, and associated logic for control and communications with the other areas of the control unit. This card also contains all processor external registers, the external interrupt hardware, and most of the processor error detection and reporting logic. The processor controls and keeps track of control unit operations through external registers via the external register bus.

Control storage consists of tables accessible by the microprogram and the microprocessor. Control storage also contains the initial microprogram load (IML) data after it has been loaded. Any time the microprocessor needs the microprogram to perform a function, it communicates with control storage to obtain the instructions. Control storage uses additional storage contained on the array card.

Status Store

The status store functional area provides a common area in the control unit to store status information. Status information is used by the microprocessor and channel adapter areas for allocation of common resources. The status store area also provides a communication path between the microprocessor and channel adapter. The status store communication card contains the logic that provides a communication path between two control units when two control units are connected as a single subsystem.

All machines are shipped with the status store card. The status store communication card is a feature on the 3480 Model A11 and standard on the 3480 Model A22. A status store card and status store communication card are required for a dual control unit configuration. The status store card contains the microprocessor bus, the channel adapter bus, the controlling logic, and the status store storage.

Status Store/Channel Adapter Communications

Status store communicates with the channel adapters by polling. Status store polls each channel adapter (A-D) in sequence.

The status store/channel adapter bus has two uses. First, it is the path by which the microcode communicates with the channel adapter. Second, it supplies information to the channel adapter that determines the initial status to be sent to the channel.

Microprogram-to-channel adapter communication is done through external registers. The content of these registers is gated to the status store/channel adapter bus. Gating is controlled by status store.

Maintenance Adapter

The maintenance adapter provides a way for the maintenance device (MD) to monitor and change the control unit's status. The maintenance adapter card enables the MD to read or write data stored in control storage and to control the microprocessor. The maintenance adapter card performs the basic communication function on the MD bus, and provides a bus for command and data transfer between the MD microprogram and external registers. The maintenance adapter card processes these Check 1 error conditions:

- Stopping the microprocessor
- Disconnecting the channels from the subsystem
- Starting the microprocessor under specific conditions.

The maintenance adapter card receives and decodes commands from an MD to:

- Perform the microprocessor control function
- Read and write control storage
- Detect and trap error conditions
- Send and receive commands and data to and from the MD microprogram for maintenance purposes.

Maintenance Adapter Registers

The following registers are contained in the maintenance adapter card logic:

- Maintenance control
- Maintenance status byte
- Maintenance data out
- Maintenance data in
- Maintenance tag out.

The registers are for temporary storage of control and status information, and data used by the maintenance device for trouble analysis.

MD Serializer/Deserializer

The MD serializer/deserializer is a shift register on the maintenance adapter card that converts serial data from the maintenance device to a parallel format for command decoding or for the microprocessor. When data and commands are to be sent to the MD, the data is converted from parallel to serial data.

Error Checking

The maintenance adapter monitors Check 1 errors. A Check 1 error is a hard microprocessor error in which the integrity of the subsystem is suspect.

A Check 2 error is a hardware-detected error. Any of the control unit cards may recognize parity errors or other errors. These errors activate the Check 2 error line to the maintenance adapter and microprocessor. The microprocessor searches for Check 2 errors during normal operation.

Power

The power area of the control unit contains an ac power supply and a dc power supply. The ac power supply provides power for the dc power supply, fans, and ac power for the tape units. The dc power supply supplies power to the control unit. Tape unit dc power is developed in each tape unit dc power supply.

Voltage Regulator

The voltage regulator card controls the voltages needed for the storage cards in the control unit.

Power-on-Reset/UV Detector

The power-on-reset (POR) card contains the POR circuits and the under voltage (UV) circuits. In addition to resetting the control unit circuits during a power-on, the POR and UV pulses are used to supply POR to the channels. A POR during a power down clamps the channel interface off before the loss of power. During a power up sequence, the channel interface is held off for approximately 800 ms to permit the voltages to stabilize.

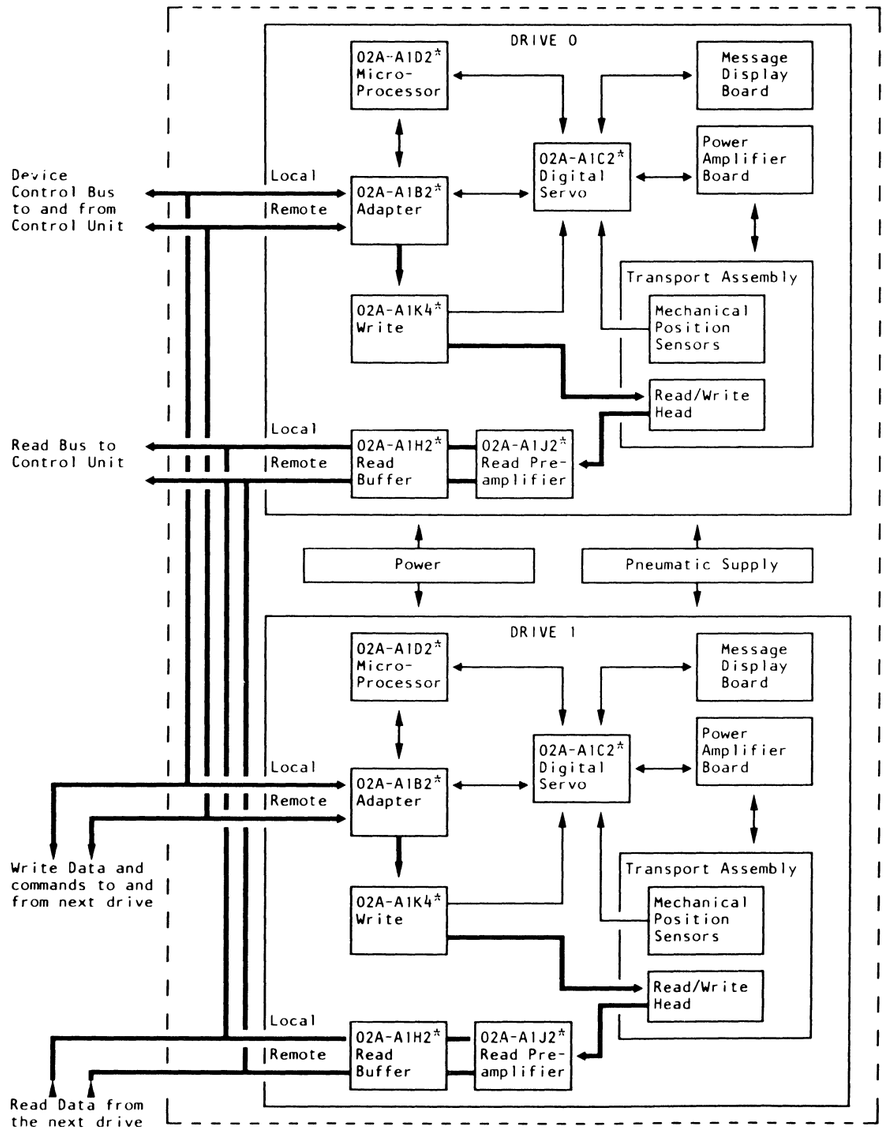
Tape Unit

Tape Unit Diagram

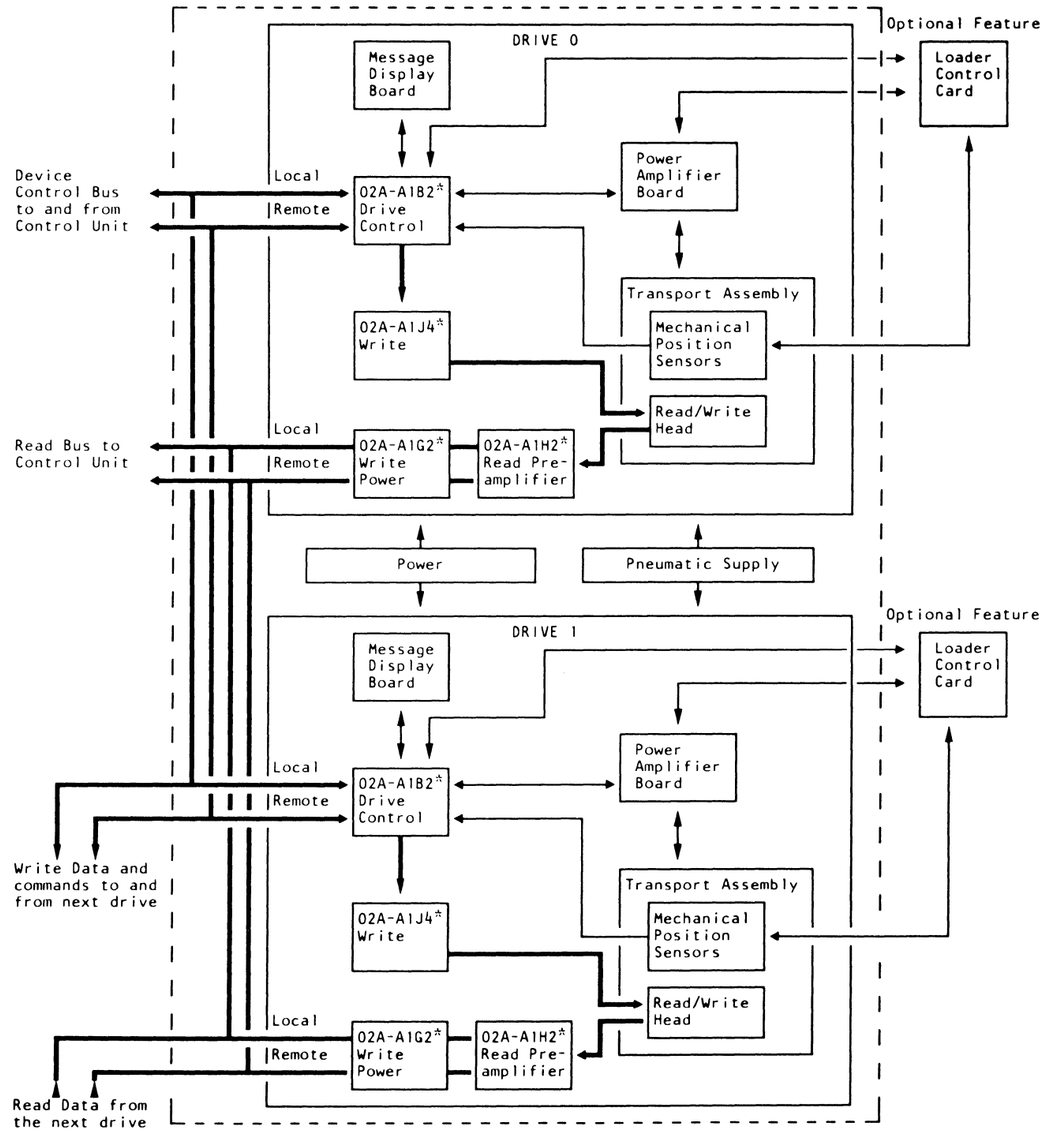
These are high level drawings showing theory only. For detailed point-to-point wiring see the machine logics.

* This FRU is EC sensitive. See CARR-DR 4.

TAPE UNIT WITHOUT EC 333293 (See CARR-DR 4)



TAPE UNIT WITH EC 333293 (See CARR-DR 4)



* This FRU is EC sensitive.
See CARR-DR 4.

Logical Components

Each tape unit contains two drives and two groups of logical components that control tape movement and data transfer within the tape unit. Each drive and its associated logical and mechanical components operates independently; however, the power and pneumatic supplies are shared by both drives.

The diagram on the preceding page shows the components needed to load, move, and unload tape, and to write on and read from tape. This topic explains the purpose of these components along with a description of the tape unit power supply and pneumatic supply is also included in this topic. The drive's mechanical components, sensors, and tape movement operations are also described.

*Processor Card**

The processor card controls all functions within the drive. Write data and commands are received by the adapter card and are passed, under control of the processor, to the digital servo card and write card. Read data is read from the tape by the read head and sent to the read card, under control of the digital servo card, as directed by the processor. All motion controls are controlled by the digital card, power amplifier card, and the processor.

*Digital Servo Card**

Because the drive is a microprocessor based system operating in a real time mode, and because of the tight control that is needed to maintain proper tape tension and tape velocity, high speed control processing is required. The digital servo card is designed to relieve the processor of simple housekeeping work, which increases its availability to perform processing tasks.

The digital servo card serves as a buffer and the interconnections between the processor and the rest of the drive. It also gathers information from the various drive sensors, mechanical switches, and error lines from other cards and presents them to the processor.

*Adapter Card**

The drives can be logically attached to one or two control units. The adapter card contains two buses and the controls that permit communications between the drives and one or both control units.

In a dual control unit configuration, only one control unit at a time is permitted to communicate with a specific drive. The other control unit cannot access the drive until the first control unit has finished using the drive.

*Drive Control Card**

The drive control card controls all functions within the drive. Write data and commands are received by the adapter section and are passed, under control of the microprocessor section, to the digital servo section and the write card. Read data is read from the tape by the read head and sent to the read preamplifier card, under control of the digital servo section, as directed by the microprocessor section. All motion control is controlled by the digital servo section, power amplifier card, and the microprocessor card.

Microprocessor

The microprocessor section of the drive control card contains the microprocessor, storage for the local storage register, and associated logic for control and interconnections to the control unit.

Some external registers (XRs), the external interrupt hardware, and most of the microprocessor error detection and reporting logic are located in this part of the card.

The microprocessor performs microcode to control and monitor control unit activity through the external registers which are accessed by way of the external register interconnections.

Digital Servo

The digital servo section of the drive control card serves as a buffer and provides the connections to and from the microprocessor and the rest of the drive. The digital section of the card gathers information from the sensors, mechanical switches, and error lines from other cards in the drive and presents them to the drive microprocessor.

Because the drive is a microprocessor based operating system in a real time mode and because correct control is needed to maintain the correct tape tension and tape velocity, high speed control processing is needed. The digital servo section is designed to relieve the microprocessor of having to do certain simple housekeeping routines.

Adapter

The adapter section of the drive control card contains two buses and the controls that permit communication between the drive and one or both of the control units. A drive can attach to one or two control units.

In the two control unit environment, only one control unit is permitted to communicate with a specific drive at any one time. The other control unit cannot access the drive until the first control unit has finished its operation.

*Write Card**

The write card contains the 18 write drivers, the head connector, parity checking circuits, and error checking circuits that check for an open head or head cable, shorted write drivers, and various other write problems.

*Read Preamplifier Card**

The read card amplifies the 18 read signals generated at the read/write head. The read preamplifier card sends the read data to the control unit by way of read bus local or remote. The bus is selected by the control unit.

Power Amplifier Board

The power amplifier board accepts digital current inputs from the processor through the digital servo section of the digital servo card, converts them to analog signals and applies necessary gain and phase shifting to drive the reel motors.

The power amplifier board uses the input from the tension transducer to keep correct tension on the tape. The power amplifier board also controls power on, power off, and power on reset.

Message Display

The message display provides a means for the host system and the tape subsystem to communicate with the operator. The message display is a logic board with eight LEDs and two bar LEDs that displays messages that are sent from the processor through the digital servo card.

Power

The tape unit ac power is provided by the control unit ac supply. AC power is cabled from the control unit to the first tape unit then cabled from that tape unit to the next tape unit, and so on.

The dc power for the tape unit is developed in each tape units dc power supply. The dc power supply furnishes the power for both drives in that tape unit.

Loader Control Card

The automatic cartridge loader - loader control card has its own microprocessor and storage. The storage is loaded from the control unit IML diskette using the "Patching Path" each time the drive patches are loaded. This code is used by the loader control card to control the functions within the automatic cartridge loader. The loader control card uses the information from sensors, mechanical switches, and cards in the drive to control the loading and unloading of the tape cartridge.

Tape Unit (Continued)

Pneumatic Supply

The tape unit contains one pneumatic supply that is shared by both drives. The pressure side of the pneumatic supply consists of a pump, regulator, and an output filter. The vacuum side of the supply uses the same pump and an inlet filter.

Air under regulated pressure is distributed to the drive components through a plenum **4**, which acts as a buffer to ensure a constant supply to the components. A pressure sensor attached to the plenum monitors the air pressure and causes a Check 46 to occur if pressure is reduced because of a leak in a hose or a loss of air from the supply.

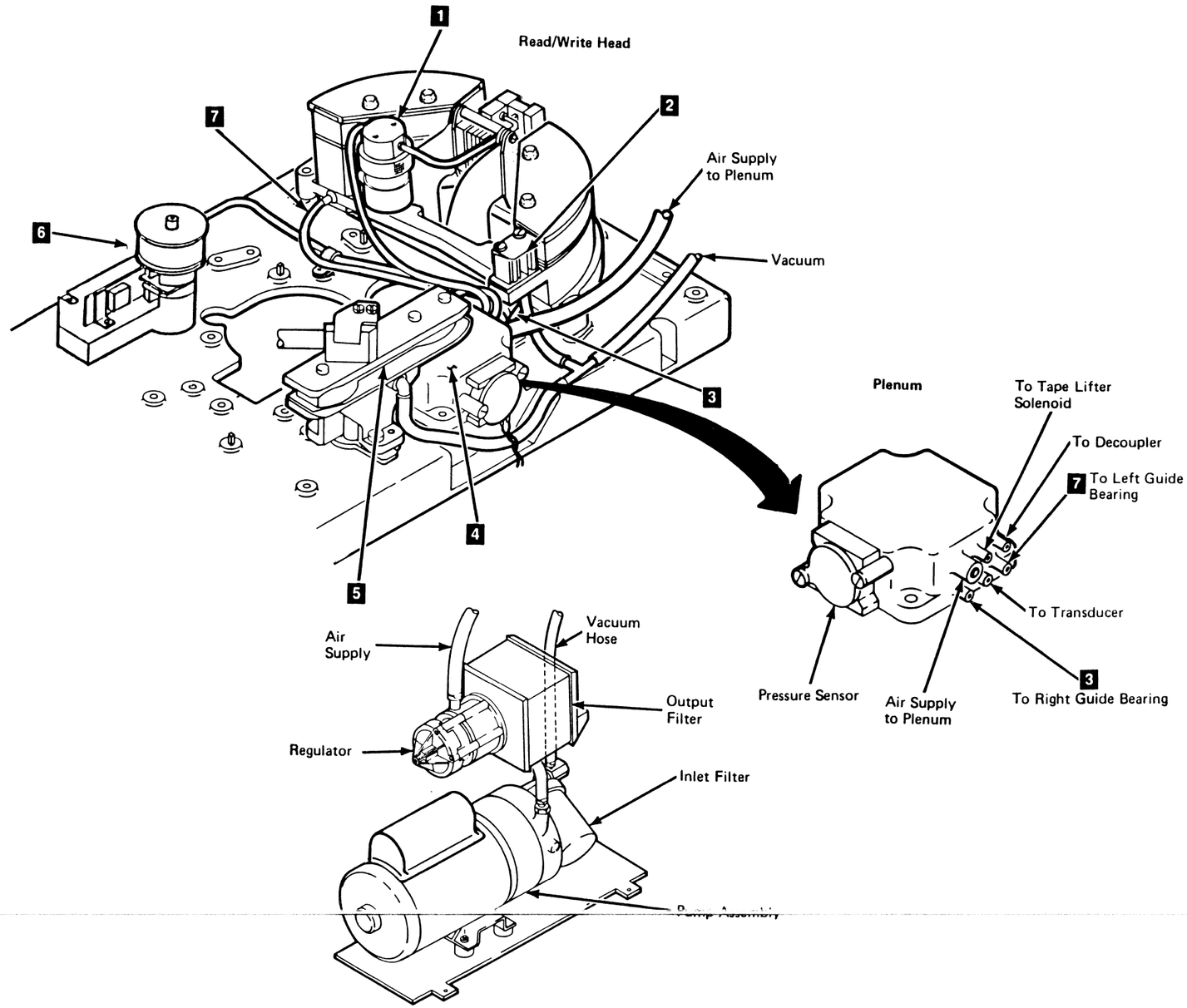
Air is supplied to the following bearing surfaces in the tape path to reduce friction and tape wear.

- Right Guide Bearing **3** (supply hose shown)
- Left Guide Bearing **7** (supply hose shown)
- Decoupler **5**
- Tension Transducer **6**.

Air is also supplied to the tape lifter solenoid **1**. The solenoid is energized whenever tape is not moving. When the solenoid is energized, air blows through a slot in the read write head and pushes the tape away from the head. If the solenoid fails to operate when tape motion is stopped, intermittent read write errors can occur.

Note: *A solenoid failure does not always cause an error check condition.*

The vacuum side of the pneumatic supply applies vacuum to the tape cleaner **2** and to the decoupler **5**. The tape cleaner removes particulate matter from the tape before it passes over the read write head. The vacuum applied to the decoupler pulls the tape into the decoupler. The decoupler provides a cushion that prevents the tape from stretching during start and stop operations. No error checking is directly associated with the vacuum side of the pneumatic supply. However, vacuum failures can cause intermittent read write errors.



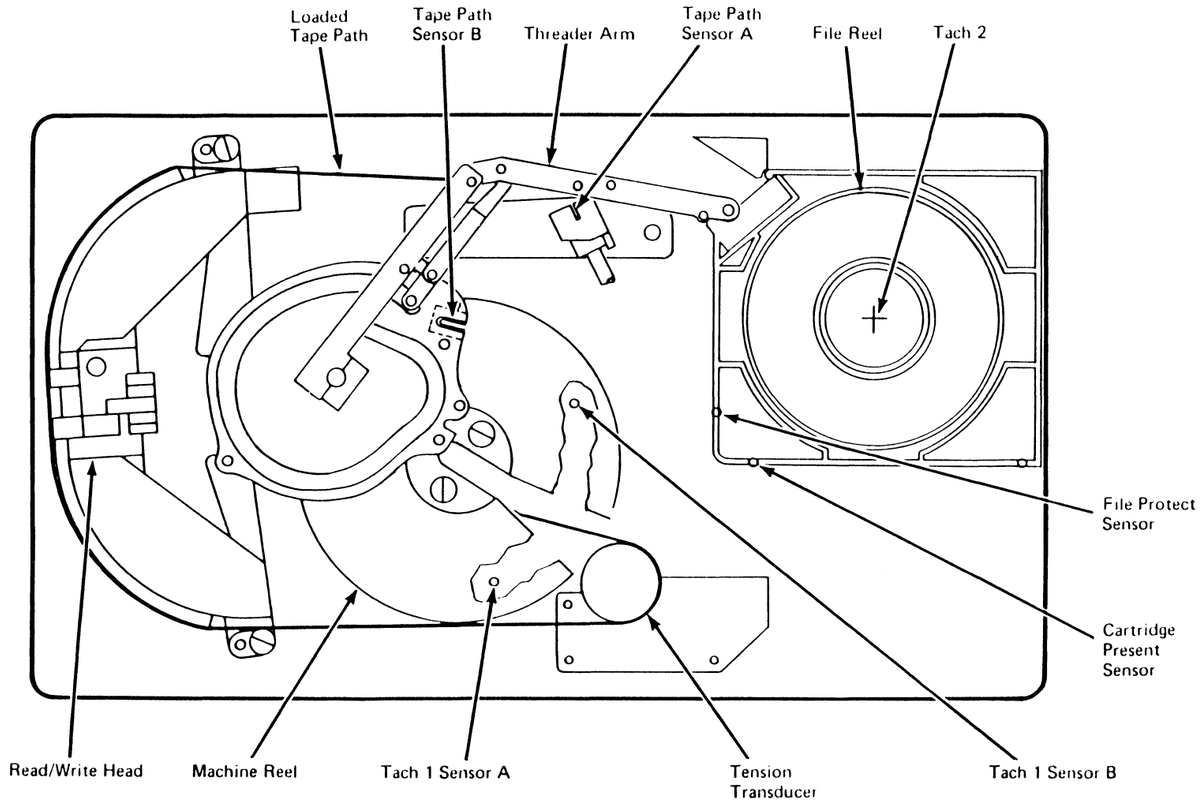
Tape Unit (Continued)

Drive

The drive contains the read/write head to read and write data, and the mechanical components, sensors, and motors to thread tape and move tape forward and backward. The processor controls all mechanical operations in the drive. The processor uses the digital servo and power amplifier to change digital signals used by the control logic to analog signals used by the drive motors.

Drive sensors feed back information to the digital servo to indicate motion errors and tape position so that the digital servo can modify the speed, velocity, or direction of tape motion. The following sensors monitor the drive:

- Cartridge Present Sensor - indicates that the tape cartridge has been inserted into the drive.
- Cartridge Latched Sensor - indicates that the cartridge is latched in place.
- Tape Path Sensor A - indicates that the tape leader block is at the file reel.
- Tape Path Sensor B - indicates that the tape leader block is at the machine reel.
- Machine Reel Tach Sensor A - senses the position of the machine reel. It is used in conjunction with Tach 1 sensor B to generate the 'tach 1' pulse.
- Machine Reel Tach Sensor B - senses the position of the machine reel. It is used in conjunction with Tach 1 sensor A.
- Tension Transducer - senses tape tension. Its output is used by the microprocessor to control the reel motor power amplifiers.
- File Reel Tachometer (Tach 2) - monitors the speed and direction of the file reel motor.



Tape Unit (Continued)

Tape Threading-Loading

Tape threading-loading is an automatic microprogram controlled operation that begins after a tape cartridge has been inserted and latched in the drive. The operation consists of:

- Sensor Test - Tests sensors and associated detection circuitry.
- ILS Test - Tests for interlayer slip.
- Thread-Load - Threading, loading, and positioning the tape at BOT.

Sensor Test

The sensor test is a diagnostic routine that tests the threading path sensors and the tension error detection circuits. The test is limited to sensors that are in a "light" (not covered) state at the time the cartridge is inserted. In addition, the test sets appropriate flags if a midtape load is required or if a cleaner cartridge has been inserted.

ILS Test

This test is performed to determine if an ILS condition exists in the cartridge before the processing of data. If this condition is detected, the control unit is instructed to issue a "Locate" command to a sector near EOT, followed by a "Rewind" command. This operation reestablishes correct tape tension on the reel.

- A start/reposition/stop loop starts.
- The acceleration rate for the start is 150 meters/sec (492.13 feet/sec).
- At 100% velocity, velocity deviation is checked at each of 32 tach-2's.
- If at any of the 32 tests made, the velocity is greater than 3.5% of nominal, an ILS condition exists.
- The above sequence is repeated ten times.
- An alert is issued to the control unit signaling load complete.
- If an ILS condition was detected, 'unit check' and the appropriate ERP code will be sent to the control unit.

Thread-Load

The thread-load operation begins by driving the thread motor in a forward direction in a pulsed mode. Pulsed mode provides velocity control for the threading mechanism. Backward bias is applied to the file reel motor to maintain tension on the tape during threading.

To thread tape, the carrier pin is extracted from the file reel by the threader mechanism **1**. At the same time that the threading mechanism starts to move, the machine reel is positioned (nulled) to permit proper entry of the tape carrier pin. The carrier pin, leader block, and tape are then pulled around the periphery of the tape path by the threader mechanism **2**. Finally, the carrier pin and leader block are housed in the machine reel **3**. Proper engagement of the carrier pin in the machine reel is ensured by a sensor at the machine reel home position.

When the threading operation is complete, the threader motor is stopped and the tape is moved forward, under microprogram control, to BOT. A Stoplock condition is activated at BOT and a 'not-ready to ready' alert is presented if the Ready/Not Ready switch is in the Ready position.

Tape Unloading

The tape unloading-rewinding operation starts when the Unload switch is pressed, and the Ready/Not Ready switch in the Not Ready position. Tape is rewound onto the file reel at high speed until BOT is detected.

Unload

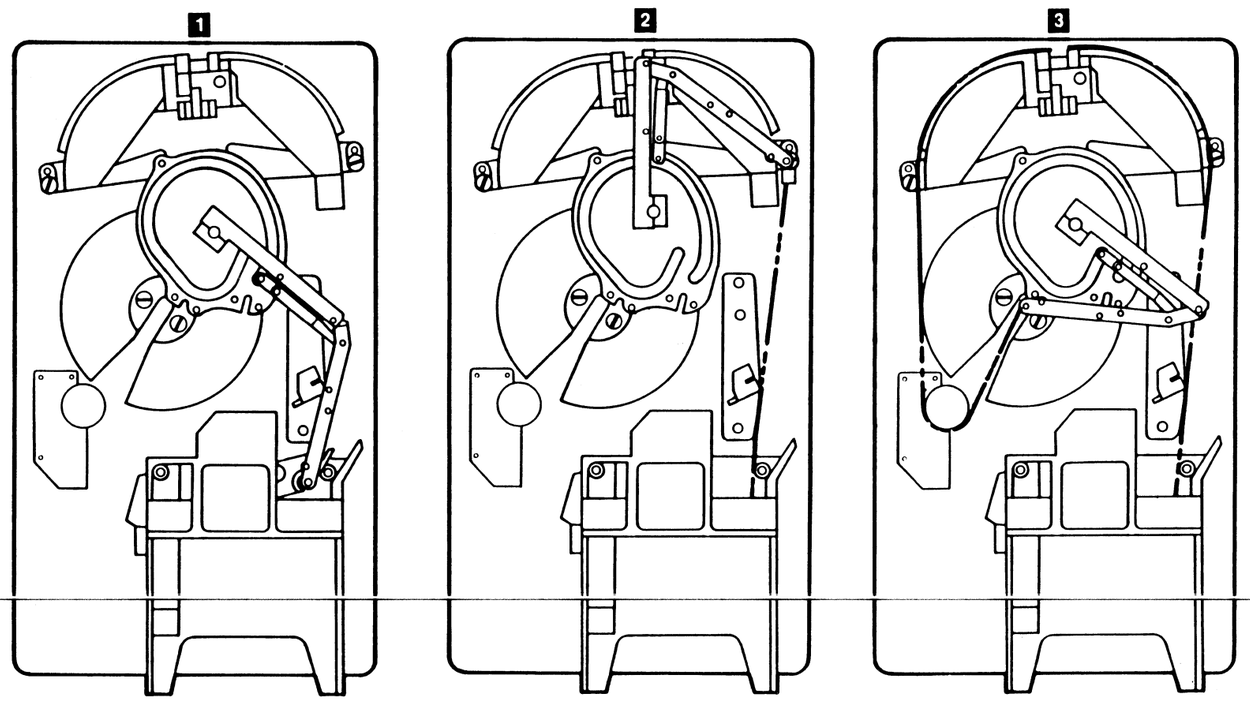
The unload (last wrap detect) sequence starts with the tape under tension, at BOT, and with 'rewind unload status' signal active. Stoplock and tension control are deactivated, and the tape is moved at low speed (less than one meter/second (3.28 feet/second)) to the last wrap null point. The last wrap null point is where the machine reel is positioned for the exit of the leader block and carrier pin.

When the tape reaches the last wrap null point, the leader block is withdrawn from the machine reel sufficiently to change the state of tape path sensor 'B'.

The machine reel is nulled to ensure proper exit of the leader block and carrier pin and a small backward bias is applied to the file reel motor to remove any slack in the tape. The thread motor is driven backward in pulsed mode. Increased bias is also applied to the file reel motor to maintain tape tension.

When the leader block is sensed at the cartridge home position, power is dropped from the file reel and threader motors, and the cartridge tray solenoid is energized. When the cartridge tray solenoid energizes, the tray cover is raised, which permits the cartridge to be removed from the drive.

Note: *The cartridge latch should be closed when the tape drive is not being used. (A cartridge need* **not** *be in the drive.) When the tape drive is needed, open the cartridge latch by pressing the Unload switch.*



Subsystem Initialization

This topic describes the power sequencing, initial microprogram load (IML), and channel selection operations.

Power Sequencing

Power sequencing for the tape subsystem is activated from the control unit. When power is applied, internal diagnostic tests check voltages. After the voltages have been checked, a general reset of the control unit and drive logic is performed. Finally, a basic function test of the control unit and drive logic is performed. Errors detected during the power on sequence are reported to the control unit.

When all tests have been made and the results have been reported to the control unit, the control unit IMLs itself from the IML diskette.

Initial Microprogram Load (IML)

After every power-on-reset, or when the IML button is pushed on an offline control unit, the control unit will IML itself from the IML diskette. The IML diskette is kept in the IML device at all times.

The control unit has a permanent microprogram that detects and reads the IML diskette information into the control storage area of the control unit logic. A read operation is performed from the diskette device and the data is sent to control storage.

If the diskette device cannot read the IML diskette, or read errors occur, the Control Unit Error Light turns on. Since the control unit is offline to the IML, no information is sent to the host system. When the host system attempts to vary the IML failed 3480 subsystem online, a host system message 'No Paths Available' occurs.

Errors that occur during the IML are saved in an area in the microcode. After the MD is connected (with the product diskette) the microcode checks this error field and creates an FSC that is used to troubleshoot the IML failure.

If no read errors occur, the control unit performs diagnostic tests to ensure that the microprogram has loaded without any errors and is executing correctly. If errors occur during the diagnostic tests, the 3480 and host system operates the same as with an IML failure with one exception. The difference is the FSC identified when the MD is connected points to the failing area found by the diagnostic instead of an IML failure.

If the IML and diagnostics complete successfully, the control unit wait light is on and the control unit error light is off. Pressing the control unit Online/Offline switch to online, causes the IML device to run again and load any necessary control unit or drive microcode patches. The control unit offline light then goes off, and the host system completes its vary online procedure.

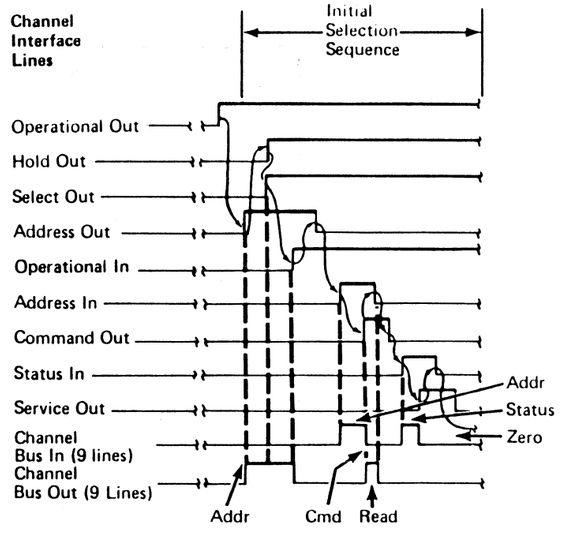
In a dual control unit configuration, each control unit is independent of the other control unit. Each control unit must be separately IML'ed. Any IML or IML diagnostic errors that occur are reported only in the failing control unit.

Channel Initial Selection

When the host system needs to access a drive, it starts a selection sequence on the data channel. The timing chart at right shows when the channel interface lines are activated and deactivated during an initial selection sequence.

Initial selection begins by activating the 'operational out', 'hold out', and 'address out' lines. An address byte that contains the address of the control unit and drive is placed on the 'bus out' interface line. The 'select out' line is activated and sent to all the units on that data channel, and then is sent to the next control unit. Each control unit, in sequence, compares the address with its own. The control unit with the correct address traps the selection and answers by activating the 'operational in' and 'address in' lines, and by placing its address on the 'bus in' line. The data channel checks the address returned and, if correct, places a command byte on the 'bus out' line and activates the 'command out' line. The microprocessor in the control unit, after checking the device status, activates the 'status in' line and places status (normally zero) on the 'bus in' line. The data channel activates the 'service out' line to indicate that it has received the status byte.

At this point, the microprocessor is ready to start decoding commands and processing data.



External Registers Data Flow/Error Detection

The external registers (XRs) are used by the microprocessor that has a 16 bit (one word) instruction to communicate, through the channel adapter to the channel, and through the device adapter to the drive.

The XRs are used to control various operations in the functional areas and also for error retention. The XRs are eight bits, plus parity, in size and are used in read-only, write-only, or read/write operations. All XR errors are reported to either the maintenance adapter (MA) or the microprocessor (MP) card.

There are seven functional areas in the control unit that use the XRs. The buffer adapter and the buffer control card are in the same functional area.

- Status Store
- Buffer
- Microprocessor
- Write Data Flow
- Device Interconnections
- Read Data Flow
- Maintenance adapter

The XRs are addressed by using an XR address bus (a six bit bus) which uses bits 0-4 and a P bit for **even parity** together with two 'extend' bits (0-1). Extend bits 0 and 1 are in fact the PCR register bits 6 and 7. See Figure 1. These bits are sent to each functional area from the MP card. They are not parity checked.

External Register Addressing

There is a five bit address in all microprocessor XR instructions permitting up to 32 XRs to be addressed (hexadecimal 0-1F).

Addresses are 'extended' by using processor control register (PCR) bits 6 and 7 (extend bits 0 and 1). 128 addresses can be selected by addressing one of four register pages. Each page contains 32 addresses.

The 'extend' bits are not part of the address bus and are not parity checked, but are sent to each functional area from the MP card.

PCR Register Bits 6 and 7		
'Extend Bits 0 and 1'		
0	0	Page A
0	1	Page B
1	0	Page C
1	1	Page D

Figure 1. Page Selection

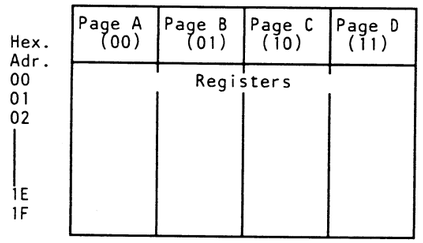


Figure 2. Register Addressing

The XR address is common to all cards containing XRs, except the buffer control card. The buffer control card receives only the P-bit from the XR address bus. XR address bits 0-4 are received from the buffer adapter card through a top card connector.

Moving Data

Data is moved using three data buses:

- XR Data Bus A
- XR Data Bus B
- XR MP Bus

The XR MP bus is internal to the MP card. Each data bus is eight bits plus a parity bit for odd parity. The XR Data Bus A moves data between the MA, DI, SS, and the MP card. The XR Data Bus B moves data between the MP, BA, DF, and the RC cards.

Clocking for the XRs is provided by the CS card. There are 22 sub cycles (S0-S21), each sub cycle is 23.1667 ns.

Note: There is an XR timing chart on EAD 8 and a drawing on EAD 2696 that may help in understanding the following sequence.

External Register Operation

The following sequence addresses, reads, and writes into a selected external register.

1. The address is placed on the XR address bus by the MP card.

   a. The bus contains bits 0-4, P with **even parity**.

   b. The 'extend' bits (0-1) are also sent to each functional area to select the page that the addressed register is on.

   c. Each functional area decodes the data on the XR address bus, together with the 'extend' bits, to determine if one of its registers is being addressed.

   d. An 'XR addressed' line is activated when an XR in a functional area is selected.

      'XR addressed' is not generated if the XR address bus has bad parity.

   e. The XR addressed lines go to the MA card where they are checked for **only one** active line.

2. If the instruction specified that an XR was to be read, an XR gate is generated permitting the addressed area to gate the data on the XR data bus.

   a. If an XR read is occurring, 'XR addressed clock' line is generated and 'XR error ungated' line is sampled at S20-S21 time. The MA card uses 'XR addressed clock' line to set the XR functional area error latch (MTI bit 4) and to latch the functional area (MP) 'XR addressed' lines if **only one** functional area is not detected.

   b. The latched XR addressed lines are read through the MDI register when the read XR addressed bits latch (MTO bit 2) is on.

   c. The MA card also uses the 'XR addressed clock' line to set the MP error latch (MTI bit 3) and MA error latch (MTI bit 5) if the XR address bus has bad parity.

   d. If 'XR error ungated' line is active, the processor sets the XR error functional area read error latch (PER bit 5). 'XR error ungated' line must not be active during S20-S21 time to avoid an error.

3. If the instruction specified that an XR was to be written, 'XR write gate' line is activated at S0-S13 time and the processor places the write data on all three XR data buses. The functional area's gate the 'XR data bus' lines on their internal buses.

4. If the XR address bus and the XR address extend bits have addressed a write XR (XR write gate is on), the functional area register activates its XR addressed line (MP). An 'XR addressed' line is not generated if the XR address bus has bad parity.

5. The MA card checks the XR addressed line for **only one** line being active. An 'XR error ungated' line is activated if the addressed area detects that the write data had bad parity. An 'error ungated' line is activated if the MA card detects bad parity on the XR address bus, or if more than one XR addressed line is active.

At S5-S7 time the 'XR load' line is activated by the control store card. The XRA register is loaded with XR address extend bits 0 and 1, and the five bits plus parity of the XR address bus. If an XR was read during the first half of the cycle and the data latched in the scan path had bad parity, the XR read parity latch (PER bit 4) is set. The XR functional area write error latch (PER bit 6) is set if XR write is occurring and 'XR error ungated' line is active at S9-S10 time.

The three XR errors indicated by PER bits 4, 5, and 6 causes the 'XR error latched' line to be active. XR error latched being active causes the 'check 2' line to be active and also activates the 'MP external interrupt 0' line and stops the XRA register from being updated. The XRA register contains the address of the register that was used when the error occurred.

Check 2 is used by the functional area's to indicate to the microcode that some error has occurred internal to their area.

XR Detected Errors

CHK 1 Errors

ERB Bit 0 is set:

If there is an XR address compare error. An address on XR address bus does not equal the address that the instruction called for.

ERB Bit 1 is set:

If the MP card (registers IMR or PDR) has bad parity.

ERA Bit 6 is set:

If MP internal XR address bus has bad parity.

CHK 2 Errors

MTI Bit 3 is set:

If the MP XR was found to have a parity error.

MTI Bit 4 is set:

If no XR or more than one XR addressed line is active.

MTI Bit 5 is set:

If the XR address bus has bad parity.

PER Bit 4 is set:

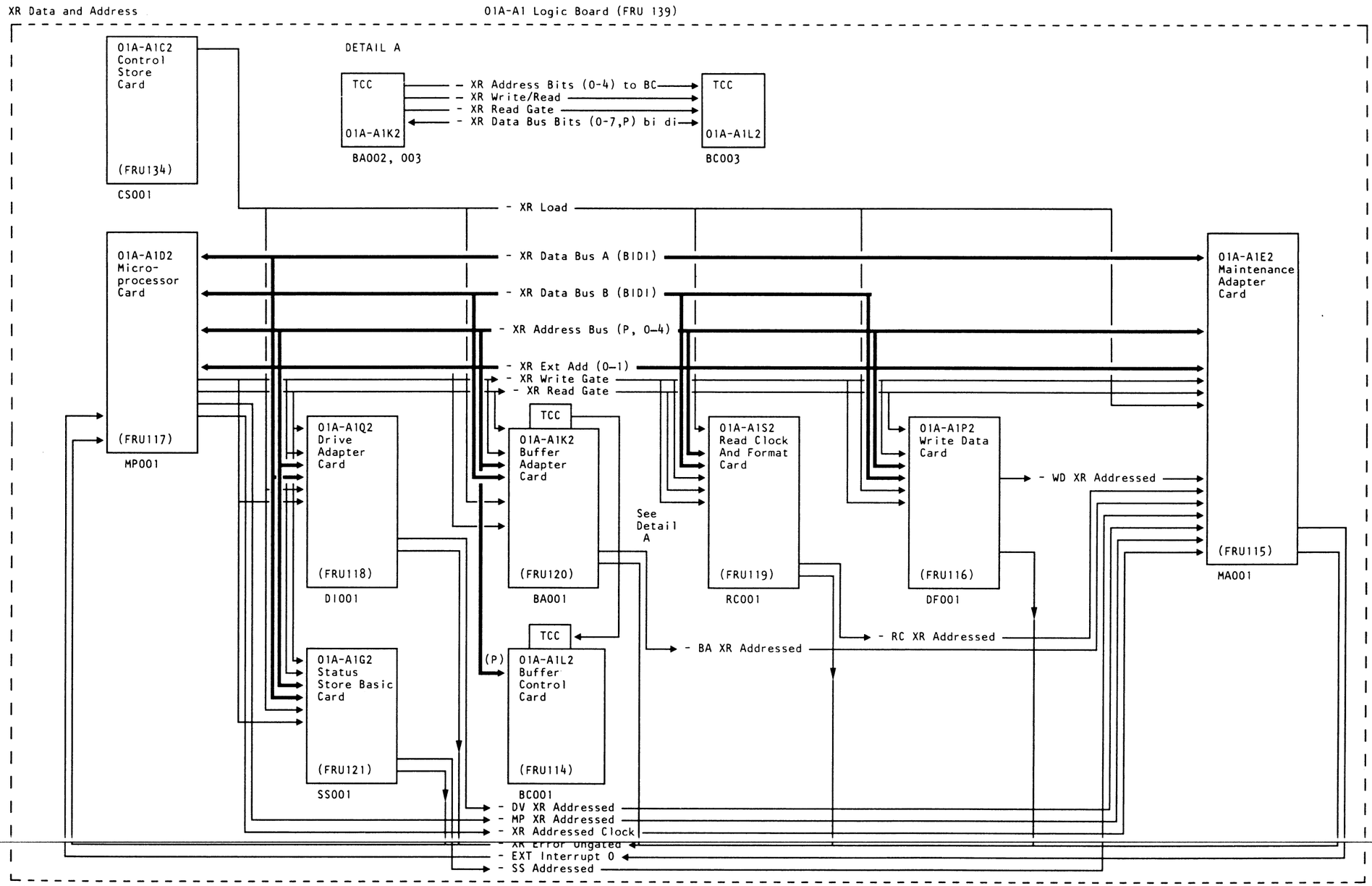
If a read data parity error is detected by the MP card during an XR read (sets PSR bit 0).

PER Bit 5 is set:

If the functional area containing the XR that was addressed detects bad parity on a read (sets PSR bit 0).

PER Bit 6 is set:

If the functional area containing the XR that was addressed detects bad parity during an XR write.



Point-to-point wiring on a board is shown on the Control Unit and/or Drive net wire lists.

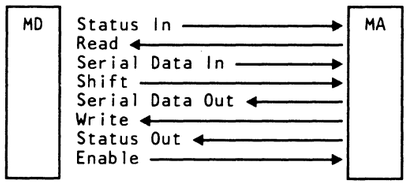
The maintenance device (MD) is the primary tool for servicing the 3480 subsystem. It executes maintenance analysis programs contained on a diskette and has a communication path to the 3480 subsystems maintenance adapter (MA) card. This communication path is used to send commands to the MA from the MD where they are recognized as control or data transfer functions.

The direction of the data movement is determined by the type of function specified by the MA (read/write) and by the type of function specified by the MD program (get/put). The communication path signal lines used for control of data byte movement differs for MD 'get' or MD 'put' type functions.

Command and data bytes are sent serially by bit from the MD to the MA. Data and status bytes are received by the MD on a separate serial data line.

The purpose of this description is to give information to explain the function of each signal line and its use for specific operations. The signal lines are named from the Product Maintenance Adapter Perspective (such as, Serial Data In). The signal levels used are +5 V dc to 0 V dc with +5 V dc being the inactive level.

MD to/from MA Communication Path Signal Lines



Status In

This line is activated at the start of an operation by the MD to signal the MA to respond with 'read' and to receive a command. It is also activated when all data bytes have been sent or received by the MD to signal the end of the operation. The command byte sent for the second 'status in' sequence is 'end-of-message' (EOM) (X'40'). This line is deactivated when the 'read' signal goes inactive.

Read

This line is activated by the MA in response to 'status in' and is used to request data bytes during an MD 'put' operation. It is a signal to the MD to start sending shift pulses. It must go inactive at the center (+ edge) of the 9th shift pulse. This line goes active then inactive for each byte that is sent by the MD.

Serial Data In

This line is used to send serial data bits from the MD serializer/deserializer (SERDES) register to the MA SERDES register. It changes on the leading (-) edge of the 'shift' pulse and it is valid for the MA to sample it on the trailing (+) edge. The bit order is 0-7, then the 'P' bit is last. See Figure 1.

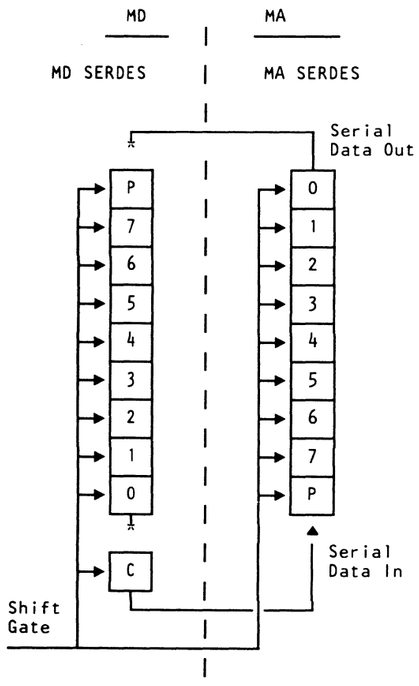


Figure 1. Shifting Bits Through SERDES

Shift

9600 bits per second (bps) pulses (104 microseconds) are placed on this line by the MD in response to the 'read' or 'write' signals from the MA. These pulses control the movement of SERDES register bits to and from the MD and the MA. Shift pulses also appear during the 'diagnostic wrap' part of an MD port 'open' operation. See Figure 1.

Serial Data Out

This line is used to send serial data bits from the MA SERDES register to the MD SERDES register. It changes on the trailing (+) edge of the shift pulse and it is valid for the MD to sample it on the leading (-) edge. The bit order is 0-7, then the 'P' bit is last. Since the MD samples for bit 0 on the leading edge (-) of the first shift pulse, the data in the MA SERDES must be valid before the 'write' line is activated.

Write

This line is activated by the MA to send data to the MD when a 'write' type command is received in an MD 'get' operation. It is a signal to the MD to start sending shift pulses. It must go inactive at the center (+) edge of the 9th shift pulse. This line goes active then inactive for each byte that is received by the MD. It is also used in combination with 'status out' to end an MD 'put' operation in progress or asynchronously to send a status byte from the MA to the MD.

Status Out

This line is used together with the 'write' line to end an MD 'put' operation if the MA detects bad parity on an incoming data or command byte. 'Write' and 'status out' may be activated when there is no other activity and the MD will send shift pulses to move a single byte of status information from the MA to the MD. This asynchronous operation occurs following all commands that are executed by the 3480 microcode. See Figure 5 on the following page.

Enable

This line is activated by the MD during an MD port 'open' operation. It is monitored by the MA card indicating that the MD is connected. It must be active during all communication path operations.

MD to MA Communication Path Error Checking

Parity Error Detection

Data received by the MD in a 'get' operation from the MA is tested for an odd number of bits (vertical redundancy). If an even number of bits are detected, the operation is ended with a 'status in' command sequence and an error condition sent to the MD program.

The MA card also checks the parity of the data it receives from the MD. If an even number of bits are detected, the MA ends the operation by activating 'status out' and 'write' at the end of the 9th bit period. This error condition is also indicated by a bit in the MA cards MTI register, and the 'status out' sequence sets error bits in the MD for detection by its program.

Communication Path Signal Sequence Error Detection

The MD checks for the correct signal during 'get' and 'put' operations. If 'read' is the expected signal, and 'write' appears without 'status out', an error is reported by the MD program.

MD Internal Adapter Error Detection

The MD checks for the correct internal interrupt sequence during all port operations and errors are reported by the MD program.

Maintenance Device to 3480 Maintenance Adapter Communication Path (Continued)

MD to MA Communication Path Operations

- Open with Diagnostic External Wrap
- Put from the MD to the MA
- Get from the MA to the MD.

1. **Open:** This function is executed in the MD and it resets the MD hardware adapter, activates the 'enable' line, and tests the data path between the MD and the MA. This test is accomplished by shifting a data byte (X'5A') from the MD SERDES through the 'serial data in' path to the MA SERDES, and returns the data to the MD SERDES through the 'serial data out' path . This test requires 18 shift pulses. See Figure 2.

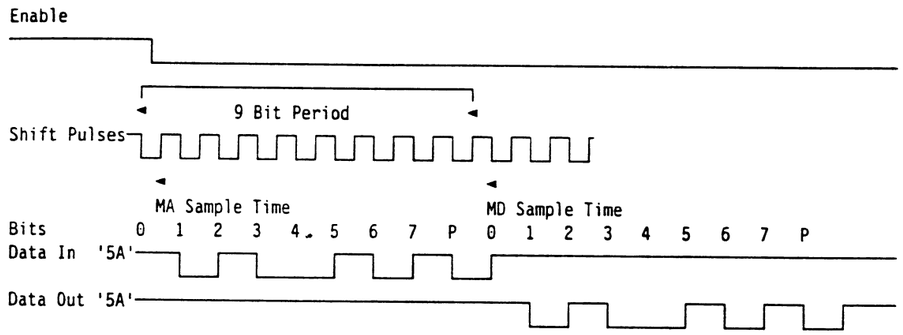


Figure 1. MD 'Open' Operation

2. **Put:** In this function both command and data bytes are sent across the 'serial data in' path using the 'read' and 'status in' lines for control. The MA command byte is sent first followed by the data bytes. The EOM command byte is sent to end the operation. Command bytes are indicated with the 'status in' signal line.

   The MD initiates the operation by activating the 'status in' line and the MA responds by activating 'read'. When the active 'read' signal line is detected by the MD, it starts sending 'shift' pulses that moves data or command bytes. There is a form of 'put' function with no data transfer that is used to send a command byte only for control type functions that have no data associated with them. See Figure 3.

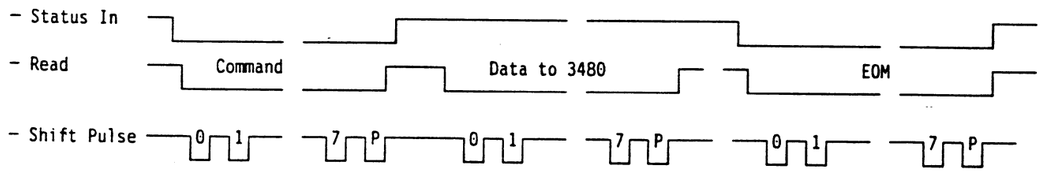


Figure 2. 'Put' Operation from MD to MA

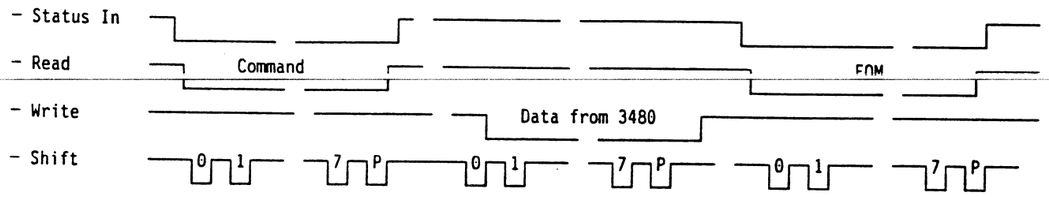


Figure 3. 'Get' Operation from the MA to MD

3. **Get:** In this function, the command bytes are sent to the MA by way of the 'serial data in' path, but the data bytes are controlled by the 'write' signal line and are received by the MD on the 'serial data out' path.

   You will notice that this operation is similar to the 'put' function except the 'write' line is used to move data and it is active before 'status in' and 'read' becomes active to send the EOM command at the end of the data transfer part of the operation. See Figure 4.

   Note: *See the Maintenance Device/Maintenance Adapter Diagnostic on DIAG 1. This diagnostic permits you to repetitively execute (loop) any of the above operations.*

   Enable Communication Path

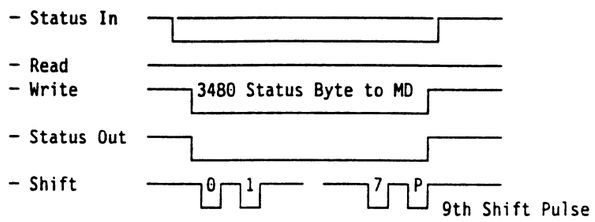
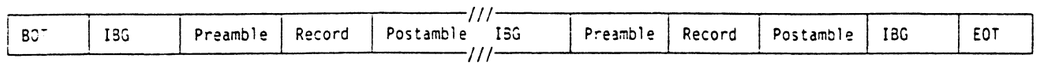


Figure 4. Status Out Sequence

Tape Record Format

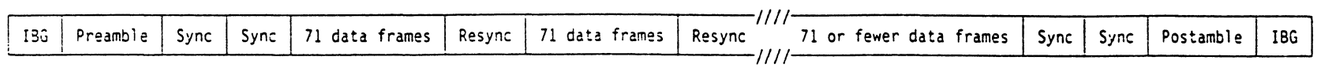
Tape Format

This diagram represents the general format of the tape.



Tape Data Record Format

This diagram represents the general format of data records on tape.



Tape Media Dimensions

The 3490 models capable of writing 3480-2 XF format support two tape lengths. Cartridge System Tape (CST) and Cartridge System Tape - 2 (CST-2). Other models of 3480/3490 support CST only.

Table 1. Tape Media Dimensions

Characteristic	CST	CST-2	Unit
Tape Width	12.65 (0.498)	12.57 (0.495)	mm (in)
Tape Length	165	332	m
Reel Circumference	280-307	310-314	mm

IBM Enhanced Capacity Cartridge System Tapes should not be mounted in a 3480 subsystem. Only the 3490E has the design updates needed to support the use of the enhanced capacity cartridge.

Tape that exceeds the length of IBM Cartridge System Tape could cause damage to either the tape or the drive, if processed to its Physical-End-Of-Tape. When an enhanced capacity cartridge is mounted in a 3480 Magnetic Tape Subsystem, the subsystem will return an ERA code to the operating system, indicating a tape length incompatibility. If this occurs, the job will not run and should be rerun with the cartridge mounted in a 3490E Magnetic Tape Subsystem. See MSG section for a discussion of ERA codes.

Tape Formats

There are three 3480/3490 tape formats and two tape lengths:

- 3480 Format

  This format is used when the data compaction and auto-blocking facility is not present, is disabled, or when the length of the compacted logical block exceeds the maximum buffered compacted block limit if an 18 track format is desired.

  3480 format is only supported on CST.

- 3480 XF Format

  This format is used when the data compaction and auto-blocking facility is enabled and the length of the compacted logical block does not exceed the maximum buffered compacted block limit if an 18 track format is desired.

  3480 XF format is only supported on CST.

- 3480-2 XF Format

  This format is the only 36 track format and is used whether data compaction is enabled or disabled.

  3480-2 XF format is supported on either CST or CST-2.

3480 models A11 and A22 control units, 3490 models D31 and D32 subsytems, and 3490 models A01 and A02 control units provide the following capabilities:

- 3480 Format Read/Write Capability.
- 3480 XF Format Read/Write Capability if the Data Compaction and Auto-Blocking Facility is installed.
- CST handling capability.

3490 model D41 and D42 subsytems, and 3490 models A10 and A20 control units provide the following capabilities:

- 3480-2 XF Format Read/Write Capability.
- 3480 and 3480 XF Format Read-Only Capability.
- CST and CST-2 handling capability.

This topic describes the major data flow paths within the subsystem that are used to transfer data during read and write operations and that control tape motion. In addition, data flow for the loop write to read diagnostic routine is also described.

Read Operation

The diagram on the OPER 95 page shows the read data flow path within the 3480 tape subsystem.

Buffered Read

A buffered read operation moves the data twice — first from the drive to the control unit data buffer, and then from the data buffer to the channel. The move from the drive to the buffer is performed at the drive data rate.

If multiple read commands have been sent to the same drive, the control unit might cause the drive to read the next data block in the file before the channel asks for it. Therefore, the requested data block might already be in the data buffer. If it is, the control unit sends it to the channel at channel speed as soon as the Read command is received, without requiring data transfer from the drive, including the drive start up time. Channel end and device end are sent as ending status and the operation is complete when all the requested data in the buffer has been sent to the channel, or the channel has stopped requesting data. If the data block is not in the buffer, the control unit responds with a channel command retry. The channel command retry causes the channel to disconnect from the subsystem and to become available for other host system work.

The control unit then selects and starts the addressed drive. As soon as the drive is up to speed, the control unit checks for read data from the drive. If a tape mark is found, the operation ends with unit exception, channel end, and device end. If no tape mark is found, the control unit checks the inter block gap, synchronization, and preamble characters for correct patterns and timing.

As the data block is read from the tape, it is loaded into the data buffer. At the same time, the control unit signals the channel by sending a device end. The channel responds to the device end by sending the original Read command. When the control unit receives the Read command, it starts sending the data block, one byte at a time, from the data buffer to the channel. The drive might still be sending data to the buffer at this time.

When all the data has been transferred by the control unit from the buffer, or the buffer and the drive, or the channel stops requesting data bytes from the buffer, the control unit sends device end and channel end to end the operation. The channel might not have requested all of the data bytes in the buffer. In this case, the remaining bytes are discarded. If any nonrecoverable errors occur during any part of the operation, unit check is sent with device end; the host system program requests sense data, and the control unit sends the drive sense bytes to the channel.

If the end-of-tape (EOT) is detected during the read operation, a unit check is sent with ending status.

If the BOT area is detected during a read backward operation, a unit check is sent with ending status.

Improved Data Recording Capability is not supported during a Read Backward operation.

0 0 0 0 0 0 0 0 0 0

Read Data Flow

This topic describes the major data flow paths within the subsystem that are used to transfer data during read and write operations and that control tape motion. In addition, data flow for the loop write to read diagnostic routine is also described.

Read Operation

The heavy lines in the diagram on the following page show the read data flow path within the 3480 tape subsystem.

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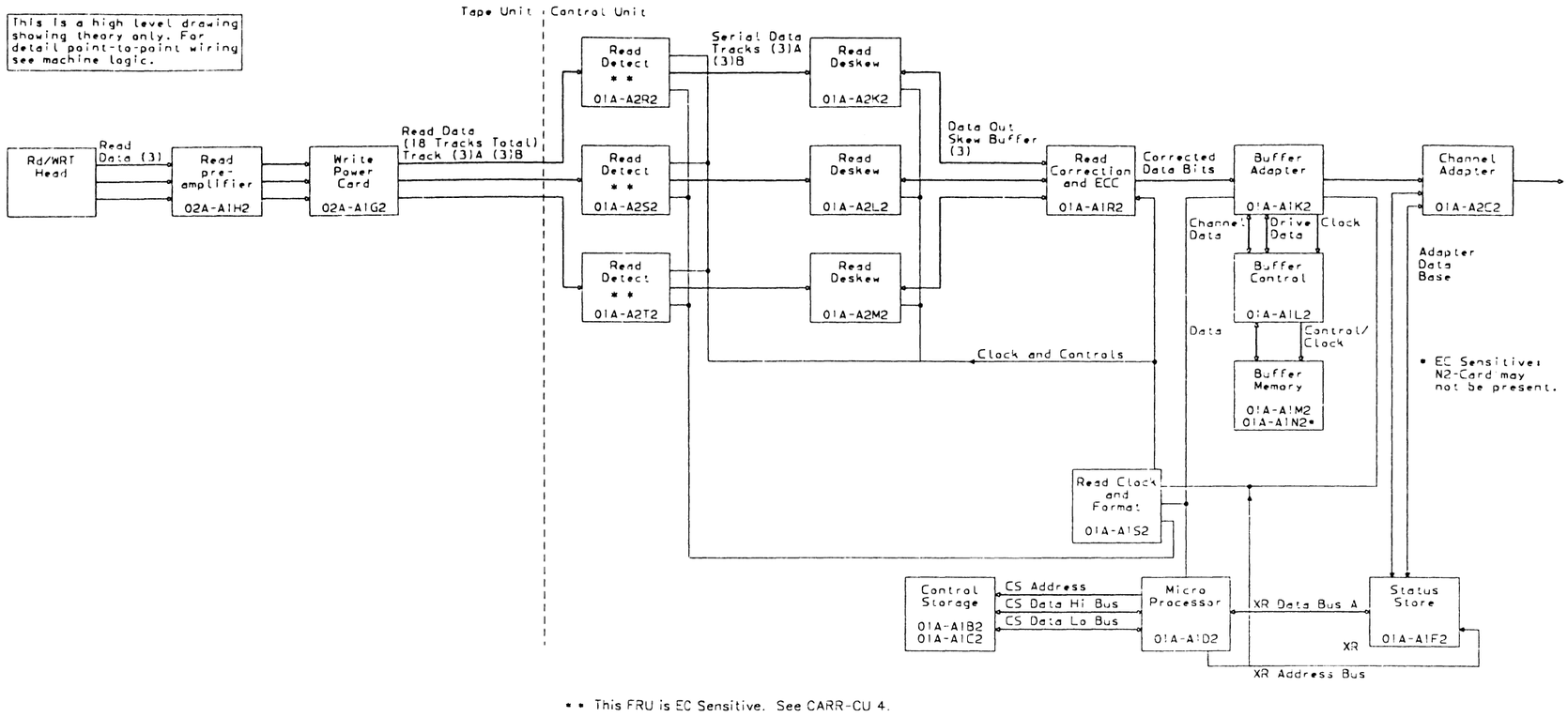
When all the data has been transferred by the control unit from the buffer, or the buffer and the drive, or the channel stops requesting data bytes from the buffer, the control unit sends device end and channel end to end the operation. The channel might not have requested all of the data bytes in the buffer. In this case, the remaining bytes are discarded. If any nonrecoverable errors occur during any part of the operation, unit check is sent with device end; the host system program requests sense data, and the control unit sends the drive sense bytes to the channel.

If the EOT is detected during the read operation, a unit check is sent with ending status.

If the BOT area is detected during a read backward operation, a unit check is sent with ending status.

Read Data Flow (Continued) **OPER 95**



• • This FRU is EC Sensitive. See CARR-CU 4.

Read Data Flow (Continued) OPER 95

Read Data Flow (Continued)

A Read command sent to the selected drive starts a read operation. When the drive is up to correct speed, and the interblock gap (IBG) preceding the record to be read has reached the read head, the drive signals the control unit by activating the 'gap in' line.

Read Operation

Use the following explanation with Figure 1.

'Gap in' sets the read status register (RSR) bit 3, causing a Level 3 Interrupt **1**. The microprocessor activates the 'read gate', (read control register (RCR) bit 0), and also checks that the read head is in the IBG (read pattern register bit 0 is set).

When the beginning of the record reaches the read head the beginning-of-block (BOB) sets read pattern register (RPR) bit 4 on, which causes a Level 2 Interrupt **2**.

The microprocessor activates the 'read condition'line (read control register (RCR) bit 2) which activates the read data flow, and sets the interval timer to check the preamble. When the sync byte reaches the read head 'begin sync' (RSR bit 0) is set, which causes a Level 3 Interrupt **3** and at the same time starts the read data flow transfer to the data buffer. The microprocessor checks that the beginning sync occurred within 100 microseconds (usec.) of the BOB. When the ending sync bytes pass the read head 'end sync' (RSR bit 1) is set, which causes a Level 3 Interrupt **4**. The microprocessor sets 'gap out enable' (RCR bit 6) and sets the interval timer to check the postamble.

The read data flow sends a 'read end' signal to the buffer adapter and 'device read end' (buffer device status and error register bit 1) is set. A Level 4 Interrupt **5** occurs and the microprocessor checks that no device buffer overrun occurred. When the last byte of the postamble has passed the read head, 'generate gap out' (RSR bit 2) is set. This causes a Level 3 Interrupt **6**. The microprocessor then checks that 'generate gap out' has occurred within 100 usec. of 'end sync', also verifies that the read head is in the IBG (RPR bit 0 is set) area, sends the 'gap out' signal to the drive, checks for any buffer or read data flow errors, checks the block ID for the correct sequence, and determines whether to continue or end the operation. If the operation continues, the buffer and read data flow controls are activated to send the next record. If the operation ends, the buffer and read data flow controls are reset and the drive is released.

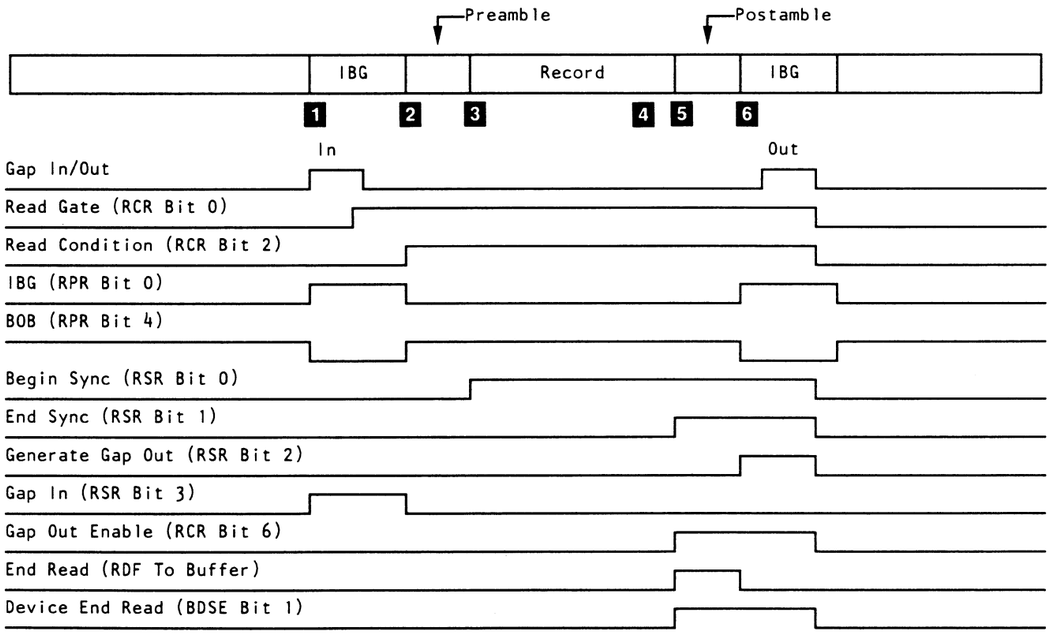


Figure 1. Read Operation Timing Chart

Write Operation

The heavy lines in the diagram on the following page show the data flow path within the subsystem for a write operation.

A write operation accepts data from the host system channel and records it on tape. The subsystem can accommodate two modes of writing:

- Buffered Write
- Tape Write Immediate

The Write command prepares the subsystem to record data on tape with the selected drive. The drive must be ready and the cartridge that is loaded must not be file-protected.

A Mode Set command before the Write command determines whether a buffered write or tape write immediate operation is to be performed. Synchronous write mode is selected automatically when the data block to be written is too large for the available buffer space.

Buffered Write Mode

The buffered write mode is the normal mode of operation. The control unit enters the starting address of the data block being written in a buffer record table. When the data is loaded into the buffer, an ending address is written in the buffer record table. The ending address enables the control unit to do the operation again if an error is detected during the write or the read-back check. The control unit receives the write data block, one byte at a time, from the channel and loads it in the data buffer. When the channel indicates that no more data is to be written, the control unit writes the ending buffer address in the buffer record table, and sends a channel end and device end to the channel. When the channel end and device end are received by the channel, the control unit is disconnected from the channel. The control unit channel adapter is then available to accept other commands, or additional data to the same drive to be written into the buffer.

Errors detected while the data is being transferred from the channel to the buffer cause a unit check to be sent along with the channel end and device end. The sense information is received, and contingent connection (CC) is set. The next channel command requests sense data.

If the next operation is another write to the same drive, the new data is placed in the data buffer at the next address following the first data block. The first data block does not need to be completely written on the tape for this to take place. Pad, CRC, and ID bytes are placed in their correct locations in the data block as it is stored in the buffer.

Records may continue to be placed into the buffer until it is full. Each data block in the buffer has its size and buffer location recorded in the buffer record table. When the requested drive becomes available, the data block can be sent from the buffer to the tape.

To send the data block from the buffer to the drive, the microprogram sends the data, one byte at a time, to the drive. When the drive signals that it is ready, the next data byte is sent. The drive processor sends the data bytes through the drive write circuits to the tape. The drive logic writes the preamble, postamble, IBG, and all pattern characters. If no errors occur, the next data block can be processed. If recoverable errors occur, the drive processor interrupts the control unit microprogram so that the error can be logged by the control unit in the buffered log. Nonrecoverable errors cause sense information to be stored by the control unit for future action.

As the data is written, a read-back check is performed to determine that writing is taking place, that the data can be read, and that the error correction code (ECC) checks without error. The read-back checks all data on the tape from the preamble to the next IBG. If no errors are detected, the microprogram generates gap out.

If errors occur while data is being written on tape, the control unit performs error recovery procedures (ERPs). If the ERPs do not correct the problem, the control unit sends unit check to the host channel during the next channel command word sent to that drive. The host system program then performs its own error recovery procedures or stops operations to that drive and sends an error message to the operator.

Tape Write Immediate Mode

The tape write immediate mode differs from buffered write mode in that it does not make the drive available to the channel at the end of the transfer of data to the buffer. When the channel completes the transfer of data to the buffer, the control unit responds only with channel end status. The control unit does not send device end status to the channel until the data has been written on the tape and the drive has moved the tape to the stoplock position.

Each time a command execution is completed, the drive stops and moves to the stoplock position. This affects subsystem performance, because during the repositioning time, the drive is not available for use.

Write Operation

The heavy lines in the diagram on the following page show the data flow path within the subsystem for a write operation.

A write operation accepts data from the host system channel and records it on tape. The subsystem can accommodate two modes of writing:

- Buffered Write
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A Mode Set command before the Write command determines whether a buffered write or tape write immediate operation is to be performed. Synchronous write mode is selected automatically when the data block to be written is too large for the available buffer space. The Improved Data Recording Capability function is not supported during Synchronous Write Mode.

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Each time a command execution is completed, the drive stops and moves to the stoplock position. This affects subsystem performance, because during the repositioning time, the drive is not available for use.

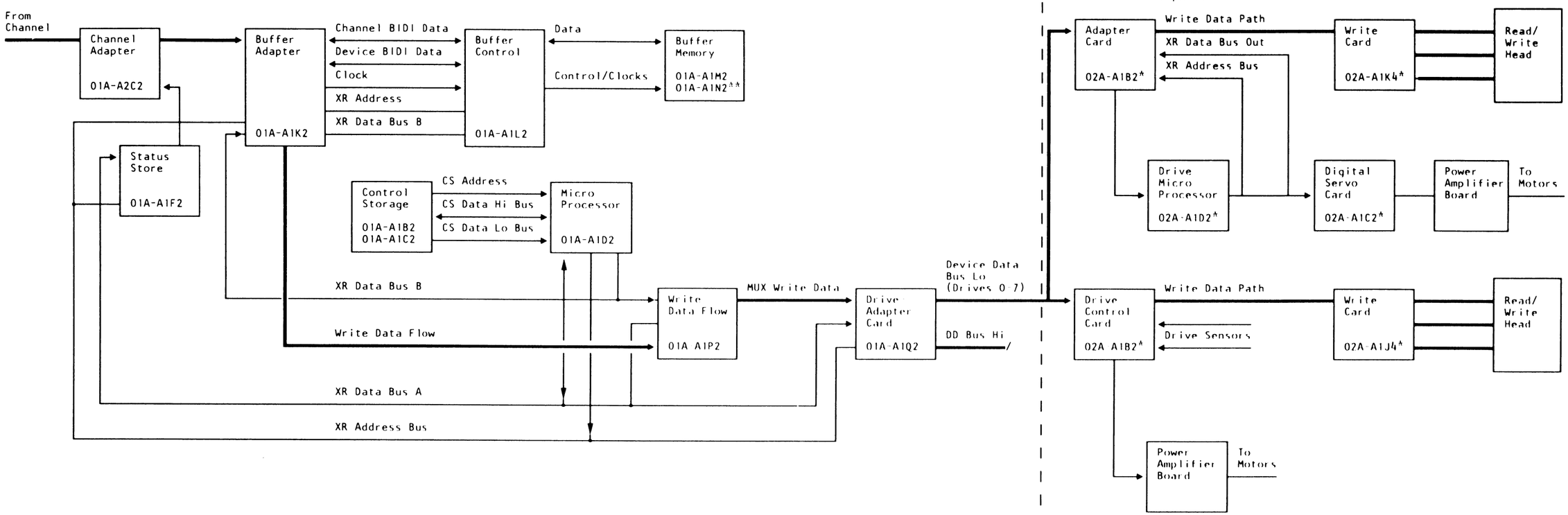
0 0 0 0 0 0 0 0 0 0

Write Data Flow (Continued)

This is a high level drawing showing theory only. For detail point-to-point wiring see machine logic.

* This FRU is EC sensitive. See CARR-DR 4.

** This FRU is EC sensitvie and may not be present.



Write Data Flow (Continued)

The microprocessor sends a Write command to the drive, and when the drive is up to the correct speed and the interblock gap (IBG) is at the write head, the drive generates a 'gap in' line to the control unit.

Write Operation

'Gap in' sets the write status Error (WSE bit 0) register (write op) and also sets the read status register bit 3 (gap in) which causes a Level 3 Interrupt 1. The microprocessor sets up the data flow controls in the write control register (WCR) and sets the timer for read back checking.

The write data flow (WDF) completes a write of the preceding IBG, and then writes the preamble and the beginning sync bytes. The WDF encodes the binary data from the buffer and writes the data portion of the record.

When all the data bytes have been sent from the buffer to the WDF, the buffer adapter sends a WDF 'end' signal to the WDF, and sets Device Transfer Complete. The WDF 'end' signals the WDF to write the ending sync bytes, postamble, and activates the WSE register bit 1. The WDF writes the greater part of the next IBG snf deactivates the WSE bit 0, Device Transfer Complete, causing a Level 4 Interrupt 2. A check is made for any buffer and WDF errors and it is then determined whether to continue or end the operation.

Read Back Checking

When timeout (set in the write sequence) occurs, a Level 1 Interrupt 3 occurs. The microprocessor activates Read Control Register (RCR) bit 0 and checks to ensure that the read head is in the preceding record, tape mark, or the end of record gap (ERG).

When the last byte of the postamble, tape mark, or the ERG goes past the read head, read status register (RSR bit 2) ('generate gap out') is set and a Level 3 Interrupt 4 occurs. The microprocessor checks that the IBG is active and that the timer is set to check for short IBGs. When the timer has timed out a Level 1 Interrupt 5 occurs. The microprocessor checks to ensure that the IBG is active, and then resets the RSR.

When the first byte of the preamble has been read by the read head, the beginning-of-bob (BOB) read pattern register (RPR bit 4) is set and a Level 2 Interrupt 6 occurs. The microprocessor activates a read condition to enable the read data flow for read back checking. The timer is set for the checking of the preamble.

When the beginning sync bytes are read at the read head, RSR bit 0 is set and a Level 3 Interrupt 7 occurs. The microprocessor then checks that the beginning sync occurred within 100 microseconds of the BOB. When the ending sync is read at the read head, RSR bit 1 is set which causes a Level 3 Interrupt 8 occurs.

The microprocessor sets the timer for a postamble check and when the last byte of the postamble has been read at the read head, RSR bit 2 ('generate gap out') is set which causes a Level 3 Interrupt 9. The microprocessor then checks that 'generate gap out' occurred within 100 microseconds of the ending sync. The microprocessor then verifies that the read head is in an IBG, and also checks for any errors. If these two conditions have been met, the control unit sends 'gap out' to the drive and resets the buffer and the data flow controls. The microprocessor then releases the drive.

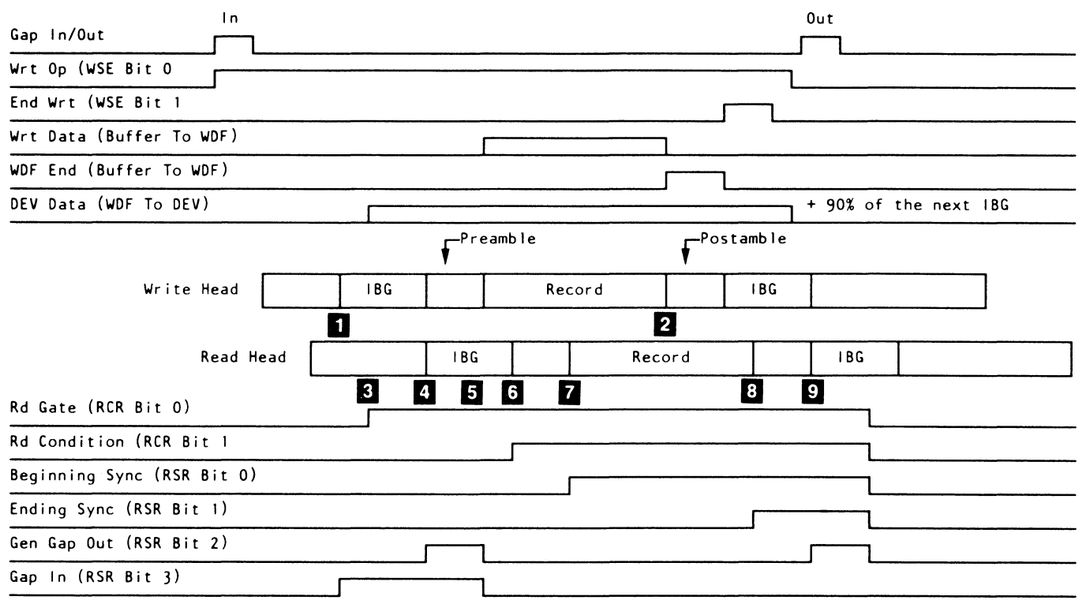


Figure 1. Write Operation Timing Chart

Loop Write to Read Data Flow

This topic describes the long and short loop write to read modules in the loop write to read diagnostic routine. Loop write to read diagnostic modules are used to check out the write and read data paths within the subsystem and to isolate problems to either the control unit or to a tape unit.

The diagram on the preceding page shows the data paths within the subsystem for the long and short loop write to read diagnostic modules. The long dashed lines show the long loop write to read data path and the short dashed lines show the short loop write to read data path. The heavy solid lines show the common data path used by both modules.

Short Loop Write to Read

The short loop write to read diagnostic module checks the write to read data path within the control unit. A data pattern, received from the maintenance device by the buffer control card, is transmitted along a data path that includes the buffer adapter card, write data flow card, read detect and read deskew cards, and finally to the read correction and ECC card where the control unit microprocessor checks for any hardware detected errors.

Long Loop Write to Read

The long loop write to read diagnostic module checks the write to read data path from the control unit to a tape unit and back to the control unit. A data pattern, received from the maintenance device by the buffer control card, is transmitted along a data path that includes the buffer adapter card, write data flow card, drive control card, the write bus, and the drive-adapter card.

The drive-adapter card transfers data over 'write bus' lines 0 and 1 to the read preamp card. At the read preamp card, the data from 'write bus' line 0 is gated to the read inputs for tracks 1A,2B,3B,4A,5B,6B,7B,8B and 9B. The data from 'write bus' line 1 is gated to the read inputs for inputs for tracks 1B,2A,3A,4B,5A,6A,7B,8A and 9A.

From the read preamp card, data is returned to the control unit over a read path that includes, the read bus, write power card, read detect and read deskew cards, and finally to the read correction and ECC card where the control unit microprocessor checks for any hardware detected errors. The write card and write head are not part of this path and are not tested in a long loop write to read operation.

A Set Diagnose command is sent to the device to condition it for a long loop write to read. Upon receipt of this command, the device checks for cartridge present. If a cartridge present is indicated, a unit check status is set, an error code is posted in sense and displayed at the device, and the loop write to read is aborted.

Loop Write to Read Data Flow (Continued) **OPER 115**

This is a high level drawing showing theory only. For detail point-to-point wiring, see machine logic.

*This FRU is EC sensitive. See CARR-DR 4.

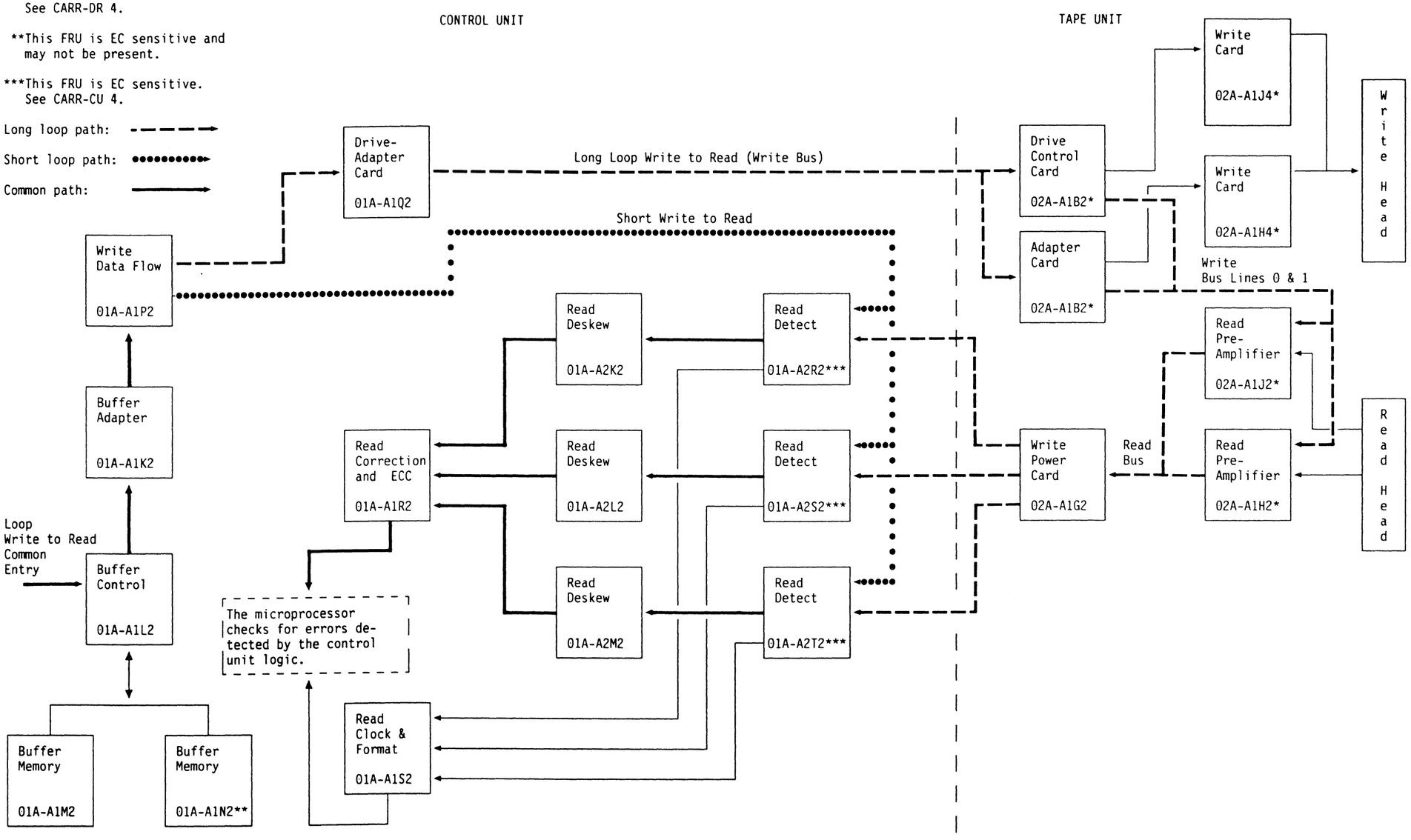
**This FRU is EC sensitive and may not be present.

***This FRU is EC sensitive. See CARR-CU 4.

Long loop path:

Short loop path:

Common path:



Loop Write to Read Data Flow (Continued) OPER 115

Drive Data Flow

* This FRU is EC sensitive.
  See CARR-DR 4.

This topic describes the read and write data flow within the tape unit.

Read

The differential signal output from each read track is directly connected to the read preamp by way of the read head cable. The read preamp amplifies these signals, and sends them to the selected read bus cable (either A or B) and to the read detect cards in the control unit. The read bus is determined by the control unit that requested the data: bus A is for control unit 0, and bus B is for control unit 1. The write power card is used as a signal feed-through from the logic board to the A and B read bus connectors.

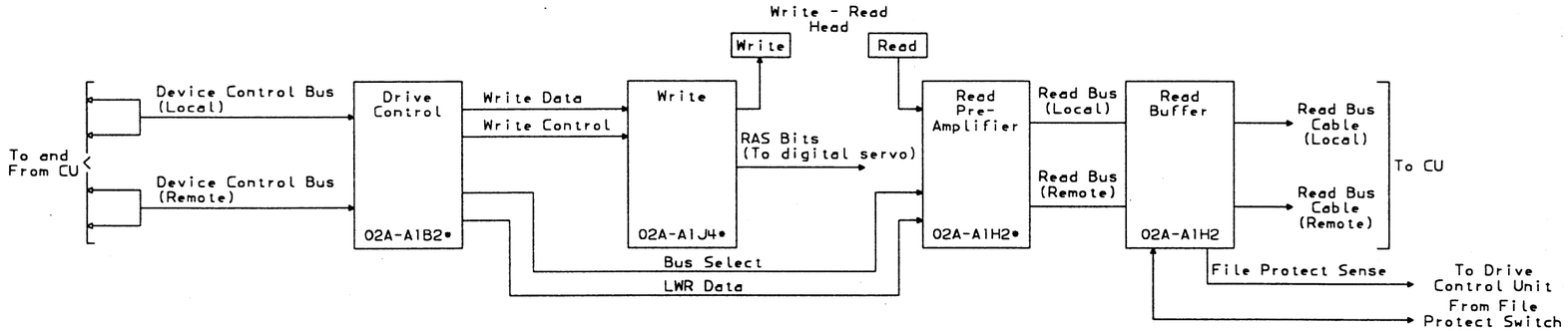
Write

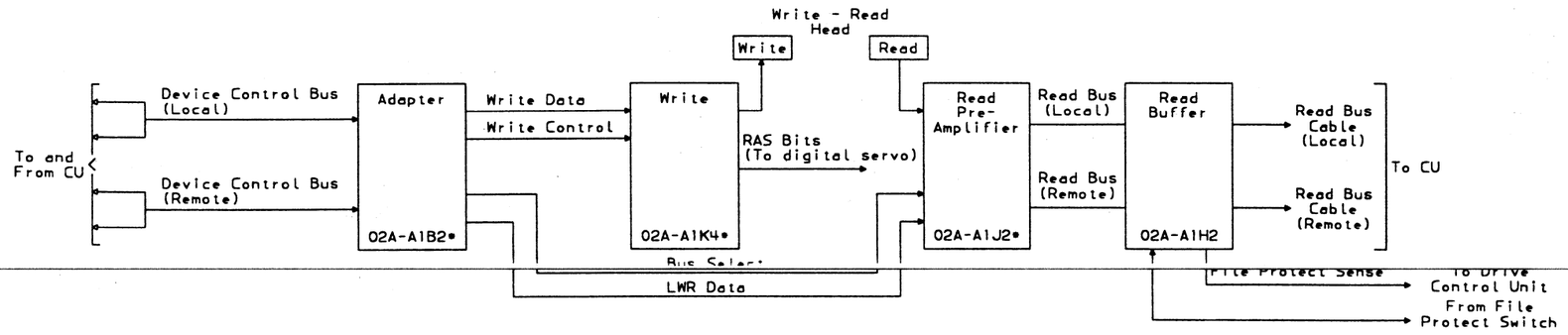
Write data is sent from a control unit to the selected drive by way of a serial connected device control bus. Either the A or B bus is used. The bus used depends on the control unit that selects the device: bus A is for control unit 0, and bus B is for control unit 1. For single control unit subsystem, bus 'A' is always used. The adapter card receives the non-return-to-zero (NRZI) data, and sends it to the correct analog read bus on the read preamp card.

The write card converts the NRZI data to a chain of current pulses that are sent directly to the write tracks by way of the write head cable.

Read/Write Operations Diagram

This is a high level drawing showing theory only. For detail point-to-point wiring see the machine logic.





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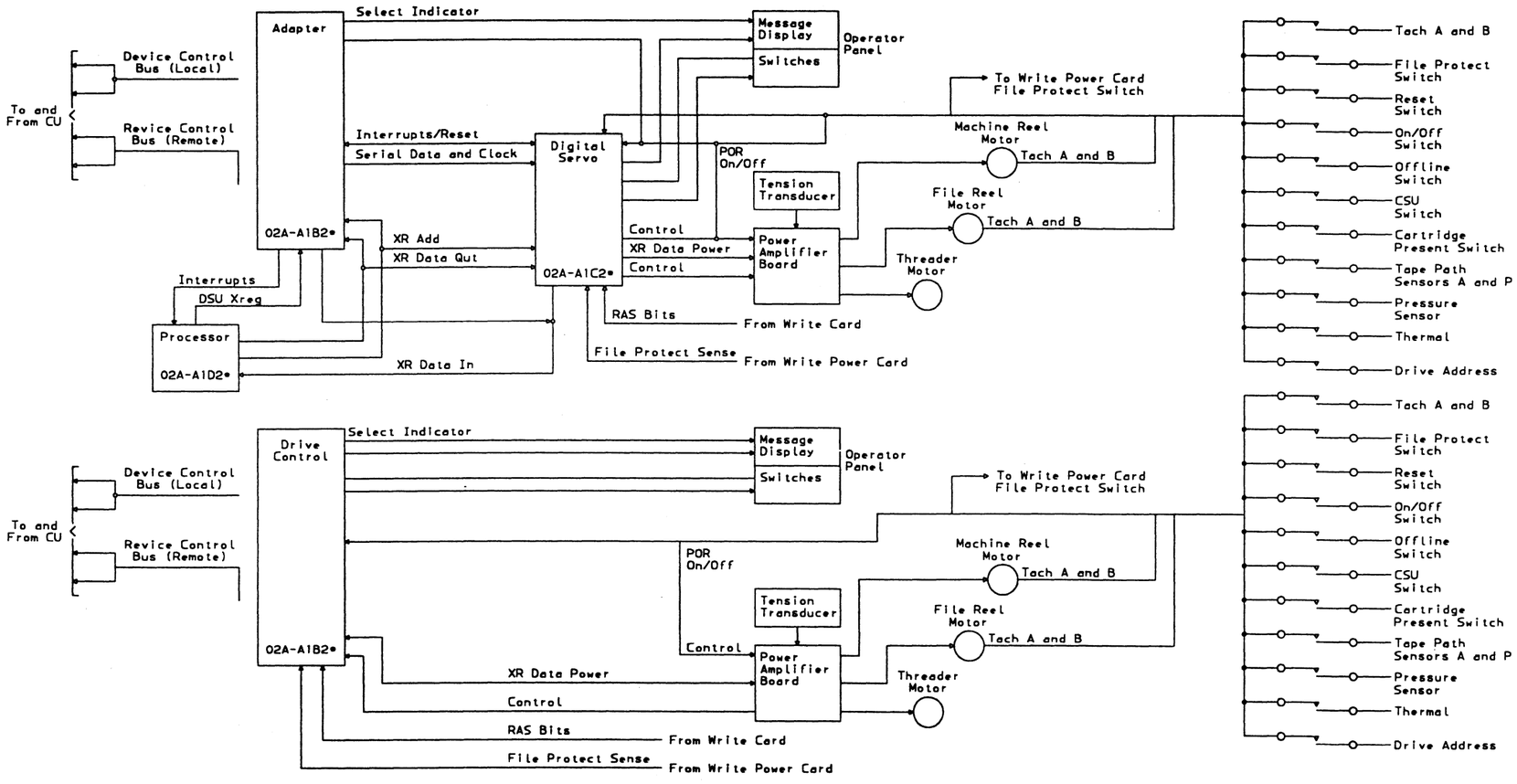
Drive Data Flow (Continued)

Motion Control Diagram

This is a high level drawing showing theory only. For detail point-to-point wiring see the machine logic.

•This FRU is EC sensitive. See CARR-DR 4.



Drive Data Flow (Continued)

Drive Data Flow (Continued)

This topic describes operations within the drive that control tape motion. Parallel and serial interconnections are also described.

Motion Control

The drive motion control logic is used for:

- Tape tension control
- Velocity control
- Backhitch (reposition) control
- Stoplock (position) control

The **tension control** function provides constant tape tension, essential for motion control.

The **velocity control** provides controlled acceleration up to recording speed or rewind speed, precise control of recording speed regardless of tape distribution on the reels, and controlled deceleration.

Following read or write operations, the tape is repositioned so that the read/write head is located just before the inter block gap that was just written or read. Repositioning is handled automatically by the motion control logic and is termed **backhitch**. The drive control logic causes the IBG to be written or read by the head while the tape is moving at normal recording velocity. Once the IBG has been written or read from the tape following a block, the head is deactivated, and the drive decelerates. By the time the tape has stopped, the head is past the IBG. The drive then backs up the tape immediately in front of the interblock gap that was just written or read, so that when the drive begins to accelerate for the next read or write operation it will be moving the tape at full speed when the IBG is encountered.

The **Stoplock** (position-hold) mode is used when the tape is in a stopped position and under tension. When in Stoplock mode, the tape lifter solenoid is energized to prevent the tape from sticking to the head.

The drive can independently reposition the tape from one location to the preceding Stoplock location, under direction from the control unit. Thus, the drive can independently revert to the preceding data block position for fast error recovery. Once loaded, the drive maintains one of three Stoplock positions, in anticipation of the next command.

- Read Forward Stoplock, ready for a read forward
- Read Backward Stoplock, ready for a read backward
- Write Stoplock, ready for a write.

Stoplock positions are achieved automatically by the drive, and are based on the command just executed. At the end of a particular command where no similar command is immediately following, the drive always assumes that some time in the future the next command to be executed will be the same as the last one. The drive repositions the tape to the Stoplock position that accommodates the next (similar) command. The exception to this is a Backspace Block command. After a Backspace Block command, the drive assumes a Read Forward Stoplock in anticipation of a subsequent Read command.

Message Display

The digital servo also communicates with the message display by way of the 'XR repowered data' bus that also connects to the power amplifier, additional display control signals, and switch signals from the operator panel.

Motor Control

The digital servo card functions as a buffer and the bus between the microprocessor and the other areas of the device. Like the adapter card, the processor communicates with the digital servo external registers using the XR data and address buses. The digital servo sends the data and control signals to the power amplifier board. The power amplifier converts this digital information to motor current. The digital servo then collects information in its external registers from the motor tachometers and tape sensors. This information is used by the processor to control the speed of the drive motors.

Parallel/Serial Interconnector

Commands are sent to the device on the Device Control Bus (DCB). For a dual control unit subsystem, cables DCB local and remote are used. For a single control unit subsystem, only the DCB local cable should be connected. The adapter card has two separate parallel paths (local/remote) and a single serial path. (The serial buses are connected together on the adapter card.)

Parallel Interconnector

Commands received on one of the parallel interconnection are controlled by the device microprogram once the 'command out' tag becomes active. (Adapter hardware logic processes the device selection.) The command is controlled by the processor, which communicates with the adapter using the external registers on the adapter and the XR data and address buses.

Serial Interconnector

The serial interconnection permits limited communication to the device while the parallel interconnection is busy or has failed. Only non-data transmission commands are sent over the serial interconnection.

The adapter card synchronizes and gates the serial clock and data to the digital servo card, where it is decoded. The data path runs from the DCB cable, through the adapter, to the digital servo. Once decoded, the motion commands are controlled by device microprogram just as if they had come on the parallel interconnection; hardware-only commands are executed independent of microprogram.

Subsystem Configurations

The 3480 tape subsystem can be configured as either a single or dual control unit subsystem. In a single control unit subsystem, the control unit sends data to and receives data from its attached drives. In a dual (two) control unit configuration, either control unit can transfer data to or receive data from its own drives or the drives attached to the other control unit. This topic describes the operation of both configurations.

Single Control Unit Configuration

A single control unit configuration consists of one control unit with up to eight attached drives. The control unit receives commands and data from the host system and transfers data and subsystem status by way of the channel and its channel adapter.

The diagram at right shows the data paths between the host channel, control unit and drives.

SS Status Store

Loc Local

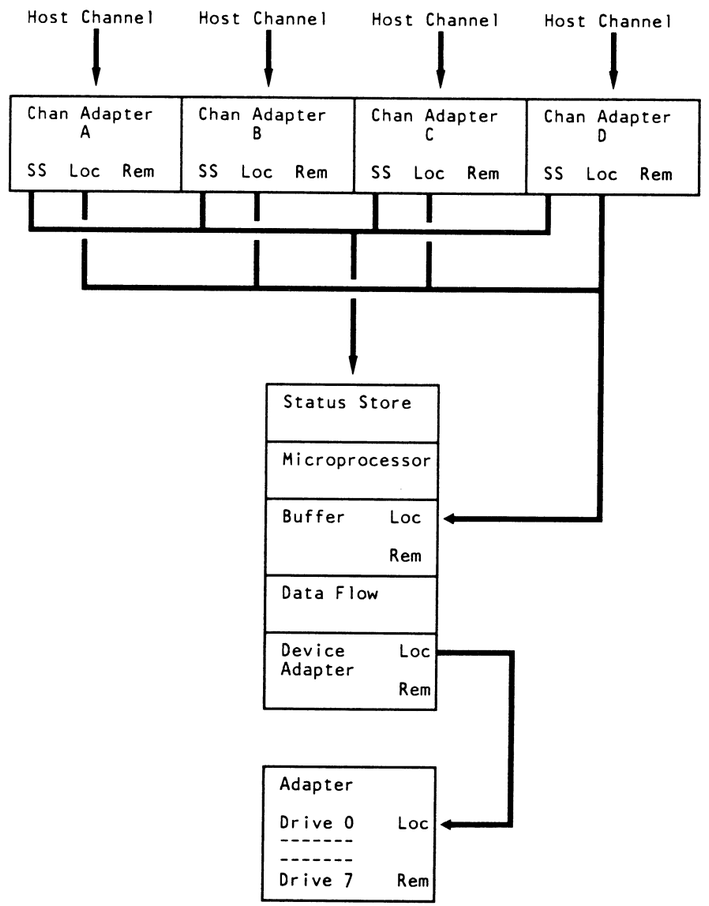
Rem Remote

Single Control Unit Command Sequence

An example of a typical single control unit command sequence is:

1. The host issues a channel command to the subsystem.
2. The channel adapter waits to be polled by status store.
3. The channel adapter requests a device assignment and the device status byte from status store.
4. Status store tests the device assignment byte, and if not assigned elsewhere, sets the channel adapter bit and responds with the device status bit.
5. The channel adapter uses the device status bit to generate initial status.
6. The channel adapter passes the initial status to the host.
7. The channel adapter stores the command, device condition byte, and interrupt request code, sets control unit busy, and activates a level 6 interrupt.
8. When the interrupt is detected by the microprogram, it examines the Channel Response Register (CRR) in status store to identify the reason for the interrupt and to find out which channel adapter bit is set.
9. The microprogram interrogates the channel RAM to find the reasons for the interrupt and the command byte.
10. The microprogram resets the interrupt to free the channel adapter, which in turn, resets 'control unit busy' in the channel adapter and permits the processing of a new command.
11. The microprogram initiates the command, sets up the buffer, starts the selected drive, and controls the data flow to or from the drive.
12. When the operation is complete, the microprogram stores an ending status byte in the channel adapter RAM and directs the adapter to present the status to the host system.
13. If command chaining is not indicated, the channel adapter interrupts the microprogram after the ending status has been transferred and requests that the device be freed in status store.

Single Control Unit Configuration Diagram



Dual Control Unit Configuration

The dual control unit configuration interconnects two control units. This dual control unit configuration permits operations in the subsystem to be balanced between the control units for most efficient use of subsystem resources. This mode of subsystem operation is transparent to the host system, because subsystem operations are automatically handled by the subsystem hardware and microprogram.

> **Note:** If when using a dual control unit subsystem one of the control units is not able to detects a response from the other control units, it indicates this in the other control unit by setting PER register bit 2 (collision detect), in that control unit. See PER bit 2 in the MI DF section.

In a dual control unit configuration the following four communication paths are used:

- Status store to status store **1**.
- Channel adapter to status store **2**.
- Channel adapter to local buffer **3**.
- Channel adapter to remote buffer **4**.

Figure 1 on the following page shows the data paths between the host channel, control unit, and drives.

SS Status Store
Loc Local
Rem Remote

Load Balancing in a Dual Control Unit Subsystem

At varying times each drive attached to the subsystem is assigned to one of the two control units. All commands to a drive are executed by the assigned control unit and all buffered data to the drive is stored in that assigned control unit.

Both control units monitor their workloads and periodically **balance** their work by reassigning drives from the more active control unit to the less active control unit. Reassignment may occur at any time during the host processing of a drives tape.

The pattern of channel attachment usage of each drive is also monitored. If the channel attachment in one control unit receives most of the host commands for some drives, the load balancing algorithms of the subsystem attempts to use the buffer in that control unit for those drives.

When a drive is assigned to a control unit for use by the service representative, (a drive is assigned to the control unit by plugging in the MD) reassignment of the drive is not permitted until the service representative releases the drive or unplugs the MD from the control unit.

Status Store to Status Store Interconnection

The status store to status store **1** communication path is used to give the two control units the ability to synchronize their individual operations and to provide a communications path between the two microprocessors using a 'master/slave' mode of operation. When either control unit is in the 'slave' status, status store does not execute orders.

Part of the status store communication path between control units is the 'RAM' address bus, RAM data bus, and 'memory write' signal. When a memory write operation is performed the RAM address bus contains the address of the status store RAM; the RAM data bus contains the data being written to the RAM, and the memory write signal is used to gate the data into the RAM. When either control unit is written into, the 'RAM' in the other control unit is also written into with the same data.

The remainder of the status store to status store communication path control signals are:

- Local Control Unit Master ÷ indicates this control unit is the current master control unit.
- Remote Control Unit Master ÷ indicates that the other control unit is the current master.
- Local Control Unit Connected ÷ the local control unit is enabled for a dual control unit mode of operation.
- Remote Control Unit Connected ÷ the remote control unit is enabled for a dual control unit mode of operation.

  > **Note:** Local and remote control unit connected lines become inactive when the corresponding control unit is offline.

- Local Control Unit Send ÷ indicates that the microcode has assembled a message in the message buffer.

  > **Note:** This signal is named 'received' at the receiving control unit.

- Local Control Unit Acknowledge ÷ this line is used to acknowledge the receiving of a message. This causes a reset of the 'send' signal at the other control unit.

Channel Adapter to Status Store Interconnection

The channel adapter to status store **2** interconnection supplies the communication path for data and status information between the channel adapters and status store.

The status store communicates with the channel adapters by polling each adapter in turn; channel adapter A, channel adapter B, and so on.

The communication path contains the following lines:

- A nine bit bi-directional data bus used to transfer orders and data between the status store and the channel adapter.
- A five bit bi-directional response used to transfer an address or response data to the channel adapter, or response data to the status store.
- Two system clocks (C1 and C2).
- Two condition bits that define the current PLA condition.
- An adapter select line to each adapter.
- An adapter reset line to each adapter.
- An adapter interrupt line from each adapter to the status store.
- An adapter failure line from each adapter to the status store.

Channel Adapter to Buffer (Local/Remote) Interconnection

All channel adapters in a control unit share the same local **3** and remote **4** buses to the buffer. Only one is permitted use of the bus at any one time.

The interconnection contains the following lines:

- Service Out (Remote/Local) – this is the channel service out tag.
- Data Out (Remote/Local) – this is the channel data out tag.
- Service In (Remote/Local) – this is the control unit service in tag.
- Data In (Remote/Local) – this is the control unit data in tag.
- Stop (Remote/Local) – this is the channel adapter signal used to inform the buffer that the data transfer has ended.
- Data Valid (Remote/Local) – this line is used as a gate for data that is sent to the channel for parity checking.
- Buffer Data Bus (Remote/Local) – this a 9-bit bi-directional data bus used to send and receive data from the buffer.
- Suppress Out (Remote/Local) – this is the channel suppress out tag.

Subsystem Configurations (Continued) OPER 140

Dual Control Unit Command Sequence

An example of a typical dual control unit command sequence is:

1. The host system issues a channel command to the subsystem.
2. The channel adapter waits to be polled by status store.
3. The channel adapter requests a device assignment and the device status byte from status store.
4. Status store requests Master status before it can begin order execution.
5. When Master status is granted, status store tests the device assignment, and if not assigned elsewhere, sets the channel adapter bit and responds with the device status byte from status store RAM.
6. The channel adapter uses the device status byte to generate initial status and transfers this to the host system.
7. The channel adapter stores the command, device condition byte, and interrupt request code in the channel adapter RAM, sets 'control unit busy', and through the channel adapter activates a request interrupt to the status store. Status store activates an interrupt level 6 to the microprogram.
8. When the interrupt is detected by the microprogram, it examines the Channel Response Register (CRR) in status store to identify the reason for the interrupt and to find which channel adapter bits are set.
9. The microprogram reads the channel adapter RAM to find the interrupt reason and the command byte.
10. The microprogram resets the interrupt to free the channel adapter. The channel adapter resets the 'control unit busy' condition.
11. The microprogram determines which control unit the drive is assigned to.

    Local: Perform the command action as required - set up the buffer, start the drive.

    Remote: Send the command to the other control unit via status store. Wait for the remote control unit to finish the command. The remote control unit sends the ending status in a message when the command is complete.
12. When the command has completed, the microprogram stores the ending status byte in the channel adapter RAM and directs the adapter to present the status to the host system.
13. If command chaining is not indicated, the channel adapter requests that the device be freed by passing a status store order on a polling operation.

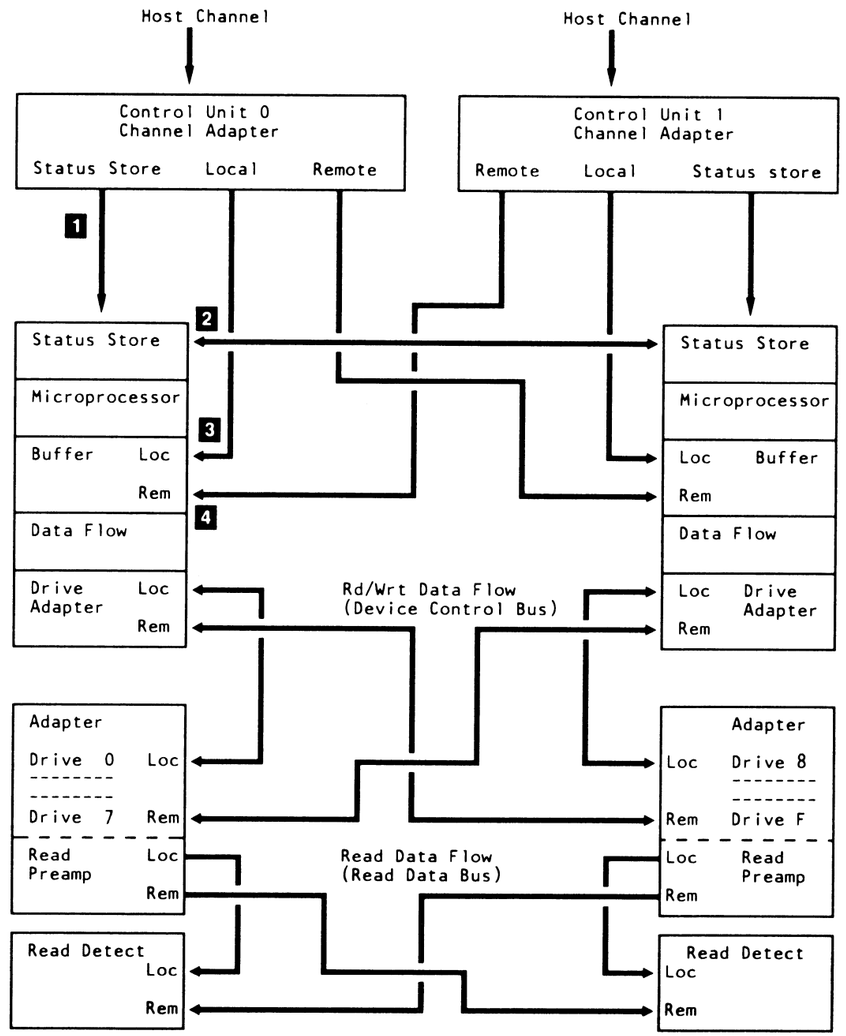


Figure 1. Dual Control Unit Configuration

Dual Control Updating Status Store 'RAM'

At installation time the customer assigns the control units as 0 and 1. During a normal dual control operation, control unit 0 assumes control of the 'master/slave' logic.

At every status store condition 3 cycle, control unit 0 deactivates the 'local master' line for one cycle to permit control unit 1 to reach the master condition if it needs to.

The importance of being in the master condition is that the status store in each control unit can not execute any orders while in the 'slave' condition. If control unit 1 is in the 'slave' condition, a request for 'master' condition is generated by activating its 'local master' line.

Part of the status store communication path between control units is the RAM address bus, RAM data bus, and a memory write signal line. When a memory write operation is performed, the RAM address bus contains the address of the status store RAM; the RAM data bus contains the data being written to the RAM, and the memory write signal is used to gate the data into the RAM. When either control unit is written into, the RAM in the other control unit is written into with the same data.

The timing chart shows an example of a message being written into address 80 and 83, and the updating of the RAM status.

Note: This is to remind you that each control units status store lines going to the other control unit are labeled local, and are labeled remote coming from the other control unit. The timing chart is shown at the control unit 0 side. See OPER 1, Subsystem Configurations, "Status Store to Status Store Communication Path Diagram."

Writing a Message into Address 80 and 83

Control unit 1 requests an initial microcode load (IML) from control unit 0 by writing a message into address 80 and 83. The first part of the timing chart shows that control unit 1 must activate its 'local master' 1 line, assemble the data and address to be written, then activates its 'memory write' 2 line to gate the information into address 80 3 and 83 4 of both RAMs.

When both addresses have been written into, control unit 1 activates its 'send' 5 line to indicate to control unit 0 that a message has been written. No other action takes place until control unit 0 acknowledges the 'remote send' line.

Note: The 'send' line is only active when a message has been sent to the RAMs. Updating the device status byte needs no 'send' line.

Updating the RAM Status Byte

The second half of the timing chart shows control unit 1 updating the device status byte in address 1B of the RAMs. Control unit 1 activates its 'local master' 6 line, assembles the data and the address to be written into, then activates its 'memory write' 7 line to gate the information into address 1B 8. Because this is not a message, control unit 1 does not activate its 'send' line.

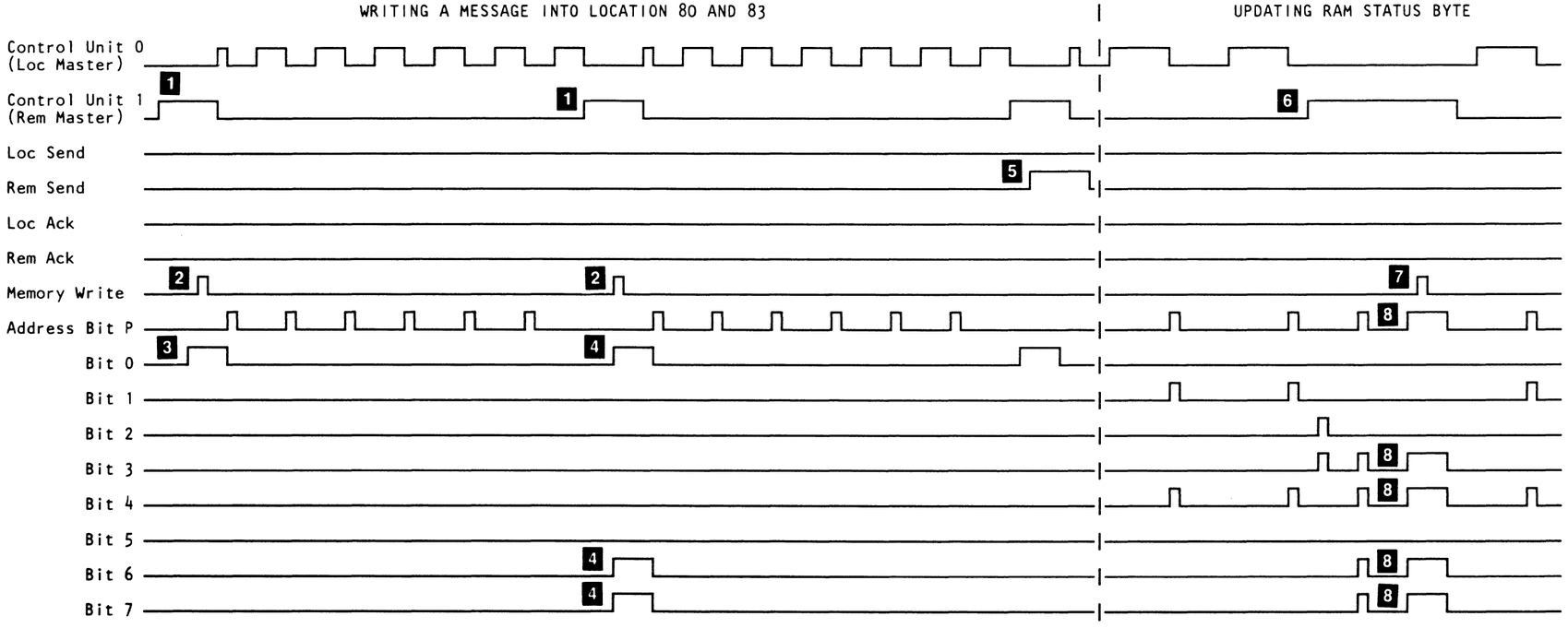


Figure 1. Status Store Communication Path Timing Chart

Subsystem Configurations (Continued) OPER 142

Subsystem Configurations (Continued)

Control Unit to Control Unit Communication

The control units, in a dual control unit configured subsystem, communicate over the Status Store to Status Store Interconnection. The status store communication card provides the logic for this communication.

In order for the microprograms in the two control units to communicate, status store provides orders, which are used by the microprogram. In addition to the orders, a portion of status store RAM is set aside as message buffers. Two message buffers are defined, one for sending and one for receiving messages. Two buffers also permit the control unit to send and receive messages at the same time.

The diagram at right shows the lines that are used to transfer data and information between the control units.

Send Message Operation

To send a message to the other control unit, the following sequence of operations is followed:

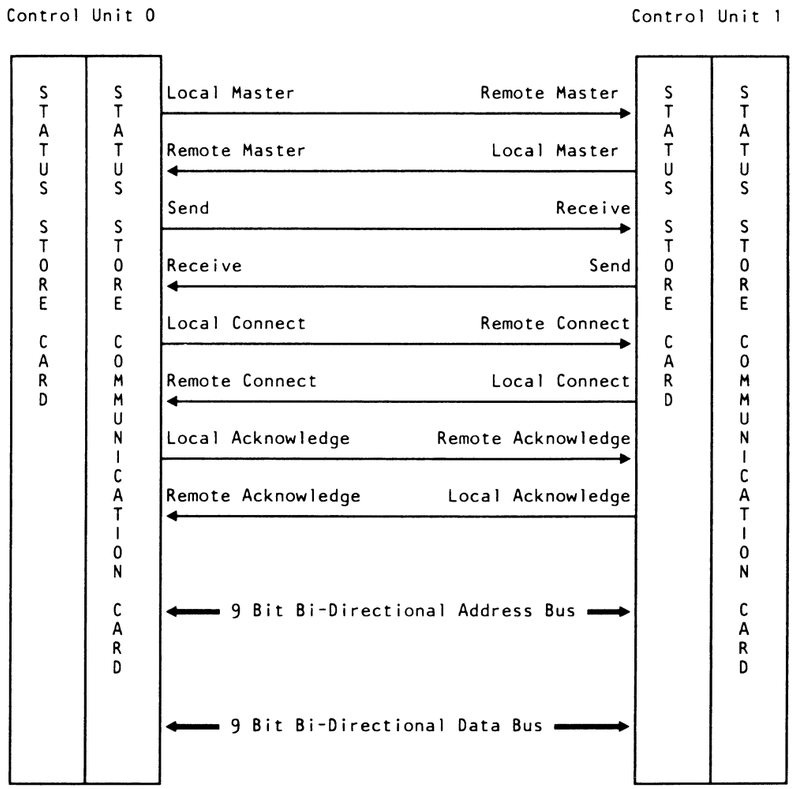
1. Test if the Acknowledge bit is on. If it is not on, the other control unit has not responded to the last message sent. A message can not be sent until the Acknowledge response is received.
2. Issue a Reset Write Message Pointer order to status store to initialize the buffer pointer.
3. Set a byte of data into the Channel Data Register (CDR).
4. Issue an Access Write Message Buffer order to store the data from the CDR into the message buffer (and into the read message buffer of the remote control unit).
5. Repeat the last two steps until all the data bytes have been sent.
6. Issue a Send order. This causes a received indication at the remote control unit.

Receive Message Operation

To receive a message from the other control unit, the following sequence of operations is followed:

1. Issue a Reset Read Message Pointer order to initialize the read buffer pointer.
2. Issue an Access Read Message Buffer order to set the data byte into the Channel Data Register (CDR).
3. Read the CDR to obtain the data byte.
4. Repeat the previous two steps until the entire message is read.
5. Issue an Acknowledge order to inform the other control unit that the message was received.

Status Store to Status Store Interconnection Diagram



Channel Commands

The 3480 executes the channel commands listed in the Channel Command Summary table on OPER 155 and described on OPER 160 through OPER 180. The Channel Summary Table provides a brief description of each command. Detailed command descriptions are found on the pages following the table.

Commands that are not usually ended immediately (channel end status sent at initial status time) can be received by the control unit when the drive is not executing an I/O operation for another channel path. If there is a delay between receiving and completing a command, the channel is disconnected by a channel command retry. While the channel is disconnected from the control unit, the subsystem can process some or all of the command. This aids in keeping the channel open much of the time.

In addition to the channel commands the 3480 uses the System/370 input/output (I/O) instructions.

For additional information concerning channel commands, see the following:

- *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers Information*, GA22-6974.
- *IBM 3480 Magnetic Tape Subsystem Description*, GA32-0042.

Input/Output Instructions

The tape subsystem uses six I/O instructions that are supplied by the System/370 design:

- Start I/O
- Start I/O Fast Release
- Test I/O
- Halt I/O
- Clear I/O
- Halt Device

Also, the tape subsystem uses the following device data streaming channel I/O instructions:

- Clear Subchannel
- Halt Subchannel
- Reset Channel Path
- Start Subchannel
- Test Pending Interruptions
- Test Subchannel

The host system sends a Start I/O, Start I/O Fast Release, or Start Subchannel instruction to start an I/O operation. These instructions send a command to the control unit for execution. See OPER 155 for the definition of the commands and their command codes.

The host system sends a Test I/O instruction to cause the channel to send a hexadecimal 00 command code to the control unit. See the description of the Test I/O command in this section for a description of the hexadecimal 00 command code.

The Halt I/O, Halt Device, or Halt Subchannel instruction causes the drive to stop executing a channel program, but does not send a command code to the control unit. All data movement stops and the drive continues to a normal ending point.

The Halt I/O or Halt Subchannel instruction can cause the channel to send an interface disconnect command sequence to the addressed drive. If the interface disconnect command sequence is sent before the initial selection is received, the ending status for the operation does not cause an interrupt when the operation is complete. An interface disconnect command sequence does not clear disconnect in.

The Clear I/O and Clear Subchannel instructions also stop an I/O operation, but at the subchannel level, and do not directly send the halt request to the addressed drive.

Channel Command Summary

Channel Command	Hex Code	Description
Assign	B7	Reserves the addressed drive to a specified channel path.
Backspace Block	27	Causes the drive to move the tape backward to the last block ID.
Backspace Block	2F	Causes the drive to move the tape backward to the last tape mark.
Control Access	E3	Permits a specified drive to be used by a host system to which it is not assigned.
Data Security Erase	97	Causes the drive to erase the tape to the end of the tape.
Erase Gap	17	Causes the drive to write an erase gap pattern.
Forward Space Block	37	Causes the drive to move the tape forward to the next block ID.
Forward Space File	3F	Causes the drive to move the tape forward to the next tape mark.
Load Display	9F	Causes a message to be displayed on the message display panel.
Locate Block	4F	Causes the drive to move the tape to the specified location of data.
Mode Set	DB	Causes a drive to be set to a specified operating mode.
No Operation	03	No operation is performed.
Read Backward	0C	Causes the drive to read in a backward direction.
Perform Subsystem Function	77	Passes control information from the control program to the subsystem.
Read Block ID	22	Causes the tape block ID to be sent to the host system.
Read Buffer	12	Causes the buffer data to be sent to the host system.
Read Buffered Log	24	Causes the stored buffered log data to be sent to the host system.
Read Device Characteristics	64	Causes up to 64 bytes of data containing installed feature information to be transferred to the host processor.
Read Forward	02	Causes the drive to read in a forward direction.
Rewind	07	Causes the drive to rewind the tape to the load point.
Rewind Unload	0F	Causes the drive to rewind the tape and unload the cartridge.
Sense	04	Causes the CU to send 32 bytes of sense data to the host system.
Sense I/O	E4	Causes the CU to send 7 bytes of subsystem ID information to the host system.
Sense Path Group ID	34	Causes the CU to send the path state byte and the 11 bytes of path group ID information to the host system.
Set Path Group ID	AF	Sends the function control byte and 11 path group ID bytes to the control unit.
Suspend Multipath Reconnection	5B	Causes a temporary connection between the addressed drive and the channel path that issued the command.
Synchronize	43	Causes the drive to be synchronized with the host system after a buffered operation.
Test I/O	00	Causes the CU to send the status byte to the host system.
Unassign	C7	Releases the addressed drive from the channel path group to which it had been reserved.
Write	01	Causes the drive to write data on the tape.
Write Tape Mark	1F	Causes the drive to write a tape mark pattern on the tape.

0 0 0 0 0 0 0 0 0 0

Channel Command Summary

CHANNEL COMMAND	HEX CODE	DESCRIPTION
Assign	B7	Reserves the addressed drive to a specified channel path.
Backspace Block	27	Causes the drive to move the tape backward to the last block ID.
Backspace File	2F	Causes the drive to move the tape backward to the last tape mark.
Control Access	E3	Permits a specified drive to be used by a host system to which it is not assigned.
Data Security Erase	97	Causes the drive to erase the tape to the end of the tape.
Erase Gap	17	Causes the drive to write an erase gap pattern.
Forward Space Block	37	Causes the drive to move the tape forward to the next block ID.
Forward Space File	3F	Causes the drive to move the tape forward to the next tape mark.
Load Display	9F	Causes a message to be displayed on the message display panel.
Locate Block	4F	Causes the drive to move the tape to the specified location of data.
Mode Set	DB	Causes a drive to be set to a specified operating mode.
No Operation	03	No operation is performed.
Read Backward	0C	Causes the drive to read in a backward direction.
Read Block ID	22	Causes the tape block ID to be sent to the host system.
Read Buffer	12	Causes the buffer data to be sent to the host system.
Read Buffered Log	24	Causes the stored buffered log data to be sent to the host system.
Read Forward	02	Causes the drive to read in a forward direction.
Rewind	07	Causes the drive to rewind the tape to the load point.
Rewind Unload	0F	Causes the drive to rewind the tape and unload the cartridge.
Sense	04	Causes the CU to send 32 bytes of sense data to the host system.
Sense I/O	E4	Causes the CU to send 7 bytes of subsystem ID information to the host system.
Sense Path Group ID	34	Causes the CU to send the path state byte and the 11 bytes of path group ID information to the host system.
Set Path Group ID	AF	Sends the function control byte and 11 path group ID bytes to the control unit.
Suspend Multipath Reconnection	5B	Causes a temporary connection between the addressed drive and the channel path that issued the command.
Synchronize	43	Causes the drive to be synchronized with the host system after a buffered operation.
Test I/O	00	Causes the CU to send the status byte to the host system.
Unassign	C7	Releases the addressed drive from the channel path group to which it had been reserved.
Write	01	Causes the drive to write data on the tape.
Write Tape Mark	1F	Causes the drive to write a tape mark pattern on the tape.

Channel Command Descriptions

Assign (X'B7')

The Assign command assigns the addressed drive to a specific channel path. This command takes the place of the physical partitioning switches that are present on tape subsystems of earlier design. The Assign command executes even if the addressed drive is not ready or if it is not installed in the subsystem. Once assigned, a drive can be used by the assigned channel paths only. If a command other than the four shown below as exceptions is sent to the drive along a channel path to which the drive is not assigned, a Unit Check (status bit 6) is set in the initial status for the command and Assigned (sense byte 0 bit 7) is set.

However, the following four commands can be sent to a drive over any channel path:

- Control Access
- Sense
- Sense Path Group ID
- Set Path Group ID

The Assign command is a supervisor command. Therefore, if a Mode Set command that inhibits execution of supervisor commands precedes the Assign command, the Assign command fails, and Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set.

The Assign command sends 11 bytes of information (named an argument) to the subsystem. These 11 bytes can contain all zeros, which assign the addressed drive to the single channel path over which the command was received. If the channel path is not grouped by a Set Path Group ID command, the control unit assumes that the group consists of a specific group of one channel path. If the 11 bytes contain non-zeros, they are interpreted as a path group ID, as determined by the Set Path Group ID command (described later in this section). The contents of the 11-byte argument are compared, and if they match a group of channel paths that have the same group ID, the addressed drive is assigned to all those channel paths. However, if no channel-path groups have the same path group ID, Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set. The 11-byte argument does not have to match the path group ID of the channel path over which the Assign command is sent. A drive can be assigned to several channel path groups by several Assign commands. The assign is active immediately after each assign command completes processing.

The assign can be removed in several ways:

- Power-On-Reset in the control unit
- System Reset on all assigned channel paths
- Control Access command with hexadecimal 40 specified
- Unassign command

A system reset over a single channel path removes all drive assigns to that path. The set of assigned channel paths can be made over by a Set Path Group ID command (described later in this section).

> **Note:** A host can send the Assign command to a drive only when that drive is not assigned to any channel path, or when the drive has already been assigned to the channel path over which the Assign command is sent. If a host sends an Assign command, but the addressed drive is not assigned to the sending channel path, the command fails and Unit Check (status bit 6) and Assigned (sense byte 0 bit 7) are set.

Backspace Block (X'27')

The Backspace Block command causes the addressed drive to move the tape one data block in the backward direction.

Backspace File (X'2F')

The Backspace File command causes the addressed drive to move the tape one tape file in the backward direction. A tape file is the data written in an area of tape between two tape marks.

Control Access (X'E3')

The Control Access command permits a host system to have special use of a drive even if the drive is assigned to a different host system. This command executes even if the addressed drive is not ready or is not online in the subsystem.

The special access can be used in the following ways:

- To permit a host that already has assignment of a specific drive to make a password to permit another host to access the drive.
- To permit a host that does not have assignment of a specific drive to send a channel program to that drive even if the drive would not normally execute a channel program from a host to which it is not assigned. The Control Access command executes only if it is either the first command in a chain of commands, or immediately after a Sense command, which is the first command in a chain of commands. A password that was assigned before must also be specified with this use of the Control Access command.

12 bytes of argument information must be sent from the host to the control unit when the Control access command is sent. If fewer than 12 bytes are sent, the Unit Check status bit and Command Reject sense bit are set to 1. If more than 12 bytes are specified, only the first 12 bytes are sent as the argument, and the Incorrect Length bit is set by the channel unless the Suppress Length Indication bit in the CCW is set to 1.

The 12-byte argument has two parts. Byte 0 contains the mode-of-use code and must contain the values of hexadecimal 00, 40, or 80. The remaining 11 bytes contain a password and should not contain all zeros, except when mode-of-use code hexadecimal 40 is specified. Mode-of-use code hexadecimal 40 ignores the contents of bytes 1 through 11. If byte 0 contains any value other than hexadecimal 00, 40, or 80, or if the remaining 11 bytes of the argument contain all zeros and the mode-of-use code is hexadecimal 00 or 80, the command is rejected, and Unit Check status bit and the Command Reject sense bit are set to 1. The mode-of-use codes are used as follows:

- **Set Password - Hexadecimal 00:** Mode-of-use code hexadecimal 00 can be used only by a host that already has assignment of the addressed drive. The Control Access command sets up a password for the addressed drive. Then, another host can access the drive by specifying the correct password in a Control Access command. Once a password has been set up, it remains associated with the drive until all assignments of that drive are cleared.

- **Generalized Unassign - Hexadecimal 40:** Mode-of-use code hexadecimal 40 clears the assignment of the addressed drive from all channel paths.

  If a password was set up by another Command Access command, the password in bytes 1 through 11 must match the password set up. If the passwords do not match, the command is rejected, and the Unit Check status bit and the Command Reject sense bit are set to 1.

  If the Control Access command is sent on a channel path that does not have assignment of the addressed drive, the command fails, and the Unit Check status bit and the Command Reject sense bit are set to 1.

- **Request Temporary Unassignment - Hexadecimal 80:** Mode-of-use code hexadecimal 80 causes the Assign Protection to be stopped for a specific channel program. The password in bytes 1 through 11 are compared to the password that was set up by an earlier Control Access command using mode-of-use code hexadecimal 00. If the passwords match, the channel program is permitted to execute.

Data Security Erase (X'97')

The Data Security Erase command erases the data from the tape. The data is erased from that point of the tape when the command is sent to the physical end-of-tape.

The Data Security Erase command must be command-chained from an Erase Gap command. If it is not, unit check (status bit 6) and command reject (sense byte 0 bit 0) are set. When the command is correctly command-chained, channel end (status bit 4) is set during initial status, which disconnects the channel to perform other work during the erase operation. When the erase operation has completed processing, the channel is reconnected, and device end (status bit 5) is set.

The Data Security Erase command cannot set unit exception (status bit 7).

Erase Gap (X'17')

The Erase Gap command writes a special pattern on 7.8 mm (0.3 inch) of tape.

Forward Space Block (X'37')

The Forward Space Block command causes the addressed drive to move the tape one data block in the forward direction.

Forward Space File (X'3F')

The Forward Space File command causes the addressed drive to move the tape one tape file in the forward direction. A tape file is the data that is written in an area of tape between two tape marks.

Load Display (X'9F')

The Load Display command sends 17 bytes of data from the channel to the control unit. This data controls the message display (and the automatic cartridge loader feature) on the addressed drive. If the channel sends fewer than 17 bytes of data, the command fails, and unit check (status bit 6) and command reject (sense byte 0 bit 0) are set. If more than 17 bytes of data are specified, the channel sends only the first 17 bytes.

After the 17 bytes of data are sent to the subsystem, channel end (status bit 4) is sent to the host. Device end (status bit 5) is sent to the host along with any error status after the message display has been loaded.

The Load Display command is a supervisor command. If a Mode Set command, which inhibits supervisor commands, precedes a Load Display command in a command chain, the Load Display command fails, with unit check (status bit 6) and command reject (sense byte 0 bit 0) set.

Format Control Byte

The format control byte is the first byte of the 17 bytes that were sent from the channel to the addressed drive. This byte controls the way the drive displays the remaining 16 bytes.

Bits 0 - 2 New Message Overlay

- When lit the messages in bytes 1-8 and 9-16 are overlayed with a drive message when the drive next starts tape motion.
- Bit 1 overlays the messages in bytes 1-8 and 9-16 with a drive message only when the tape cartridge is physically removed from the drive.
- Bit 2 overlays the messages in bytes 1-8 and 9-16 with a drive message only when the drive becomes ready.
- Bits 0, 1, and 2 displays the messages in bytes 1-8 and 9-16 until a tape cartridge has been physically removed from the drive. Then, display only the message in bytes 9-16 until the drive becomes ready.

Bit 3, Alternate Messages

When bit 3 is set to 0, the drive displays only the message that is specified in bit 5.

When bit 3 is set to 1, the drive displays both messages specified in bytes 1-8 and 9-16, respectively, alternating them on the message display. When bit 3 is set to 1, bits 4 and 5 are ignored.

Bit 4, Blink Message

When bit 4 is set to 0, the message specified by the setting of bit 5 is not blinked.

When bit 4 is set to 1, the message specified by the setting of bit 5 is displayed repeatedly for about 2 seconds with an interval of about 0.5 seconds between each display. Bit 4 is ignored when bit 3 is set to one.

Bit 5, Display Low/High Message

When bit 5 is set to 0, the message specified in bytes 1-8 is displayed.

When bit 5 is set to 1, the message specified in bytes 9-16 is displayed.

Bits 6, Reserved

Bit 7, Load Type

Bit 7 is valid only with an MVS operating system, an automatic cartridge loader feature installed on the drive, and the automatic cartridge loader mode switch on its operator panel set to System.

1. If these conditions are not met the setting of bit 7 is ignored.
2. With the above conditions set, bit 7 set to 1 inhibits the message from appearing on the drive message display if the automatic cartridge loader is capable of performing the automatic load (a cartridge is available in the input stack and space is available in the output stack). The cartridge is loaded.

   If the automatic cartridge loader is not capable, the message appears on the drive message display.
3. With the above conditions set, bit 7 set to 0 permits the message to appear on the drive message display.

The operator should handle messages on the drive message display as an action prompt.

After the 17 bytes of data are transferred to the subsystem, the channel end status bit is sent to the host. The device end status bit is sent to the host processor along with any error status after the host message has been sent to the drive.

Locate Block (X'4F')

The Locate Block command positions the tape on the addressed drive to permit the host to write or read a specific block on the tape.

Four bytes of data must be supplied to the control unit as an argument to the Locate Block command. These four bytes usually are the first four bytes of the block identifier, which were returned as a result of a Read Block ID command that was sent before. If fewer than four bytes are supplied, the unit check status bit and the command reject bit are set to 1, and the command fails. If more than four bytes are supplied, only the first four bytes are used. When a locate operation starts, the control unit disconnects from the channel and the drive. The drive then searches at high speed for the location specified. When the drive reaches the approximate location of the block, the control unit reconnects to the drive, and the drive searches at recording speed for the specific data block or file mark that was requested.

The control unit sends channel end status to the host after the Locate Block command argument is received. The device end status is sent to the host when the command completes the operation. A unit check status is sent along with the device end status if the specified block cannot be found.

If the specific data block or file mark cannot be found, the control unit assumes that the user is moving the tape for a write operation. In this case, the drive searches for the data block or file mark that precedes the one specified in the Locate Block command argument. The drive moves the tape after the preceding block or file mark so that the host can write the data block or file mark that is being located. However, if the control unit is not correct because a non-write operation is requested, the non-write command fails, and the unit check status bit and the locate block function failed sense bit are set to one.

If the Locate Block command does not find the data block, the tape location is not known. However, the host system can use the Read Block ID command to determine the tape location relative to the start of tape.

Mode Set (X'DB')

The Mode Set command sends one byte of mode control information from main storage to the control unit. All controls specified by the Mode Set command (except tape format, bits 0 and 1) are only in effect for the commands in the chain following the Mode Set command. If the subsystem does not receive a Mode Set command before the current executing command, the default values are assumed. The Mode Set command is a supervisor command. If another Mode Set command inhibits supervisor commands in a command chain in which a second Mode Set command appears, the second Mode Set command fails, and the unit check status bit and the command reject sense bit are set to one.

This command is performed even though the addressed drive is not ready or is not online in the subsystem.

The format of the byte of mode control information that is sent from main storage to the control unit is as follows:

Bits 0 and 1 - Tape Format: These bits must contain X'00', which is the default value. If a combination other than X'00' is specified, the command fails, and the unit check status bit and the command reject sense bit are set to one.

These bits have meaning only if the tape is located at the beginning-of-tape (BOT). The first command that causes the tape to move must be a write-type command.

Bit 2 - Write Mode: Bit 2 is set to zero to cause execution in buffered write mode, and set to one to cause execution in tape write mode. The default value is zero.

Bit 3 - Inhibit Supervisor Commands: When a zero is specified in this bit, any supervisor command can execute after this Mode Set command appears in a command chain. When a one is specified in this bit, any supervisor command that appears after this Mode Set command fails, and the unit check status bit and command reject sense bit are set to one.

Bit 4 - ~~Extended~~ Improved Data Recording ~~Format~~ Capability Mode: Bit 4 is set to 1 to turn on the ~~extended~~ improved data recording format for the next write operation.

Bits 5 through 7 - Reserved: The values in these bits should be set to 0.

No-Operation (NOP) (X'03')

The No-Operation (NOP) command causes no operations to be performed in the drive. The control unit sets channel end (status bit 4) and device end (status bit 5) when it receives a NOP command.

0 0 0 0 0 0 0 0 0 0

Data Security Erase (X'97')

The Data Security Erase command erases the data from the tape. The data is erased from that point of the tape when the command is sent to the physical end of tape.

The Data Security Erase command must be command-chained from an Erase Gap command. If it is not, Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set. When the command is correctly command-chained, Channel End (status bit 4) is set during initial status, which disconnects the channel to perform other work during the erase operation. When the erase operation has completed processing, the channel is reconnected, and Device End (status bit 5) is set.

The Data Security Erase command cannot set Unit Exception (status bit 7).

Erase Gap (X'17')

The Erase Gap command writes a special pattern on 7.8 mm (0.3 inch) of tape.

Forward Space Block (X'37')

The Forward Space Block command causes the addressed drive to move the tape one data block in the forward direction.

Forward Space File (X'3F')

The Forward Space File command causes the addressed drive to move the tape one tape file in the forward direction. A tape file is the data that is written in an area of tape between two tape marks.

Load Display (X'9F')

The Load Display command sends 17 bytes of data from the channel to the control unit. This data controls the message display (and the automatic cartridge loader feature) on the addressed drive. If the channel sends fewer than 17 bytes of data, the command fails, and Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set. If more than 17 bytes of data are specified, the channel sends only the first 17 bytes.

After the 17 bytes of data are sent to the subsystem, Channel End (status bit 4) is sent to the host. Device End (status bit 5) is sent to the host along with any error status after the message display has been loaded.

The Load Display command is a supervisor command. If a Mode Set command, which inhibits supervisor commands, precedes a Load Display command in a command chain, the Load Display command fails, with Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) set.

Format Control Byte

The format control byte is the first byte of the 17 bytes that were sent from the channel to the addressed drive. This byte controls the way that the drive displays the remaining 16 bytes.

Bits 0 - 2 New Message Overlay

- When lit the messages in bytes 1-8 and 9-16 are overlayed with a drive message when the drive next starts tape motion.
- Bit 1 overlays the messages in bytes 1-8 and 9-16 with a drive message only when the tape cartridge is physically removed from the drive.
- Bit 2 overlays the messages in bytes 1-8 and 9-16 with a drive message only when the drive becomes ready.
- Bits 0, 1, and 2 displays the messages in bytes 1-8 and 9-16 until a tape cartridge has been physically removed from the drive. Then, display only the message in bytes 9-16 until the drive becomes ready.

Bit 3, Alternate Messages

When bit 3 is set to 0, the drive displays only the message that is specified in bit 5.

When bit 3 is set to 1, the drive displays both messages specified in bytes 1-8 and 9-16, respectively, alternating them on the message display. When bit 3 is set to 1, bits 4 and 5 are ignored.

Bit 4, Blink Message

When bit 4 is set to 0, the message specified by the setting of bit 5 is not blinked.

When bit 4 is set to 1, the message specified by the setting of bit 5 is displayed repeatedly for about 2 seconds with an interval of about 0.5 seconds between each display. Bit 4 is ignored when bit 3 is set to 1.

Bit 5, Display Low/High Message

When bit 5 is set to 0, the message specified in bytes 1-8 is displayed.

When bit 5 is set to 1, the message specified in bytes 9-16 is displayed.

Bits 6, Reserved

Bit 7, Load Type

Bit 7 is valid only with an MVS operating system, an automatic cartridge loader feature installed on the drive, and the automatic cartridge loader mode switch on its operator panel set to System.

1. **If these conditions are not met the setting of bit 7 is ignored.**

2. **With the above conditions set, bit 7 set to 1 inhibits the message from appearing on the drive message display if the automatic cartridge loader is capable of performing the automatic load (a cartridge is available in the input stack and space is available in the output stack). The cartridge is loaded.**

   If the automatic cartridge loader is not capable, the message appears on the drive message display.

3. **With the above conditions set, bit 7 set to 0 permits the message to appear on the drive message display.**

The operator should handle messages on the drive message display as an action prompt.

After the 17 bytes of data are transferred to the subsystem, the channel end status bit is sent to the host. The device end status bit is sent to the host processor along with any error status after the host message has been sent to the drive.

Locate Block (X'4F')

The Locate Block command positions the tape on the addressed drive to permit the host to write or read a specific block on the tape.

4 bytes of data must be supplied to the control unit as an argument to the Locate Block command. These 4 bytes usually are the first 4 bytes of the block identifier, which were returned as a result of a Read Block ID command that was sent before. If fewer than 4 bytes are supplied, the Unit Check status bit and the Command Reject bit are set to 1, and the command fails. If more than 4 bytes are supplied, only the first 4 bytes are used. When a locate operation starts, the control unit disconnects from the channel and the drive. The drive then searches at high speed for the location specified. When the drive reaches the approximate location of the block, the control unit reconnects to the drive, and the drive searches at recording speed for the specific data block or file mark that was requested.

The control unit sends channel end status to the host after the Locate Block command argument is received. The device end status is sent to the host when the command completes the operation. A unit check status is sent along with the device end status if the specified block cannot be found.

If the specific data block or file mark cannot be found, the control unit assumes that the user is moving the tape for a write operation. In this case, the drive searches for the data block or file mark that precedes the one specified in the Locate Block command argument. The drive moves the tape after the preceding block or file mark so that the host can write the data block or file mark that is being located. However, if the control unit is not correct because a non-write operation is requested, the non-write command fails, and the Unit Check status bit and the Locate Block Function Failed sense bit are set to 1.

If the Locate Block command does not find the data block, the tape location is not known. However, the host can use the Read Block ID command to determine the tape location relative to the start of tape.

Mode Set (X'DB')

The Mode Set command sends 1 byte of mode control information from main storage to the control unit. All controls specified by the Mode Set command (except tape format, bits 0 and 1) are only in effect for the commands in the chain following the Mode Set command. If the subsystem does not receive a Mode Set command before the current executing command, the default values are assumed. The Mode Set command is a supervisor command. If another Mode Set command inhibits supervisor commands in a command chain in which a second Mode Set command appears, the second Mode Set command fails, and the Unit Check status bit and the Command Reject sense bit are set to 1.

This command executes even if the addressed drive is not ready or is not on-line in the subsystem.

The format of the byte of mode control information that is sent from main storage to the control unit is as follows:

Bits 0 and 1 - Tape Format: These bits must contain 00, which is the default value. If a combination other that 00 is specified, the command fails, and the Unit Check status bit and the Command Reject sense bit are set to 1.

These bits have meaning only if the tape is located at the beginning-of-tape (BOT). The first command that causes the tape to move must be a Write-Type command.

Bit 2 - Write Mode: Bit 2 is set to zero to cause execution in buffered write mode, and set to one to cause execution in tape write mode. The default value is zero.

Bit 3 - Inhibit Supervisor Commands: When a zero is specified in this bit, any supervisor command can execute after this Mode Set command appears in a command chain. When a one is specified in this bit, any supervisor command that appears after this Mode Set command fails, and the Unit Check status bit and Command Reject sense bit are set to 1.

Bits 4 through 7 - Reserved: The values in these bits should be set to 0.

No-Operation (NOP) (X'03')

The No-Operation (NOP) command causes no operations to execute in the drive. The control unit sets Channel End (status bit 4) and Device End (status bit 5) when it

Channel Commands (Continued)

Read Backward (X'0C')

Read Backward is similar to Read Forward, except that the tape moves in a backward direction. The data is passed to the channel in a backward sequence and the channel must place it in the correct sequence in the host system storage.

The control unit will pre-read data in the backward direction in the same way as in the forward direction. See "Read Forward" in this section.

Read Block ID (X'22')

The Read Block ID command sends two 4-byte block identifiers to the host system. If the host requests fewer than 8 bytes, only the requested number of bytes are sent. If the host requests more than 8 bytes, the control unit sends only 8 bytes.

The Read Block ID command executes even if the addressed drive is not ready, or if it is not on-line in the subsystem.

The bits in each 4-byte block identifier are identified from high order to low order, with the higher-order bits having lower bit position values.

BIT POSITION	DESCRIPTION
31-12	Logical block position
11-8	Reserved, always zero
7-1	Physical reference value
0	Reserved, always zero

The physical reference value (bits 1 through 7) identifies the approximate physical location of a data block or file mark on a tape. The physical reference value of the block IDs for the next two data blocks or file marks may or may not be the same. The first data block or file mark after the tape cartridge is loaded has a physical reference value of hexadecimal 01.

The last 20 bits (bits 12 through 31) of a block ID contain the sequential count of the data block or file mark on the active tape. The first data block or file mark after the load point is sequential count zero. A block ID identifies a data block or file mark from the host, and does not see the buffer action of the control unit.

The block ID at any point of processing is the next data block or file mark that appears to the host to be on the tape between the current data block or file mark and the physical end of tape. The first block ID describes the data block that is about to be passed between the host and the subsystem in either read or write mode. In read-backward mode, the first block ID describes the latest data block sent to the host.

The second block ID describes to the host:

- The next data block that is to be written to the tape from the control unit buffer for write mode.
- The next data block that is to be read from the tape to the control unit for read mode.
- The latest data block that was read from the tape to the control unit buffer for read-backward mode.

If the control unit is not performing any pre-buffer operations, the first and second block IDs are the same.

The value of the difference between the logical block position part of the two block IDs indicates the number of data blocks in the control unit buffer when the Read Block ID command is executed. The result of subtracting the logical block position part of the second block ID from the logical block position of the first block ID indicates the direction of tape movement before the Read Block ID command was sent. If the result is negative, the control unit buffer is in read mode. If the result is positive, the control unit buffer is in write or read-backward mode. If the logical block position parts of both block IDs are the same, the control unit is not performing any pre-buffer operations.
Examples:

Write Commands Precede the Read Block ID Command:

The first block ID identifies the next block that the host will write. The second block ID identifies the next block that the control unit buffer will write to the tape. The result is positive, which indicates that four blocks of data are in the buffer and the direction is forward.

Read Commands Precede the Read Block ID Command:

The first block ID identifies the next block that the host will read. The second block ID identifies the next block that is to be read from the tape to the control unit buffer. The result is negative, which indicates that four blocks of data are in the buffer and the direction is forward.

Read-Backward Commands Precede the Read Block ID Command:

The first block ID identifies the next block that the host will read in the forward direction. The second block ID identifies the latest block that was read from the tape to the control unit buffer. Because the result is positive, there are four blocks in the buffer and the tape movement is in the backward direction.

The control unit assumes that the Read, Write, or Read-Backward commands will continue. The next operation that is not a command that the control unit expects, causes pre-buffered write data to be written to tape, or causes pre-buffered read data to be erased. The tape is then located at the point necessary to execute the unexpected command. The unexpected command is held in the subchannel by a channel command retry until the control unit completes the operations necessary to execute it. When the control unit receives a command that is not the expected command, no pre-buffering of read data is performed until the beginning-of-tape (BOT) is indicated, a Locate command is executed, or a tape mark is read or written.

Read Buffer (X'12')

The Read Buffer command causes the host to get the buffered write-type data that the control unit has not yet written to tape. For each Read Buffer command, the host receives one block of data in a first in/first out sequence until the buffer for the addressed drive is empty. This command is usually sent by the host when the drive or subsystem has an error, and cannot write data from the buffer to the tape.

The Read Buffer command executes even if the drive is not ready, or is not on-line in the subsystem.

The block identifier is the first data block that is received from the buffer. If the host receives all the buffered data blocks from the control unit, the block identifier accurately identifies the next data block that is to be written on the tape. However, if the host does not receive all the data blocks, the block identifier is not accurate.

To ensure that all of the data block is received from the control unit buffer, the channel command words (CCWs) for the Read Buffer command can be made to cause the host to read the data back from the control unit, using the value in sense byte 31. Sense byte 31 contains a count of 4,096-byte blocks of data that are in the control unit buffer for the addressed drive. Sense byte 31 indicates the amount of main storage that the host must have to receive the buffered data.

The Read Block ID command can determine the number of data blocks that are in the control unit buffer. This information sets the number of Read Buffer commands to execute.

Note: Data blocks larger than 131,067 bytes are written from the host using the tape synchronous mode only. When writing in tape synchronous mode or tape write mode, a Read Buffer command cannot get the data block. The block identifier that is returned by the Read Block ID command immediately after a tape synchronous mode or tape write mode write error contains a count of the completed data blocks that have been sent across the channel. This enables the host error recovery routines to know how many data blocks were written on the tape before the failure. For such an event, the record is complete when the error occurs, and the host error recovery routines can start the Write command again.

Channel Commands (Continued)

Perform Subsystem Function (X'77')

The perform subsystem function command is used to pass control information from the control program to the subsystem. The command passes a variable amount of data depending on the order being executed. If the channel transfers more bytes than the the order requires, only the number of bytes required by the order are accepted. If the channel transfers less bytes than required for the order of if the command contains an undefined or invalid order, unit check status is presented with sense data indicating ERA 27 (command reject). A minimum of two bytes must be transferred for every order.

BYTE	ORDER
BYTE 0	X'80' - Active forced error logging X'81' - Deactivate forced error logging X'82' - Activate logical write protect X'83' - Deactivate forced write protect X'90' - Test device
BYTE 1	Flag reserved - must be 0
BYTE 2	Parameters if any. See order definition.

Activate Forced Error Logging Order

This order requires one parameter byte in addition to the flag byte passed with the command.

BYTE 2	ACTIVATION MODE X'01' - Implicit activation (all devices) X'02' - Explicit activation (addressed device)

Deactivate Forced Error Logging Order

This order requires one order parameter byte n addition to the flag byte passed with the command.

BYTE 2	DEACTIVATION MODE X'01' - Implicit deactivation (all implicitly activated devices) X'02' - Explicit deactivation (addressed device)

Activate Logical Write Protect

This order activates the logical write protect facility and does not require a parameter byte.

Deactivate Logical Write Protect

This order deactivates the logical write protect facility and does not require a parameter byte.

Test Device

This order is equivalent to the No-operation function of the load display command. It can be issued at anytime to verify the state of the device and does not require a parameter byte.

Read Backward (X'0C')

A Read Backward command is similar to the Read Forward command, except that the tape moves in a backward direction. The data is passed to the channel in a backward sequence and the channel must place it in the correct sequence in the host system storage.

The control unit will pre-read data in the backward direction in the same way as in the forward direction. See "Read Forward" in this section.

Read Block ID (X'22')

The Read Block ID command sends two 4 byte block identifiers to the host system. If the host system requests fewer than eight bytes, only the requested number of bytes are sent. If the host requests more than eight bytes, the control unit sends only eight bytes.

The Read Block ID command is performed even though the addressed drive is not ready, or if it is not on-line in the subsystem.

The bits in each 4-byte block identifier are identified from high order to low order, with the higher-order bits having lower bit position values.

BIT POSITION	DESCRIPTION
0	Reserved;always 0
1-7	Physical reference value
8-9	Format mode 00 = 3480 format 01 = Reserved 10 = 3480 Improved Data Recording ~~Capacity~~ Capability 11 = Reserved
10-31	Local block number

The physical reference value (bits 1 through 7) identifies the approximate physical location of a data block or file mark on a tape. The physical reference value of the block IDs for the next two data blocks or file marks may or may not be the same. The first data block or file mark after the tape cartridge is loaded has a physical reference value of X'01'.

The last 22 bits (bits 10 through 31) of a block ID contain the sequential count of the data block or file mark on the active tape. The first data block or file mark after the load point is sequential count zero. A block ID identifies a data block or file mark from the host, and does not see the buffer action of the control unit.

The block ID at any point of processing is the next data block or file mark that appears to the host system to be on the tape between the current data block or file mark and the physical end of tape. The first block ID describes the data block that is about to be passed between the host system and the subsystem in either read or write mode. In read backward mode, the first block ID describes the latest data block sent to the host system.

The second block ID describes to the host:

- The next data block that is to be written to the tape from the control unit buffer for write mode.
- The next data block that is to be read from the tape to the control unit for read mode.
- The latest data block that was read from the tape to the control unit buffer for read backward mode.

If the control unit is not performing any pre-buffer operations, the first and second block IDs are the same.

The value of the difference between the logical block position part of the two block IDs indicates the number of data blocks in the control unit buffer when the Read Block ID command is executed. The result of subtracting the logical block position part of the second block ID from the logical block position of the first block ID indicates the direction of tape movement before the Read Block ID command was sent. If the result is negative, the control unit buffer is in read mode. If the result is positive, the control unit buffer is in write or read-backward mode. If the logical block position parts of both block IDs are the same, the control unit is not performing any pre-buffer operations.

Examples:

Write Commands Precede the Read Block ID Command:

The first block ID identifies the next block that the host will write. The second block ID identifies the next block that the control unit buffer will write to the tape. The result is positive, which indicates that four blocks of data are in the buffer and the direction is forward.

Read Commands Precede the Read Block ID Command:

The first block ID identifies the next block that the host will read. The second block ID identifies the next block that is to be read from the tape to the control unit buffer. The result is negative, which indicates that four blocks of data are in the buffer and the direction is forward.

Read-Backward Commands Precede the Read Block ID Command:

The first block ID identifies the next block that the host will read in the forward direction. The second block ID identifies the latest block that was read from the tape to the control unit buffer. Because the result is positive, there are four blocks in the buffer and the tape movement is in the backward direction.

The control unit assumes that the Read, Write, or Read Backward commands will continue. The next operation that is not a command that the control unit expects, causes pre-buffered write data to be written on tape, or causes pre-buffered read data to be erased. The tape is then located at the point necessary to execute the unexpected command. The unexpected command is held in the subchannel by a channel command retry until the control unit completes the operations necessary to execute it. When the control unit receives a command that is not the expected command, no pre-buffering of read data is performed until the beginning-of-tape (BOT) is indicated, a Locate command is performed, or a tape mark is read or written.

Read Buffer (X'12')

The Read Buffer command causes the host system to get the buffered write-type data that the control unit has not yet written to tape. For each Read Buffer command, the host receives one block of data in a first in/first out (FIFO) sequence until the buffer for the addressed drive is empty. This command is usually sent by the host when the drive or subsystem has an error, and cannot write data from the buffer to the tape.

The Read Buffer command is performed even though the drive is not ready, or is not on-line in the subsystem.

The block identifier is the first data block that is received from the buffer. If the host system receives all the buffered data blocks from the control unit, the block identifier accurately identifies the next data block that is to be written on the tape. However, if the host does not receive all the data blocks, the block identifier is not accurate.

To ensure that all of the data block is received from the control unit buffer, the channel command words (CCWs) for the Read Buffer command can be made to cause the host to read the data back from the control unit, using the value in sense byte 31. Sense byte 31 contains a count of X'1000' (4,096) byte blocks of data that are in the control unit buffer for the addressed drive. Sense byte 31 indicates the amount of main storage that the host must have to receive the buffered data.

The Read Block ID command can determine the number of data blocks that are in the control unit buffer. This information sets the number of Read Buffer commands to execute.

Read Device Characteristics - (X'64')

A read device characteristics command causes up to 64 bytes if data to be transferred to the channel.

BYTE	CHARACTERISTICS
0 - 1	Control unit type X'3480'
2	Control unit model - X'11' = A11 X'22' = A22
2 - 4	Drive type - X'3480'
6 - 8	Binary 0's
9	Drive and Control unit features - Bit 0 = Automatic cartridge loader Bit 1 = Reserved Bit 2 = PSF base support Bit 3 through 7 reserved
10	Device class code (X'80')
11	Device type code (X'80')
12-39	Binary 0's
40	MDR Record ID for device (X'41')
41	OBR Record ID for device (X'80')
42-63	Binary 0's

Note: Data blocks larger than 131,067 bytes are written from the host using the tape synchronous mode only. When writing in tape synchronous mode or tape write mode, a Read Buffer command cannot get the data block. The block identifier that is returned by the Read Block ID command immediately after a tape synchronous mode or tape write mode write error contains a count of the completed data blocks that have been sent across the channel. This enables the host system error recovery routines to know how many data blocks were written on the tape before the failure. For such an event, the record is complete when the error occurs, and the host system error recovery routines can start the Write command again.

0 0 0 0 0 0 0 0 0 0

Read Buffered Log (X'24')

The Read Buffered Log command sends 32 bytes of buffered log data (sense information, format 21) to the host from the control unit for the addressed drive.

The Read Buffered Log command executes even if the addressed drive is not ready or is not on-line in the subsystem.

Read Forward (X'02')

The Read Forward command causes the drive to read a block of data into the control unit data buffer. Then the control unit sends the data over the host system channel one byte at a time at the channel data rate. The byte count in the channel command word (CCW) may not equal the length of the data block. When the channel stops requesting data bytes, the control unit may discard any data remaining in the data buffer.

If a tape mark is read instead of a data block, a unit exception is sent by the control unit and no data is read.

After receiving the Read command, the control unit will disconnect from the channel by sending a Channel End and Device End or a channel command retry. This is done to let the channel to perform other host system work while the data is being read into the data buffer.

After the first Read command to a drive, the control unit will pre-read data blocks from the tape and hold them in the data buffer.

Rewind (X'07')

The Rewind command rewinds the tape to the start of tape. The control unit sets Channel End (status bit 4) in initial status and disconnects itself from the channel during the rewind operation. When the rewind operation has completed, the control unit sends Device End (status bit 5) and error status information, if any, to the host.

Rewind Unload (X'0F')

The Rewind Unload command rewinds the tape into the cartridge, which permits the cartridge to be removed from the drive.

Sense (X'04')

The Sense command sends 32 bytes of sense information (format 20) to the host. The host should send the Sense command when the control unit sets the Unit Check status bit.

> **Note:** Until the host that received the Unit Check status bit sends a command other than Test I/O or NOP, a contingent connection is maintained from the control unit for the addressed drive to that host. Until the contingent connection is cleared, the addressed drive appears to be busy to any other host that attempts to address the drive.

Sense I/D (X'E4')

The Sense I/D command sends seven bytes of identification information to the host. This information identifies the subsystem by drive and model number.

This command executes even if:

- Intervention required (sense byte 0 bit 1) is on
- The addressed drive is not ready (no tape cartridge is loaded)
- The addressed drive is not installed in the subsystem

The format of the seven bytes is as follows:

BYTE	DESCRIPTION OF CONTENTS
0	Hexadecimal FF
1-2	Control Unit Type Number
3	Control Unit Model Number
4-5	Tape Drive Type Number
6	Tape Drive Model Number

Sense Path Group ID (X'34')

The Sense Path Group ID command sends 12 bytes of channel path information from the control unit to the channel. The first byte is the path-state byte, and the remaining 11 bytes contain the path-group identifier. The bit assignments of the path-state byte are: bits 0 and 1 contain the grouping status, bits 2 and 3 contain the assignment status, bit 4 contains the mode status, and bits 5 through 7 are reserved and contain all zeros.

Set Path Group ID (X'AF')

The Set Path Group ID command identifies a host system and specific channel path to the addressed drive. The subsystem can then determine which host system to reconnect to over different channel paths. This path group ID is also used as the argument by the Assign command. The Set Path Group ID command is especially useful when the subsystem is shared by more than one host in that each host has a special path group ID.

The host must specify the Set Path Group ID command to each drive that it wants to use, and the command must be sent over each channel path to be used when addressing that drive. For example, if a drive can be used as address 181 or 281 from the same host using two different channel paths, the Set Path Group ID command must be sent to that drive once for each channel path.

A drive cannot recognize a path group ID until a Set Path Group ID command has been sent to it over each channel path it can use. If a channel path is not identified as part of a path group ID, the drive assumes the path to be a single, special path group.

The Set Path Group ID command must not be included in a channel command word (CCW) chain with other commands. If the Set Path Group ID command is CCW-chained after another command, the Set Path Group ID command fails, and Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set. In addition, if the Set Path Group ID command has another command CCW-chained after it, the Set Path Group ID command executes, but the following chained command fails, and Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set. The Set Path Group ID command executes even if:

- The addressed drive is not in the ready state (no tape cartridge is loaded).
- The addressed drive is not installed in the subsystem.
- The addressed drive has not been assigned to the channel path over which the command was received.

The Set Path Group ID command sends 12 bytes of path group ID information from the host to the addressed drive. If fewer than 12 bytes are sent to the control unit, the command fails, and Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set. If more than 12 bytes are specified in the CCW, only the first 12 bytes are sent from the host.

Suspend Multipath Reconnection (X'5B')

The Suspend Multipath Reconnection command is a supervisor command used in a channel program. This command causes the addressed drive to have a connection with the channel path over which the command is received, but only for the length of time the channel program that it is a part of is active. Therefore, all the status information and data for the channel program are sent to and from the host system along the channel path that was used to send the Suspend Multipath Reconnection command. Any multipath dynamic path definitions are ignored.

If an earlier Mode Set command inhibited supervisor commands in the channel program in which the Suspend Multipath Reconnection command appears, the Suspend Multipath Reconnection command fails, and Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set.

This command executes even if the addressed drive is not ready or is not on-line in the subsystem.

Synchronize (X'43')

The Synchronize command causes synchronization between the drive and the host processor after buffered operations. This command ensures that, during a buffered write operation, all the buffered data is written on the tape and the tape is moved to receive the next record. The command completes execution only after all I/O operations for the addressed drive have completed processing and all the write data is moved from the buffer to the tape.

When write-type data has to be written from the buffer to the tape before the Synchronize command can complete execution, the data channel is disconnected by channel command retry.

The Synchronize command is normally used by the system control program before a tape volume is closed. Therefore, you do not usually have to specify the Synchronize command.

Other commands sent by the host that perform the same operation as a synchronize operation are:

- Write Tape Mark
- Erase Gap
- Locate Block
- Rewind
- Rewind Unload
- Any space command, such as Forward Space Block
- Any read-type command that follows a write-type command

As a result of the Synchronize command, no data is sent on the channel path. However, the Synchronize command is not used as an immediate command as defined in *System/370 Principles of Operation*.

> **Note:** The System/370 channel does not permit a zero-count field in a CCW. However, because no data is sent as a result of the Synchronize command and because the Synchronize command is not an immediate command, the non-zero length in the CCW normally causes an incorrect-length indication to appear in the CSW when the command completes execution. Therefore, when the Synchronize command is programmed, the Suppress Length Indication bit should be set to 1 in the CCW.

Test I/O (X'00')

The Test I/O command causes the status of the addressed drive to be sent to the host. The status byte is sent to the host system during the initial selection sequence.

If earlier status is waiting or stacked, that status is given in response to the Test I/O command. If no status is stacked and the addressed drive is not ready, a Unit Check status bit is set along with other status, if any.

The Test I/O command does not reset any contingent connections.

> **Note:** The Test I/O (TIO) host instruction sends the Test I/O command to the control unit. If an all-zero command code is used in a channel program, that command is invalid and results in a channel program check.

Unassign (X'C7')

The Unassign command terminates an earlier assignment of the addressed drive to the exclusive use of a channel path or channel path group. The command must be sent over a channel path to which the addressed drive was assigned before. When the Unassign command is sent over a channel path to which the addressed drive was assigned before, it is executed even if the drive is not ready or off-line. If the Unassign command is sent over a channel path to which the addressed drive was not assigned, the Unassign command causes Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) to be set.

The Unassign command is a supervisor command. Therefore, if a Mode Set command that inhibits execution of supervisor commands precedes the Unassign command, the Unassign command fails, and Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set.

The Unassign command passes 11 bytes of information (named an argument) to the subsystem. These 11 bytes can contain all zeros, which release the addressed drive from the assignment to the channel path group over which the command was received. If the channel path over which the command was received was not grouped by a Set Path Group ID command before, the control unit assumes that the group consists of a special group of one channel path.

If the 11 bytes contain non-zeros, they are interpreted as a channel path group ID as set up by the Set Path Group ID command (described earlier in this section). The contents of the 11-byte argument are compared to the channel path group ID assigned before, and the drive is released from those channel paths that have the same path group ID. However, if the addressed drive is not assigned to a channel path group ID that matches the one specified in the Unassign argument, Unit Check (status bit 6) and Command Reject (sense byte 0 bit 0) are set. The Unassign command does not have to contain an argument that matches the channel path group ID for the channel path over which the Unassign command was sent.

> **Note:** The Unassign command can be sent from any host processor along any assigned channel path and can release the addressed drive from any correctly specified channel path, even if that channel path is attached to another host.

Write (X'01')

The Write command causes data to be written from the host to the addressed drive. The control unit buffer makes up for the difference in data rate between the channel and the drive.

> **Note:** The drive writes variable length data on the tape. However, the drive does not keep a count of the number of bytes written. This says that a Write command from the host must be programmed with the Suppress Length Indication bit set to 1 in the Channel Command Word (CCW). If this bit is not set to 1, the channel sends an incorrect length signal to the host.

The Write command sends an initial status of zero and an ending status when both Channel End and Device End bits are set.

Write Tape Mark (X'1F')

The Write Tape Mark command writes a special pattern on the tape. One tape mark separates two files; two tape marks indicate the end of the tape.

> **Note:** A block ID is assigned to a tape mark when it is read or written, but the block ID is not physically written on the tape.

Control Unit to Drive Operation

To start an I/O operation to the drive an initial selection of the drive is first performed.

Note: Control units send commands, drive addresses, and write data across the device control bus (DCB) and receive the drive address (complemented) and status information from the drives across the DCB. Control units receive read data from the drives across the read data bus.

Initial Selection

To start an initial selection sequence the control unit activates 'select out' 1 to the drive by setting bit 0 of the device tag register (DTR). The DTR is an external register that is used by the microcode to transfer control tags to and from the drive across the DCB. Each drive removes its own 'alert' 2 by testing for the device control bus being clear.

Note: An alert is a signal given by the drive and is used to gain the attention of the control unit after the completion of a disconnected drive operation.

When the DCB is cleared of 'alerts' the control unit places the drive address on the bus and activates 'address out' 4 by setting bit 1 of the DTR.

The control unit sets bit 2 of the DCR 3 and switches the bi-directional bus to the send (write) mode. The drive address on the bi-directional bus is then gated to the drive.

The drive activates 'address in' 5 to the control unit by setting bit 5 of the DTR. The control unit switches the bi-directional bus to the receive (read) mode by setting the DCR bit 2 6 to zero (read) and waits for a response from the drive. The drive responds by putting its complemented address on the bus. When the control unit reads the complemented drive address, 'address out' 7 is deactivated.

Note: If the address is not correct 'select out' is deactivated and the operation is ended. If the returned drive address was correct the control unit switches the bus to the send (write) mode and 'address in' 8 is deactivated.

With 'address out' not active the control unit activates 'command out' 9 to the drive by setting bit 2 of the DTR. The control unit decodes the command and puts it on the bus to the drive. After the command has been sent to the drive the bi-directional DCB is switched to receive (read) and the control unit waits for a response from the drive.

The drive places the first of two status bytes on the DCB and activates 'status in' 10 to the control unit by setting bit 6 of the DTR. The control unit accepts status byte 1 from the drive and requests the second status byte by activating 'clock A out' 11.

Note: The first status byte reports any error conditions that may exist (unit check) and the status of the drive (repositioning, performing a manual rewind unload and so forth).

The drive responds by placing status byte 2 on the bus to the control unit and activating 'clock B in' 12. The control unit accepts the second status byte and drops 'clock A out'.

Note: The second status byte pertains to the drive and tape cartridge (ready, at beginning-of-tape, at end-of-tape, or file protected).

When both status bytes have been accepted, the control unit resets 'command out' 13 and the drive resets 'status in' 14.

Select out remains on if:

- The command was a burst command.
- The command was a control type with data to be transferred.

Select out is reset if:

- A control command and no data is to be transferred.
- The command was an immediate command.
- The status byte contained unusual or unexpected information.

This ends the initial selection sequence to the drive. The drive is now ready for a data transfer operation.

Alert Sequence

An 'alert' sequence is started by the drive when:

- A disconnected sequence is complete
- The drive goes from 'not ready' to 'ready'
- Repositioning is complete
- A manual rewind unload is started
- Request processor microcode patches

Whenever the drive needs to communicate with the control unit, it sets an 'alert' bit in the drive device alert register (DAR) and also the control unit device interrupt register (DIR).

The DIR bit set corresponds to the drive sending the alert. If the remote connection is used, the register bit still corresponds to the drive sending the alert.

Once an 'alert' has been set in the control unit DIR the control unit must initiate an 'initial selection' sequence to the drive to clear the alert.

The control unit sets 'select out' in the device tag register and switches to send mode. The drive address is placed on the device control bus (DCB) and 'address out' is set into the DTR. The DCB is switched to receive mode and 'address in' is activated. The control unit waits for a response from the drive. When the address complemented is received, 'address out' is reset followed by 'address in'. The sequence continues as for an initial selection. The status bytes sent to the control unit at the end of the sequence contains the alert information. The drive alert is reset in the DIR and the control unit and drive are ready for the next operation. See the 'initial selection' sequence timing chart.

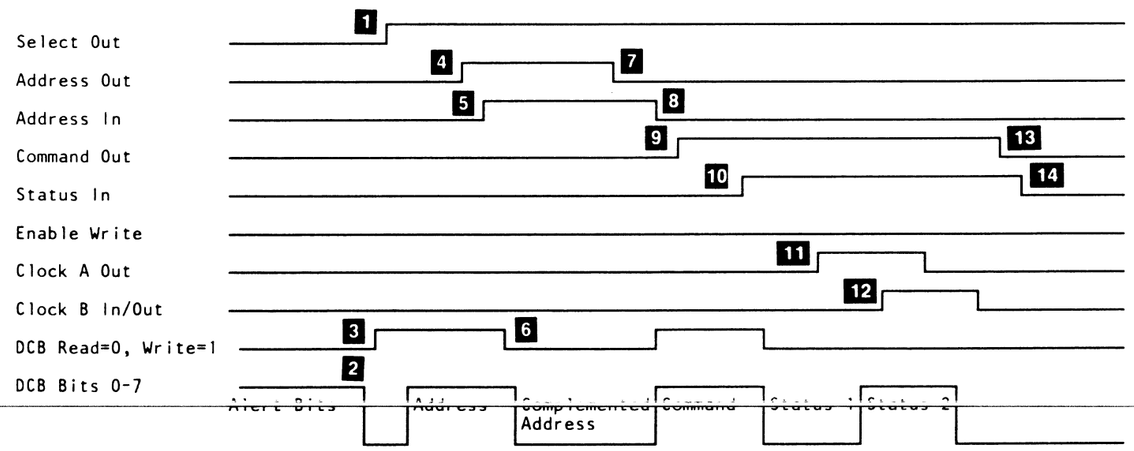


Figure 1. Control Unit to Drive Initial Selection Sequence

Control Unit To Drive Operation (Continued)

Ending Sequence (Control Unit Initiated)

An "ending sequence" (device stop) is used to disconnect the drive from the control unit. An "ending sequence" can be started by the control unit or the drive, except for a "data transfer sequence," which can only be ended by the control unit.

> **Note:** If 'address in' is active before the "ending sequence," and is inactive when 'command out' becomes active, it indicates a microcode detected error. If 'address in' becomes active while 'command out' is active, a hardware error is indicated (check 1).

The "ending sequence" for a data transfer starts when either 'write enable' (write operation) 1 or 'read gate' (read operation) is reset. The control unit checks for 'address in' 2 from the drive. If no errors are detected, the control unit activates 'command out' 3 to the drive.

'Address in' 4 is again checked for an indication of an error, by the control unit. The drive activates 'status in' 5 and the control unit checks for 'address in' 6 again (any errors). The drives status byte 1 7 is sent to the control unit across the device control bus (DCB). 'Address in' 10 is checked again (indicating errors) by the control unit.

'Clock A out' 8 is activated requesting status byte 2 from the drive and 'clock B in' 9 is activated verifying that status byte 2 11 has been sent to the control unit across the DCB. After the control unit receives status byte 2 'clock A out' 12 is deactivated and 'address in' 13 is checked once again. 'Clock B in' 14 is deactivated and 'status in' 15 is then deactivated indicating no more status bytes are to be sent.

Both status bytes from the drive have been received, and at this time 'select out' 16 is deactivated. 'Command out' 17 is deactivated stopping the drive, completing the ending sequence.

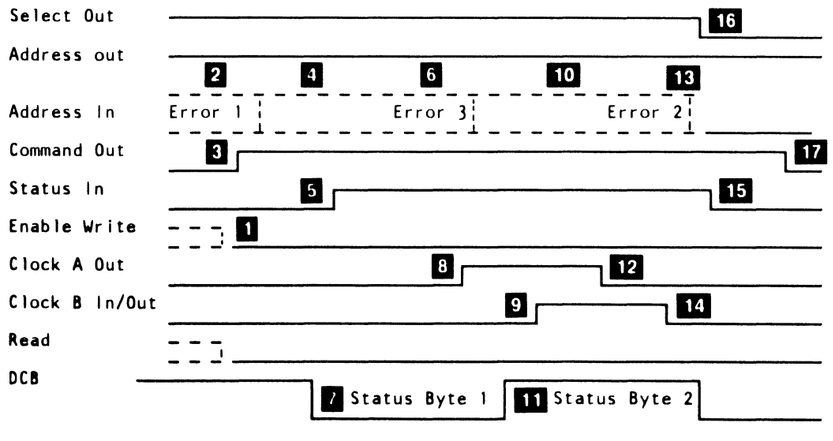


Figure 1. Ending Sequence (Device Stop)

Control Unit To Drive Operation (Continued) OPER 186

Control Unit To Drive Operation (Continued)

Write Operation

A write operation is started when the control unit sends a write command across the device control bus (DCB) to the drive. This starts tape motion and conditions the drive to write. After the tape has reached the correct speed and is at the correct place to start writing, the drive signals the control unit by activating the 'gap in' 1 line to the control unit. The write status/error register (WSE) bit 0 2 must be on to indicate to the drive that this is a write operation.

The write control register (WCR) 3 is set with the following:

- Bits 0 and 1 - Starting Block ID Sequence '00'
- Bit 5 - Write data flow operation enabled
- Bits 6 and 7 - Write data flow operation

At this time the interblock gap (IBG) 4, which is supplied by the control unit, is written. After the IBG has been written a check is made to ensure that the write operation 5 is still being performed by testing bit 0 of the WSE register. A check is made to ensure that the correct write control register (WCR) bits 6 were set by doing a compare. 'Gap out' 7 is a signal from the control unit indicating that the IBG has been recognized. The channel then starts sending data through the write data flow to the drive. As it is written the data is converted to the 3480 tape format.

When a data block 8 has been written a Block ID (sequence number) is added to the end of the data block, and a sequence count is set into the WCR for each block written. Both of these are recorded as part of the data record.

An 'end write' (write stop) 9 line (bit 1 of the WSE register) signals the end of each data record. This line is a result of a count of 'write request' signals from write data flow to the channel. The control unit can now issue a command to the write data flow that specifies either a new record is to be written or to stop writing. A new IBG is written in either case.

If a new record is to be written, set a Block ID number and advance the sequence number and reset the 'end write' (write stop) line. If the command is to stop writing because of the end of data, the drive is signaled to stop by the control unit.

1. Reset the WCR write data flow operation enable 10.
2. Reset end write (write stop) 11.
3. The WSE register bit 0 (write operation) should be off 12. If it is not, an error is indicated.

The drive slows down and comes to a stop. The tape moves backward to the write stoplock position, which is in front of the IBG. The drive assumes that the next command is another write-type operation. The drive is now in position for the next command.

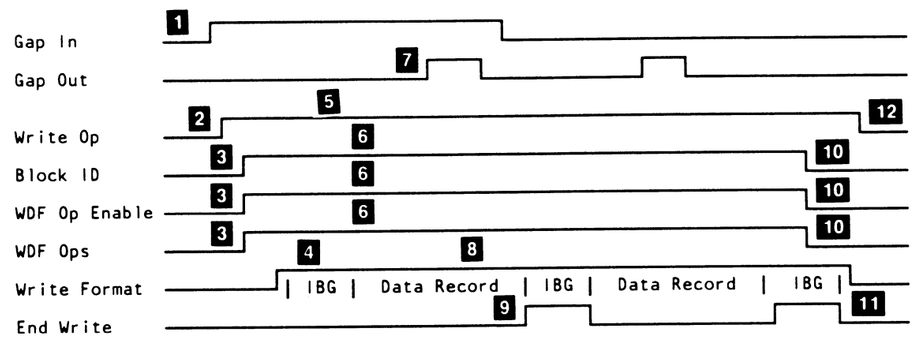


Figure 1. Write Operation

Serial Interconnection Sequence

The serial interconnection (using the device control bus) is used when the control unit is busy using the parallel interconnection on another drive.

The serial interconnection contains three signal lines:

- Repositioning In - is a line from all attached drives to the control unit. It indicates that the drive is repositioning or not at the stoplock position.
- Serial Clock Out - is a line from the control unit to all attached drives. It clocks the serial information to all drives. There are 18 serial clock out pulses. There is no response to this line.
- Serial Data Out - is a line from the control unit to all attached drives. It sends information to all nonselected drives together with 'serial clock out'. The 'serial clock out' gates the 'serial data out' line.

The serial interconnection saves time by getting another drive up to speed ('early start') while the parallel interconnection is in use with another drive using the parallel interconnection. (Only commands are sent across the serial interconnection.)

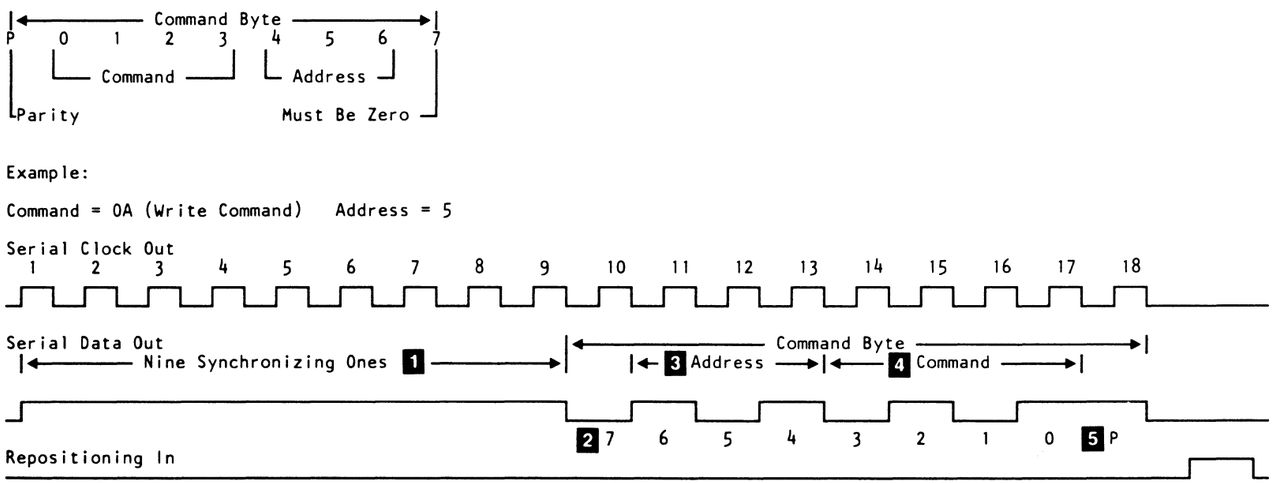


Figure 1. Serial Interconnection

Data is sent to the drive, serial by bit, as an 18 bit word that contains an address and command. No response is sent to the control unit from the drive unless the drive is repositioning. If the drive is repositioning, the 'repositioning in' line is activated to the control unit.

The serial command must be followed on the parallel interconnection with the same command before the drive is up to speed and has activated the 'gap in' line.

> **Note:** The initial selection sequence and the command must be completed over the parallel interconnection to the drive before 'gap in' is received at the control unit.

The parallel command is then executed from this point. If no parallel command is received by 'gap in' time, the drive goes to the serial stoplock position and waits for a parallel command.

There are seven serial interconnection commands.

- (06) Clamp
- (07) Unclamp
- (08) Reset A
- (02) Read Forward
- (03) Read Backward
- (0A) Write
- (00) Test I/O

The Clamp, Unclamp, and Reset A commands are issued when the drive is suspected of not operating correctly. The Read Forward, Read Backward, and Write commands are issued to cause tape movement.

When the serial command is received, and the drive is not at the correct stoplock, the drive repositions to the correct stoplock for the serial command just received and then sends an 'alert' to the control unit.

The Test I/O command causes hardware to gate the status on the 'repositioning in' tag line.

Serial Format

The serial command is a string of 18 data bits with 18 associated clock pulses.

The format is as follows:

1. At least nine logical '1's' in a row (preamble) **1**.
2. Followed by one logical '0' **2**.
3. The three drive address bits (low order first) **3**.
4. The four command bits (low order first) **4**.
5. One parity bit associated with steps 2, 3, and 4. **5**.

If the correct preamble is not received by the serial interconnection, no serial command is decoded.

The control unit must communicate with both the channel of the host system and with each of the tape units of the subsystem. A method for this communication is supplied by two I/O connections, channel to the control unit and control unit to the drive. See the diagram on the following page.

The basic timing sequence of the interface is found in *IBM System/360 and System/370 Interface Channel to Control Unit Original Equipment Manufacturers Information Manual,* GA22-6974.

Channel to Control Unit Interface

Bus Out

There are eight information lines plus one parity line on 'bus out'. Bus out is used to send a control unit address, device address, commands, and data to the control unit from the channel.

Bus In

There are eight information lines plus one parity line on 'bus in'. Bus in is used to send a control unit address, device address, status information, sense information, and data to the channel from the control unit.

Operational Out

The 'operational out' tag is a line from the channel that connects the control unit to the channel. When 'operational out' is deactivated, the existing operation across the interface must be reset.

Address Out

'Address out' is a tag line from the channel to the control unit. It is used to signal the control unit to decode the control unit and device address sent on bus out. The control unit then must activate 'operational in' to the channel.

Hold Out

'Hold out' is a line from the channel to the attached control unit and is used with 'select out' to synchronize control unit selection.

Select Out

'Select out' is a line from the channel to the control unit and, together with 'select in', supplies a loop for scanning the attached control unit. A control unit can activate 'operational in' to the channel only when 'select out' is sent to the control unit.

Command Out

'Command out' is a line from the channel to the attached control unit and is used to signal the selected device in response to 'address in', 'status in', or 'service in' from the control unit.

Service Out

'Service out' is a tag line from the channel to the control unit and is a response to 'status in' or 'service in'. It indicates to the control unit that the channel has received information sent on 'bus in' or has supplied (on bus out) the data requested by 'service in'.

Data Out

'Data out' is a tag line from the channel to the control unit and is used in response to a signal on 'data in'. A signal on 'data out' indicates the channel has received the information on 'bus in' or has supplied (on bus out) the data requested by 'data in'.

Suppress Out

'Suppress out' is a line sent from the channel to the control unit and is used alone or together with other out tags to supply the signal to suppress data, suppress status, do command chaining, or a selective reset.

Select In

'Select in' is a line that extends 'select out' from the from the channel to the control unit and is returned to the channel as 'select in'. 'Select in' is only returned to the channel if no device address has been decoded.

Operational In

'Operational in' is a line from the control unit to the channel and is used to signal the channel that the device has been selected. It must remain active for the complete time of the selection.

Address In

'Address in' is a line from the control unit to the channel and is used to signal the channel that the addresses of the control unit and the selected device have been placed on 'channel bus in' (CBI).

Status In

'Status in' is a line from the control unit to the channel and is used to signal the channel that the selected control unit has placed status information on CBI.

Service In

'Service in' is a tag line from the control unit to the channel and is used to signal the channel when the selected device is ready to send or receive a byte of data. 'Service in' on a read operation validates data on 'bus in', and on a write operation acknowledges receipt of data on 'bus out'.

Meter In

'Meter in' is a line from the control unit to the channel and is used to enable the subsystem after status has been cleared. At the end of the operation being executed, 'meter in' is deactivated, status is cleared, and the subsystem is disabled.

Data In

'Data in' is a tag line from the control unit to the channel and is used to signal the channel that the selected control unit has a byte of information for the channel.

Request In

'Request in' is a line from the control unit to the channel and indicates the control unit is ready to present status information or data, and is therefore requesting a selection sequence.

Disconnect In

'Disconnect in' is a line from the control unit and permits the control unit to signal the system of a failure that could prevent the control unit from signaling correctly over the interface.

Mark In

Used in a command-retry sequence. If during the execution of a command, the control unit finds a condition that requires a retry, the control unit requests command retry by activating 'mark 0 in' and 'status in' while sending a unit check and status modifier together with channel end and/or device end to the host system. The channel acknowledges the request for command retry by indicating command chaining.

Mark Out

'Mark out' is only used with the "Bus Extension Feature." This feature extends the interface by adding an extra bus to permit data transfer of either one or two bytes in parallel. During the transfer of data between the channel and the control unit, the 'mark out' lines must be valid the same time as the data on the 'bus out' lines and indicates the number of bytes provided by the channel on 'bus out'.

Control Unit to Drive Interconnection

Select Out

'Select out' is a line from the control unit to the drive. Whenever 'select out' is inactive, all lines from the drive to the control unit must be inactive, except for the device control bus (DCB) when sending **alerts** to the control unit. Any operation on the interconnection must be reset, except that operations at the device continue to a normal stopping point.

Address Out

'Address out' is a line from the control unit to all attached drives. The address of the needed drive is placed on the DCB, following the activating of 'select out', signaling all drives to decode the address. 'Address in' is deactivated after the complemented drive address has been returned to the control unit.

Address In

'Address in' is a line from all attached drives to the control unit. It is the response to 'address out' to signal the control unit that the complemented drive address is correct on the DCB. 'Address in' remains active until 'address out' is deactivated.

'Address in' is used after the above sequence to indicate any error or unusual condition that occurs before the ending 'status in'.

When 'address in' becomes active in response to 'command out' it means a drive hardware error.

I/O Interface (Continued) OPER 196

Command Out

'Command out' is a line from the control unit to all attached drives. The command must be correct on the DCB before 'command out' is activated. It is a response to 'address in' going inactive during initial selection and indicates to the selected drive that the command is correct on the DCB. 'Command out' remains active until 'status in' is received.

When used during a data transfer sequence, data transfer stops, and there is no information on the DCB associated with the tag. 'Status in' is activated in response.

Status In

'Status in' is a line from all attached drives to the control unit. It verifies the first status byte and remains active for both status byte 1 and status byte 2. Status byte 2 is requested when the control unit activates 'clock A out' and is verified by the drive activating 'clock B in'.

During the initial selection sequence, 'status in' is in response to 'command out' going active and goes inactive after 'command out' is deactivated.

Repositioning In

'Repositioning in' is a line from all attached drives to the control unit. It indicates that the drive is repositioning or not at a stoplock position. The 'repositioning in' response occurs after the command byte is received.

Gap In/Out

'Gap in/out' is a bi-directional line between the control unit and all drives. The line is used by the control unit (gap out) and the selected device (gap in) during data transfer sequence to indicate the relative position of the tape and the read/write head.

Clock A Out

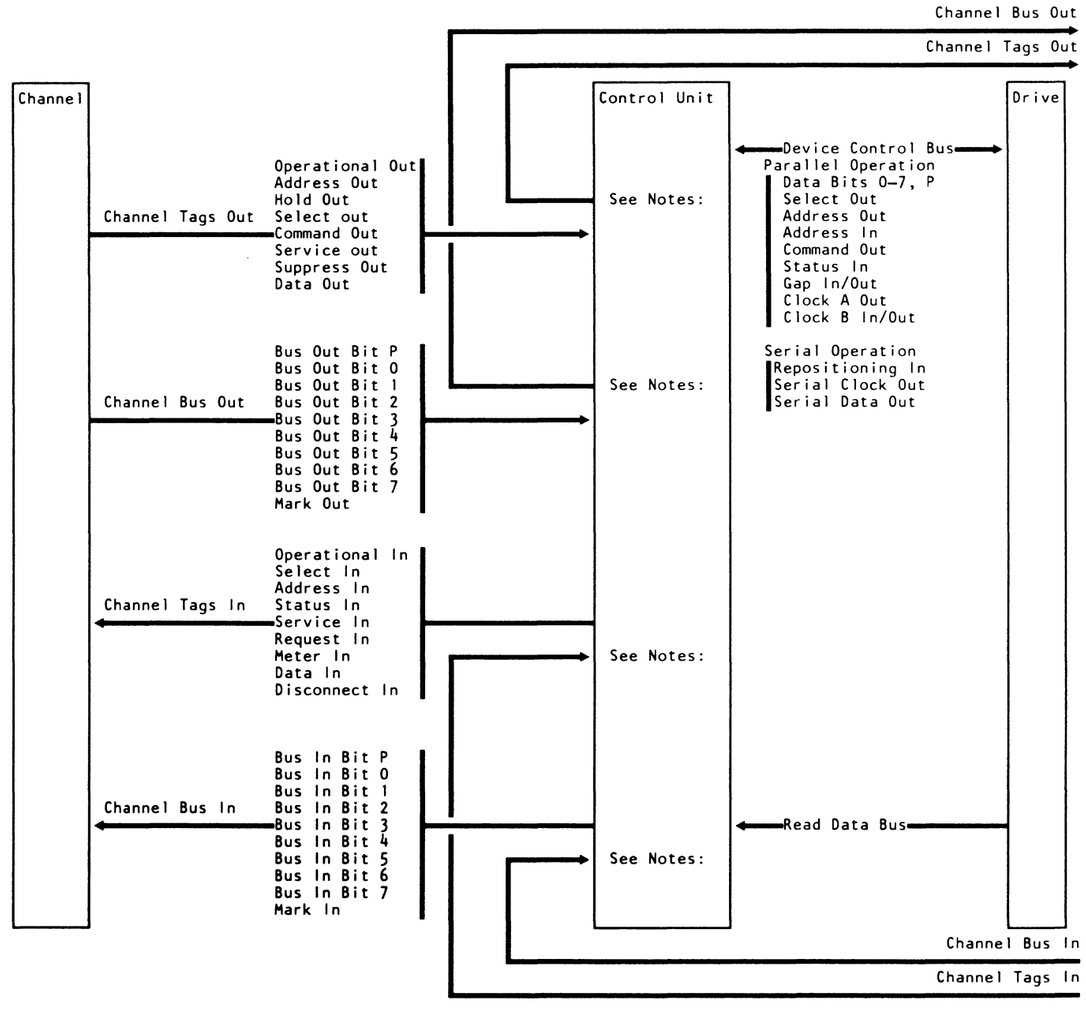
'Clock A out' is a line from the control unit to all attached drives and is activated when the control unit requests the second status byte from the drive.

Clock B In/Out

'Clock B in/out' is a bi-directional line between the control unit and all attached drives. These lines are used during a data transfer, control transfer, sense transfer, and a status 2 transfer sequence.

Notes:

1. The bus and tag terminators are installed on the **last** control unit during installation.
2. There can be from one to four channels for each control unit or from one to eight channels for a two control unit subsystem.



I/O Interface (Continued) OPER 196

Microprocessor to Channel Adapter Operation

This is a list of acronyms that are used extensively in the explanation of the microprocessor to channel adapter operation.

```
MP - Microprocessor
SS - Status Store
CA - Channel Adapter
RAM - Random Access Memory
CCC - Channel Card Control
CDR - Channel Data Register
CCA - Channel Card Address
CRR - Channel Response Register
CER - Channel Error Register
XR - External Register
CDTI - Channel Diagnostic Tag In
Register
CTO - Channel Tag Out
```

Communication between the MP and the CA is accomplished through the SS. The MP sends orders to XRs in SS, which are sent on to the CA.

The adapter and device address, or 'RAM' offset, are sent through the CCC register. Any data sent or received is through the CDR. The actual order and RAM page number is sent through the CCA register. Writing the CCA register causes the order, address, and data to be sent to the CA. When the order is completed, the CA returns any data requested through the CDR register. Also, a response is returned and loaded into the CRR.

The MP monitors CCR bit 6 (order complete) and CCR bit 7 (order successful) to determine the results of the order sent. Errors are set in the CER.

Note: Some of the external registers in the SS are read only, write only, or both.

MP to SS Communications

The MP to SS communication is through the normal external register path.

Major functional lines include the following:

- XR ADR EXT Bits 0 and 1 - set from the processor control register bits 6 and 7.
- XR ADR Bus Bits P, 0-4 - bits 0-4 are set from the five bits on the control storage data bus that corresponds to the XR address in the instruction. The 'P' bit is generated to maintain even parity on this bus.
- XR Data Bus P, 0-7 - a bi-directional bus for read or write data.
- XR Read Gate - active at S18-S21 time for XR read.
- XR Write Gate - active at S0-S13 time for XR write.
- XR Load - active at S5-S7 time. If XR write gate is on, the addressed register is loaded with the data on the XR data bus. This signal is generated by the control store card and always occurs. No writing occurs unless the write gate is also on.

SS to CA Communications

SS to CA communications is accomplished by a polling sequence. SS polls each CA in sequence. A poll operation has four conditions, S0-S3, determined by the binary bits 1 and 2.

If SS receives an order from the MP for the CA, the order and address is sent during S0 time, also data if required, is sent or received during S2 time. If the CA has an order for SS to process, it sends the order to SS during S1 time, and SS responds during S3 time.

SS to CA path includes the following functional major lines:

- Select Bus 0-3 - bits 0 through 3 select channel adapters A through D.
- Data Bus P, 0-7 - bi-directional bus for read, write, or control data.
- Response Bus P, 0-3 - bi-directional bus for control or response data. When the response bus contains response data it is defined as follows.

  During S2 time (SS execution of a MP order)

  - Bit 0 - adapter installed
  - bit 1 - adapter installed
  - Bit 2 - order complete
  - Bit 3 - order successful

  During S3 time (SS execution of a CA order)

  - Bit 0 - response valid
  - Bit 1 - no errors detected
  - Bit 2 - adapter permitted
  - Bit 3 - assign successful
- Order State - active when SS external register 01 (CCA) has been set with an MP order for the channel adapter.
- Binary State Bit 1 and 2 - decode of these lines determines S0-S3 times.

MP to SS to CA Communication

EXAMPLE:

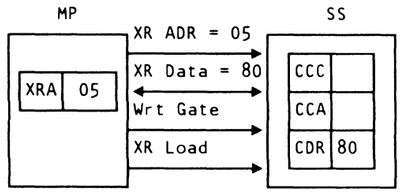
Assume that the MP is running the channel wrap test EE62, and wants to activate the 'operational in' tag line, and also check that it wraps to the 'operational out' tag line. This is accomplished by the following operation.

1. The MP sends a CA order and the required data to SS to activate the 'operational in' bit in the CDTI register.
2. On the next poll, SS sends the order and data to the CA which activates the 'operational in' bit in the CDTI. With the wrap blocks installed, 'operational in' is wrapped to 'operational out'.
3. Because the CTO register is a status register external to the RAM, the MP must first write the CTO into the RAM position assigned to this register. Later it can be read out to determine if the 'operational in' bit is on. Therefore, the MP sends a CA order to SS to write the CTO into the RAM.
4. On the next poll SS sends the order to the CA, and the CTO is written into the RAM.
5. The MP now sends the necessary order to SS to read the RAM location just written.
6. On the next poll SS sends the order on to the CA which reads the assigned RAM location and sends the data back to SS where it is loaded into the CDR.
7. The MP checks the results in the CDR with a normal XR read to SS.

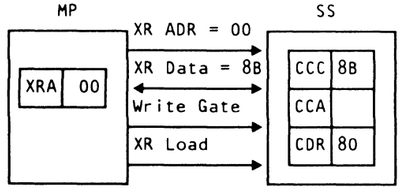
MP to SS Operation (Set CDTI Bit 0 On)

The following three diagrams relates to Step 1 of the EXAMPLE.

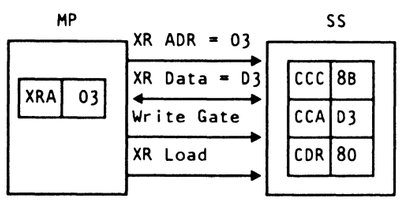
- MP sets CDR register to X'80'.
  1. Gate X'05' to the XR address bus.
  2. Gate X'80' to the XR data bus.
  3. Activate the write gate and XR load.



- MP sets CCC to X'8B'.
  1. Gate X'00' to the XR address bus.
  2. Gate X'8B'to the XR data bus.
  3. Activate the write gate and XR load.



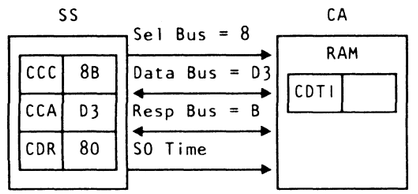
- MP sets CCA to X'03'.
  1. Gate X'03' to the XR address bus.
  2. Gate X'D3' to the XR data bus.
  3. Activate the write gate and XR load.



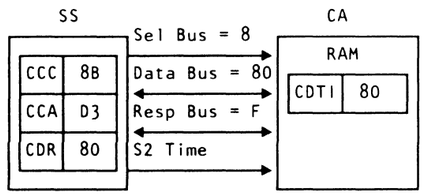
SS to CA Operation (Set CDTI Bit 0 On)

The following two diagrams relate to Step 2 of the EXAMPLE.

- Status store polls at S0 time.
  1. Gate CCA register to the data bus (MP order and RAM page number).
  2. Gate CCC register bits 0-3 to the select bus (channel adapter address).
  3. Gate CCC register bits 4-7 to the response bus (page offset).



- Status store poll at S2 time.
  1. Gate CDR register to the data bus.
  2. CA write data into RAM page 3, offset B (CDTI).
  3. CA sets response bus to X'F' (order complete and successful).



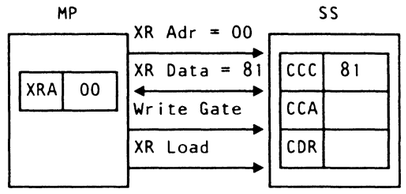
The CDTI register bits are:

Bit 0 Operational In
Bit 1 Address In
Bit 2 Select In
Bit 3 Request In
Bit 4 Status In
Bit 5 Service In
Bit 6 Data In
Bit 7 Disconnect In

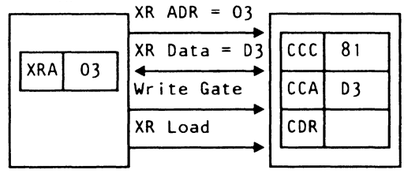
MP to SS Operation (Write CTO into RAM)

The following two diagrams relate to Step 3 of the EXAMPLE.

- MP sets CCC register to X'81'.
  1. Gate X'00' to the XR address bus.
  2. Gate X'81' to the XR data bus
  3. Activate the write gate and XR load.



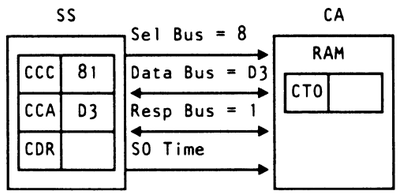
- MP sets the CCA register to X'D3'.
  1. Gate X'03' to the XR address bus.
  2. Gate X'D3' to the XR data bus.
  3. Activate the write gate and the XR load.



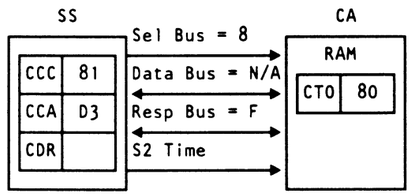
SS to CA Operation (Write CTO into RAM)

The following two diagrams relate to Step 4 of the EXAMPLE on OPER 205.

- Status store poll at S0 time.
  1. Gate the CCA register to the data bus (MP order and RAM page number).
  2. Gate the CCC register bits 0-3 to the select bus (Channel Adapter Address).
  3. Gate the CCC register bits 4-7 to the response bus (Page Offset).



- Status store poll at S2 time.
  1. CA writes CTO register into RAM page 3, offset 1 (CTO).
  2. CA sets response bus to X'F' (order complete and successful).



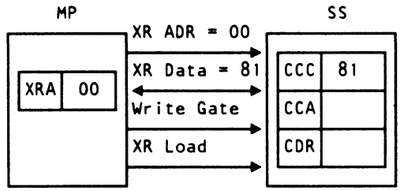
The CTO register bits are:

Bit 0 Operational Out
Bit 1 Address Out
Bit 2 Select Out
Bit 3 Hold Out
Bit 4 Command Out
Bit 5 Service Out
Bit 6 Data Out
Bit 7 Suppress Out

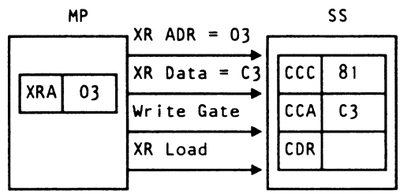
MP to SS Operation (Read RAM CTO location)

The following two diagrams relate to Step 5 of the EXAMPLE on OPER 205.

- MP sets CCC register to X'81'
  1. Gate X'00' to the XR address bus.
  2. Gate X'81' to the data bus.
  3. Activate the write gate and XR load.



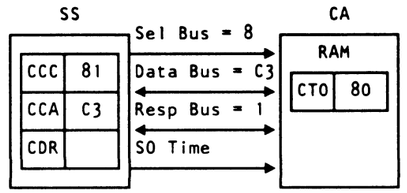
- MP sets CCA to X'C3'.
  1. Gate X'03'to the XR address bus.
  2. Gate X'C3'to the XR data bus.
  3. Activate the write gate and XR load.



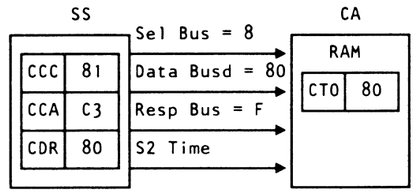
SS to MP Operation (Read RAM CTO location)

The following two diagrams relate to Step 6 of the EXAMPLE on OPER 205.

- Status store poll at S0 time.
  1. Gate CCA register to the data bus (MP order and RAM page number).
  2. Gate CCC register bits 0-3 to select bus (CA address).
  3. Gate CCC register bits 4-7 to response bus (page offset).



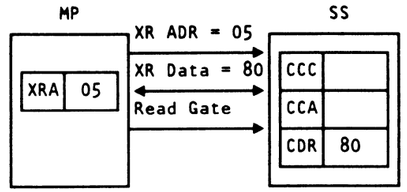
- Status store poll at S2 time.
  1. CA gates RAM data X'80' to the data bus.
  2. SS writes data to the CDR.
  3. CA sets response bus to X'F' (operation complete and successful).



MP External Register Read (Read Data into CDR)

The following diagram relates to Step 7 of the EXAMPLE on OPER 205.

- MP reads CDR register in status store
  1. Gate X'05'to the XR address bus.
  2. Activate the read gate.
  3. SS gates the CDR register X'80'to the XR data bus.



MP to SS to CA Data Flow

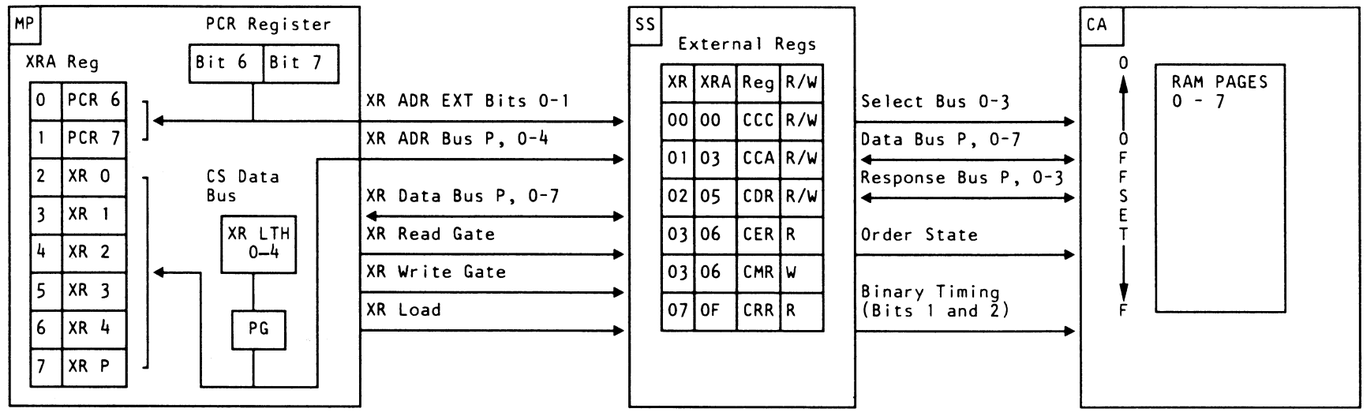


Figure 1. Microprocessor To Channel Adapter Data Flow

XRA Decode

The following is an example of XRA decoding, using status store external register 02.

0	1	2	3	4	5	6	7
EXT 0	EXT 1	ADR 0	ADR 1	ADR 2	ADR 3	ADR 4	ADR P
0	0	0	0	0	1	0	1

Status store is selected by bits 0 and 1 set to 00.

Bits 2 through 7 are set to a binary value of the external register with even parity.

The result is XRA = X'05'

Channel Card Control Register

The following is the layout of the channel card control register.

CCC Register XRA Register = 00

0	1	2	3	4	5	6	7
CA A	CA B	CA C	CA D	Page Offset			

Channel Card Address Register

The following is the layout of the channel card address register.

CCA Register XRA Register = 03

0	1	2	3	4	5	6	7
MP Order				RAM Page			

Channel Data Register

The following is the layout of the channel data register.

CDR XRA Register = 05

0	1	2	3	4	5	6	7
RAM Read/Write Data							

Status registers external to the RAM. In order to inspect, write into RAM, and read the RAM.

Control Registers external to the RAM. Write to the RAM writes into the register and RAM.

Off-set	RAM PAGE 3
0	CBO-Channel Bus Out
1	CTO-Channel Tag Out
2	CBI-Channel Bus In
3	CTI-1-Channel Tag In 1
4	CTI-2-Channel Tag In 2
5	CAE-Channel Adapter Error
6	CAS-Channel Adapter Status
7	Unused
8	CDBO-Channel Diagnostic Bus Out
9	CDTO-Channel Diagnostic Tag Out
A	CDBI-Channel Diagnostic Bus In
B	CDTI-Channel Diagnostic Tag In
C	CDC-Channel Diagnostic Control
D	Unused
E	Unused
F	CIR-Channel Interrupt Request

IML Diskette Drive OPER 220

IML Diskette Drive Operation

The initial microprogram load (IML) diskette drive is either a 5.25 inch or a 3.5 inch disk drive. The 5.25 inch drive provides 500 kilobytes of unformated storage on a double density, double sided, flexible diskette. The 3.5 inch disk drive provides 1 megabyte of unformatted storage on a double sided diskette. The purpose of the diskette drive is to IML the fuctional microcode for the 3480 subsystem.

The IML is accomplished during a 3480 power on, or by pressing the IML switch when the control unit Test/Normal switch is in the Normal position and the control unit Online/Offline switch is offline.

The IML sequence of operation is as follows:

1. Run the programmable read only memory (PROM) diagnostics to test the 128 kilobytes of control storage. Error information is stored in a microcode table for later use by the functional microcode and the maintenance diskette.

2. Start the IML diskette drive to load IML diagnostics into control storage and run the diagnostics. The IML diagnostics check out the control unit.

   Note: All errors are placed in a microcode table but, severe (CHK 1) errors cause 'disconnect in' and the control unit stops.

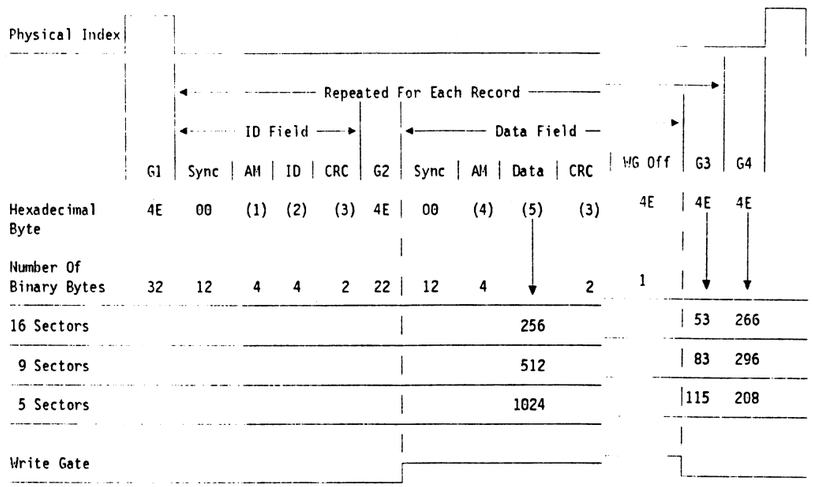
   Errors other than CHK 1 errors cause the control unit to respond with a unit check to the next 'Start I/O' command from the host system.

3. Load the functional microcode to start a normal operation. The maintenance diskette looks at the microcode table for any error information.

4. If you are installing a subsystem the IML diskette is used to load installation diagnostics. You must place the Test/Normal switch in the Test position to run the installation diagnostics.

   Note: When the Normal/Test switch is in the Test position the installation diagnostics are run before the start of normal operations.

Modified frequency modulation (MFM) is a function of the control units control storage card and the recording format is in the MFM format. See Figure 1. The inter-sector gaps are shown as G1, G2, G3, and G4.



Notes: (1) ID Address Mark With Missing Clock
(2) Cylinder Number, Head Number, Sector Number, and Physical Record Length
(3) Generated by CRC Generator.
(4) Data Address Mark With Missing Clock
Deleted Data Address Mark With Missing Clock
(5) Users Data

Figure 1. MFM Sectored Format

0 0 0 0 0 0 0 0 0 0

IML Diskette Drive Operation

The initial microprogram load (IML) diskette drive is a 13.34 centimeter (5.25 inch) flexible disk drive. The IML Diskette drive provides unformatted storage of 500 kilobytes on a double density two-sided flexible diskette. Its purpose is to IML the functional microcode for the 3480 subsystem.

The IML is accomplished during a 3480 power on, or by pressing the IML switch when the control unit Test/Normal switch is in the Normal position and the control unit Online/Offline switch is offline.

The IML sequence of operation is as follows:

1. Run the programmable read only memory (PROM) diagnostics to test the 128 kilobytes of control storage. Error information is stored in a microcode table for later use by the functional microcode and the maintenance diskette.

2. Start the IML diskette drive to load IML diagnostics into control storage and run the diagnostics. The IML diagnostics check out the control unit.

   Note: All errors are placed in a microcode table but, severe (CHK 1) errors cause 'disconnect in' and the control unit stops.

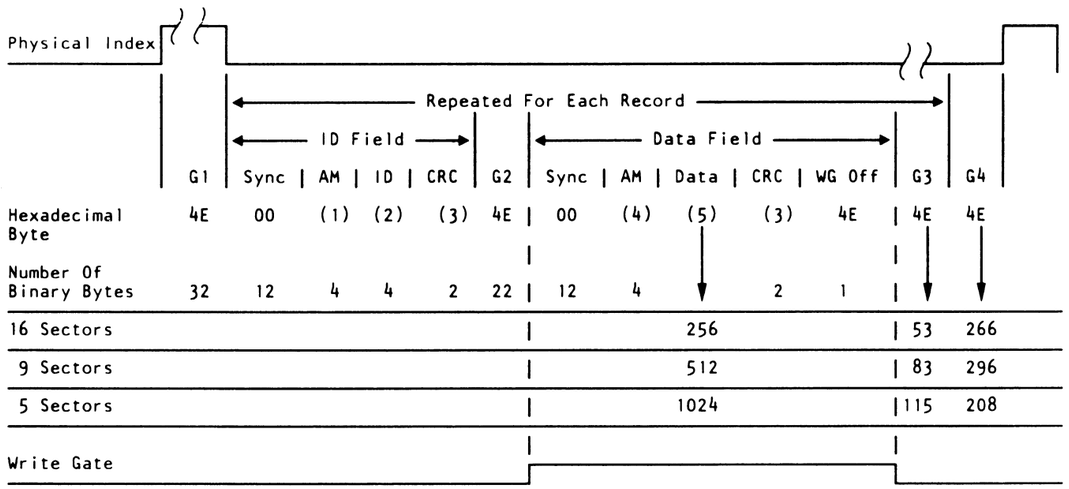
   Errors other than CHK 1 errors cause the control unit to respond with a unit check to the next 'start I/O' command from the host system.

3. Load the functional microcode to start a normal operation. The maintenance diskette looks at the microcode table for any error information.

4. If you are installing a subsystem the IML diskette is used to load installation diagnostics. You must place the Test/Normal switch in the Test position to run the installation diagnostics.

   Note: When the Normal/Test switch is in the Test position the installation diagnostics are run before the start of normal operations.

Modified Frequency Modulation (MFM) is a function of the control units control storage card and the recording format is in the MFM format. See Figure 1. The inter-sector gaps are shown as G1, G2, G3, and G4.



Notes: (1) ID Address Mark With Missing Clock
(2) Cylinder Number, Head Number, Sector Number, and Physical Record Length
(3) Generated by CRC Generator.
(4) Data Address Mark With Missing Clock
Deleted Data Address Mark With Missing Clock
(5) Users Data

Figure 1. MFM Sectored Format

Control Storage To Drive Interconnections

The IML diskette drive has two connectors. Connector P1/J1 connects the digital I/O signals, and connector P2/J2 connects the +5 V dc and the +12 V dc. The interconnections second level diagram in Figure 1 identifies the pin assignments for these connectors.

Figure 2 is a timing chart showing the signal lines and their relationship.

Drive Select 0 To Disk

An active level on the 'drive select to disk' (DS0) line (pin E of the J1 connector) permits communication between the individual drive and the control storage card.

The drive select address is selected by a pluggable jumper. The DS0 jumper is installed at the plant and must be inserted in the DS0 position for correct operation. When the two DS0 jumper pins are shorted, the IML drive is activated by an active signal on the 'drive select to disk' line.

Motor On To Disk

An active level on pin J of the J1 connector enables the drive motor. One-half second is required after 'motor on' is activated for the spindle to come up to speed before reading or writing on the diskette is permitted. Pin J is deactivated for maximum motor life if no commands are issued to the drive within two seconds (10 media revolutions) after completion of a preceding command.

Direction Select To Disk

'Direction select' (pin K of the J1 connector) defines the direction of the read/write head. An active level on this line causes the head positioning mechanism to move the read/write head toward the center of the diskette when the 'step' line becomes active.

When the 'direction select' line is not active, the 'step' line causes the head positioning mechanism to move the read/write head away from the center of the diskette.

Step To Disk

When the 'step' line is active on pin L of the J1 connector the read/write head is moved one track. The direction is controlled by the 'direction select' line.

Write Data To Disk

The data that is written on the diskette is sent on pin M of the J1 connector. Each transition on pin M from not active to active causes the write current direction through the write head to be reversed.

Write Gate To Disk

An active level on pin N of the J1 connector enables the write current, and disables the stepping (head positioning) circuits. With pin N not active, the read circuits are enabled..

Side Select To Disk

The 'side select' line (pin T of the J1 connector) defines which surface of a two-sided diskette is to be accessed for writing or reading data. An active level on pin T selects the read/write head for diskette side 1 (the side facing the printed circuit board). With pin T not active, side 0 (the diskette side facing the disk drive chassis) of the diskette is selected. When switching from side to side, a 100 microsecond delay is provided before any read or write operation can be performed.

Drive to Control Storage Interconnections

Index From Disk

This signal on pin D of the J1 connector is provided by the drive once each diskette revolution. The leading (negative going) edge of the Index pulse indicates to the control unit the beginning of a track.

Track 00 From Disk

When pin P of the J1 connector is active it indicates that the read/write head is positioned at track 00.

Write Protect From Disk

This line is not used:

Note: IML diskettes can be written on when file protected.

Read Data From Disk

Data on pin S of the J1 connector is read from the diskette to the host system in the same form as when it was written on the diskette.

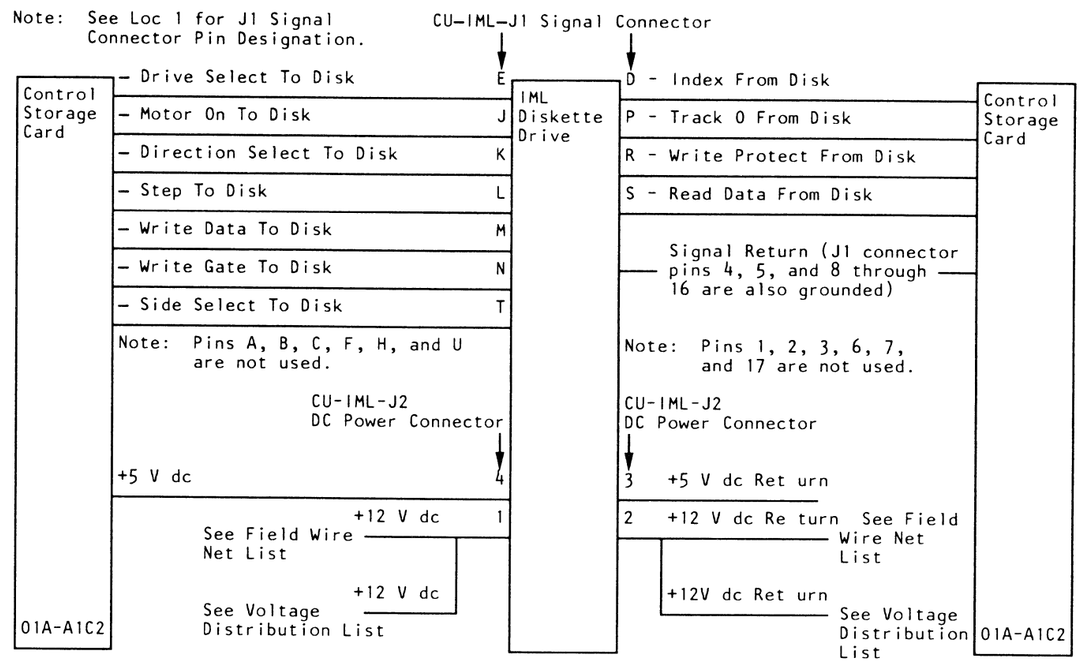


Figure 1. Control Storage To/From IML Diskette Drive

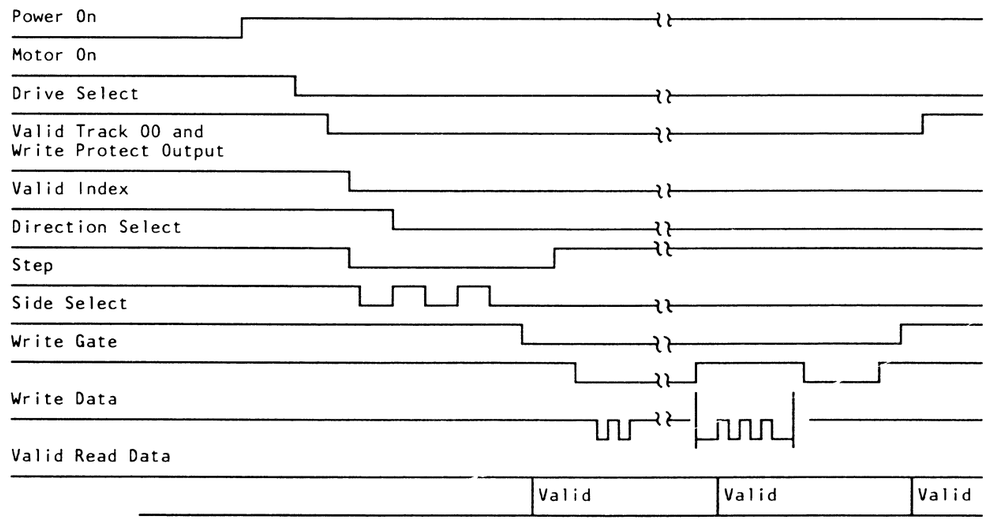


Figure 2. Controls and Data Timing Chart

Control Storage To Drive Interconnections

The IML diskette drive has two connectors. Connector P1/J1 connects the digital I/O signals, and connector P2/J2 connects the + 5 V dc and the + 12 V dc. The interconnections second level diagram in Figure 1 identifies the pin assignments for these connectors.

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Drive Select 0 To Disk

An active level on the 'drive select to disk' (DS0) line (pin E of the J1 connector) permits communication between the individual drive and the control storage card.

The drive select address is selected by a pluggable jumper. The DS0 jumper is installed at the plant and must be inserted in the DS0 position for correct operation. When the two DS0 jumper pins are shorted, the IML drive is activated by an active signal on the 'drive select to disk' line.

Motor On To Disk

An active level on pin J of the J1 connector enables the drive motor. One-half second is required after 'motor on' is activated for the spindle to come up to speed before reading or writing on the diskette is permitted. Pin J is deactivated for maximum motor life if no commands are issued to the drive within two seconds (10 media revolutions) after completion of a preceding command.

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When the 'direction select' line is not active, the 'step' line causes the head positioning mechanism to move the read/write head away from the center of the diskette.

Step To Disk

When the 'step' line is active on pin L of the J1 connector the read/write head is moved one track. The direction is controlled by the 'direction select' line.

Write Data To Disk

The data that is written on the diskette is sent on pin M of the J1 connector. Each transition on pin M from not active to active causes the write current direction through the write head to be reversed.

Write Gate To Disk

An active level on pin N of the J1 connector enables the write current, and disables the stepping (head positioning) circuits. With pin N not active, the read circuits are enabled..

Side Select To Disk

The 'side select' line (pin T of the J1 connector) defines which surface of a two-sided diskette is to be accessed for writing or reading data. An active level on pin T selects the read/write head for diskette side 1 (the side facing the printed circuit board). With pin T not active, side 0 (the diskette side facing the disk drive chassis) of the diskette is selected. When switching from side to side, a 100 microsecond delay is provided before any read or write operation can be performed.

Drive to Control Storage Interconnections

Index From Disk

This signal on pin D of the J1 connector is provided by the drive once each diskette revolution. The leading (negative going) edge of the Index pulse indicates to the control unit the beginning of a track.

Track 00 From Disk

When pin P of the J1 connector is active it indicates that the read/write head is positioned at track 00.

Write Protect From Disk

Diskettes that are write protected will cause an error during Power On and IML.

Read Data From Disk

Data on pin S of the J1 connector is read from the diskette to the host system in the same form as when it was written on the diskette.

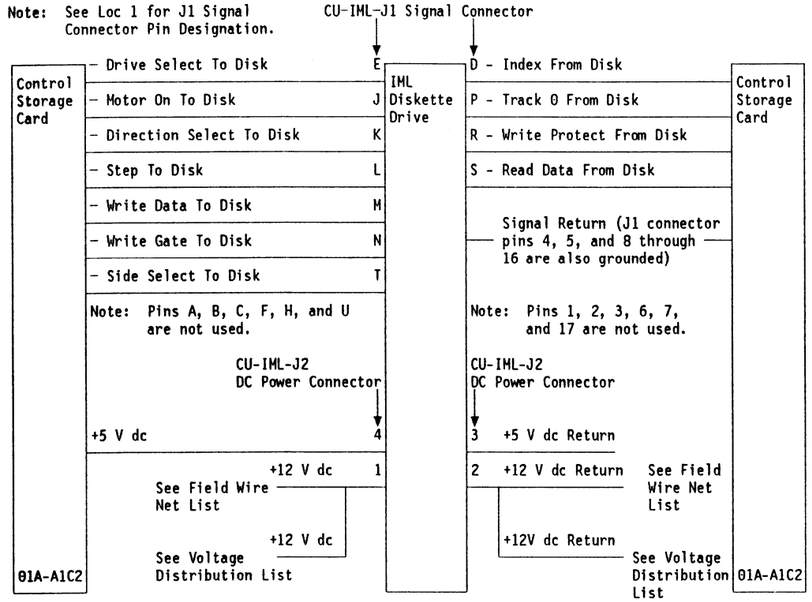

Figure 1. Control Storage To/From IML Diskette Drive

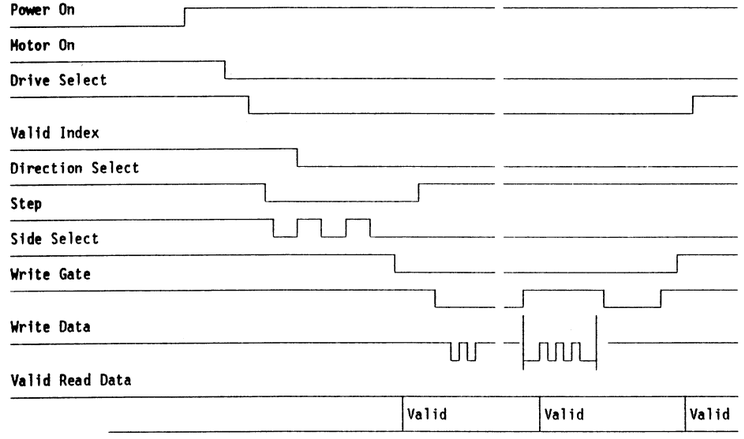

Figure 2. Controls and Data Timing Chart

0 0 0 0 0 0 0 0 0 0

Automatic Cartridge Loader

The diagram shows the functional areas of the automatic cartridge loader. This topic explains the purpose of the functional areas. A brief description of the functional areas is included.

- Loader Operator Panel
- Loader Control Card
- Loader Mechanical Assembly
- Load Assembly.

The Loader Operator Panel Consists Of:

- Mode Selection Switch
- Start Switch
- Attention Indicator
- Power Indicator.

Mode Selection Switch

The mode selection switch has three positions and can be changed at any time by the operator. Generally, the device will switch to the new mode automatically, without any other operator action. The exception is switching to auto mode. The start switch must be depressed to activate the new mode.

Automatic Mode

In this mode, cartridges in the input stack will be sequentially loaded into the drive, and upon completion of use by the drive, will be unloaded and positioned in the output stack.

Manual Mode

In this mode, cartridges are manually inserted into any position of the input station by the operator. When the drive unloads, the cartridge will remain at the feed station.

System Mode

This mode incorporates the attributes of both the automatic and manual modes. This mode is valid only on MVS systems (the ones that support the "Load Display" Command). Any other system will not allow the automatic cartridge loader to operate in this mode.

Start Switch

This switch is used to initialize auto or system mode, reinitialize auto or system mode, or to activate each manual load cycle. The start switch is also used to remove a cartridge from the feed station when the attention indicator is flashing and a cartridge is in the 3480.

Attention Indicator

When flashing, it indicates an operator action is required. The operator should remove the cartridge from the output stack or press the automatic cartridge loader start switch to clear the attention condition. When on solid, it indicates an error condition exists. If in a recovery mode and the light is on solid, press the drive unload switch to clear the solid attention light on the automatic cartridge loader.

Power Indicator

Indicates when DC power is on at the automatic cartridge loader.

Loader Control Card

This card contains the microprocessor, drivers, memory and interfaces to the sensors, motors, automatic loader operator panel and tape drive. After getting an IML load from the CU by way of the tape drive, the card will control all the motions of the automatic cartridge loader.

Loader Mechanical Assembly

This assembly contains all the components required to hold, load, unload and stack cartridges. The assembly consists of these major components:

- Input Stack Assembly
- Feed Assembly
- Output Stack Assembly.

Input Stack Assembly

The input stack assembly holds the cartridges and moves them into position to be fed into the 3480.

Feed Assembly

The feed assembly feeds the cartridge into the load assembly or removes the cartridge from the load assembly and moves it to the output stack assembly.

Output Stack Assembly

The output stack assembly receives the cartridge from the feed assembly and stacks it for later operator removal.

Load Assembly

The load assembly consists of all the parts required to position the tape cartridge within the tape drive for loading. It replaces the cartridge latch assembly on drives without automatic cartridge loaders.

Automatic Cartridge Loader Sensors and Motors

Load Motor Complete Sensor

This senses a disk on the output shaft of the load motor and is used for positioning the motor at its up or down position.

Cartridge Latched Sensor

This sensor indicates that the loader tray is in the down position where the tape drive can thread tape. This sensor initiates the thread operation. The tape drive also uses this to control how long the latch solenoid signal is left on.

Cartridge Present Sensor

This indicates that a cartridge is present in the loader tray. It becomes active before the cartridge has been pushed all the way into the tray. The cleaning cartridge does not activate this sensor when it is in the tray.

File Protect Switch

This is used to detect the file protect condition of the cartridge. It is also used to indicate that a cleaning cartridge is in the tray if the cartridge present sensor is not active.

Feed Complete Switch

This indicates that a cartridge has been pushed all the way into the loader tray so that when the tray is driven down, the cartridge will seat on the alignment pins. This will indicate to the feeder that the forward drive can be turned off, the tracks opened and the load motor may be driven down.

Cartridge in Stack Sensor

This indicates that cartridges are loaded in one or more of the top five cells of the input stack.

Load Motor

This motor is used to drive the load tray up or down to release or seat the cartridge on the aligning pins.

Input Motor

This motor is used to drive the input rail assemblies down to position the cartridge for insertion by the feed assembly.

Cartridge Staged Sensor

This senses that a cartridge is in feed station.

Tracks Feed Sensor

This sensor indicates that the tracks have moved in from their open position.

Tracks Closed Sensor

This indicates that the tracks have closed past the position where they stop if a cartridge was anywhere in the feed position. This is used to sense if a cartridge is in the feed position.

Extract Complete Sensor

This indicates that a cartridge has been fed completely back into the feed position in the stack. With this indication, the feeder motor will stop.

Stack Up Position Sensor

This sensor is used to position the output stack.

Stack Low Position Sensor

This indicates that the output stack is full. This condition will inhibit input stack operations until cartridges are removed from the output stack.

Feeder Solenoid

This solenoid is used to force the feeder belts against the sides of the cartridge on either a load or unload operation.

Feed Motors Right and Left

These motors turn the feed belts that drive the cartridge into or out of the load assembly.

Output Motor

This motor is used to drive the output stack assembly up or down thru a worm gear and threaded shaft.

Real Time Statistical Analysis and Reporting System

Real Time Statistical Analysis and Reporting System

Statistics or counts of specified hardware events are accumulated each and every time a cartridge is mounted. These statistics are then combined with the preceding history of the device to produce measures of performance trends for the device. Alert messages are generated when service representative action is required. When statistics indicate the customer should clean the drive, a "CLEAN" message is posted on the drive's message display pod.

There is a device condensed statistical history data record for each device attached to a control unit. These records are used to develop device dependent performance trends for generating alert messages for the device. These records are also used to develop string and control unit performance trends for generating alert messages for the string or control unit.

These hardware performance measures are used to identify:

- When a device requires cleaning.
- When a device is degraded in performance and should be repaired.
- When a string of devices are degraded in performance and should be repaired.
- When a control unit is degraded in performance and should be repaired.

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